WILTRON

560A SCALAR NETWORK ANALYZER
5600 AUTOMATED SCALAR NETWORK ANALYZER SYSTEM (VOL 1)

OPERATION AND MAINTENANCE MANUAL

APPLICABLE 560A SERIAL NUMBERS

431001 and up

NOTE

This manual is either the Model 560A Scalar Network Analyzer manual or the Network Analyzer volume (Vol. I) of the 5600 Automated Scalar Network Analyzer System manual.

WILTRON

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2 MODEL 560A SCALAR NETWORK ANALYZER OPERATION AND MAINTENANCE MANUAL

3 SERIES 6600A PROGRAMMABLE SWEEP GENERATORS, MULTIBAND (OR SINGLE-BAND) MODELS, OPERATION AND MAINTENANCE MANUAL

4 HP 85 OWNER'S MANUAL AND PROGRAMMING GUIDE, and Other Pertinent Data
(supplied in separate binder)

5 5600 SOFTWARE USER'S GUIDE
(supplied in separate binder)

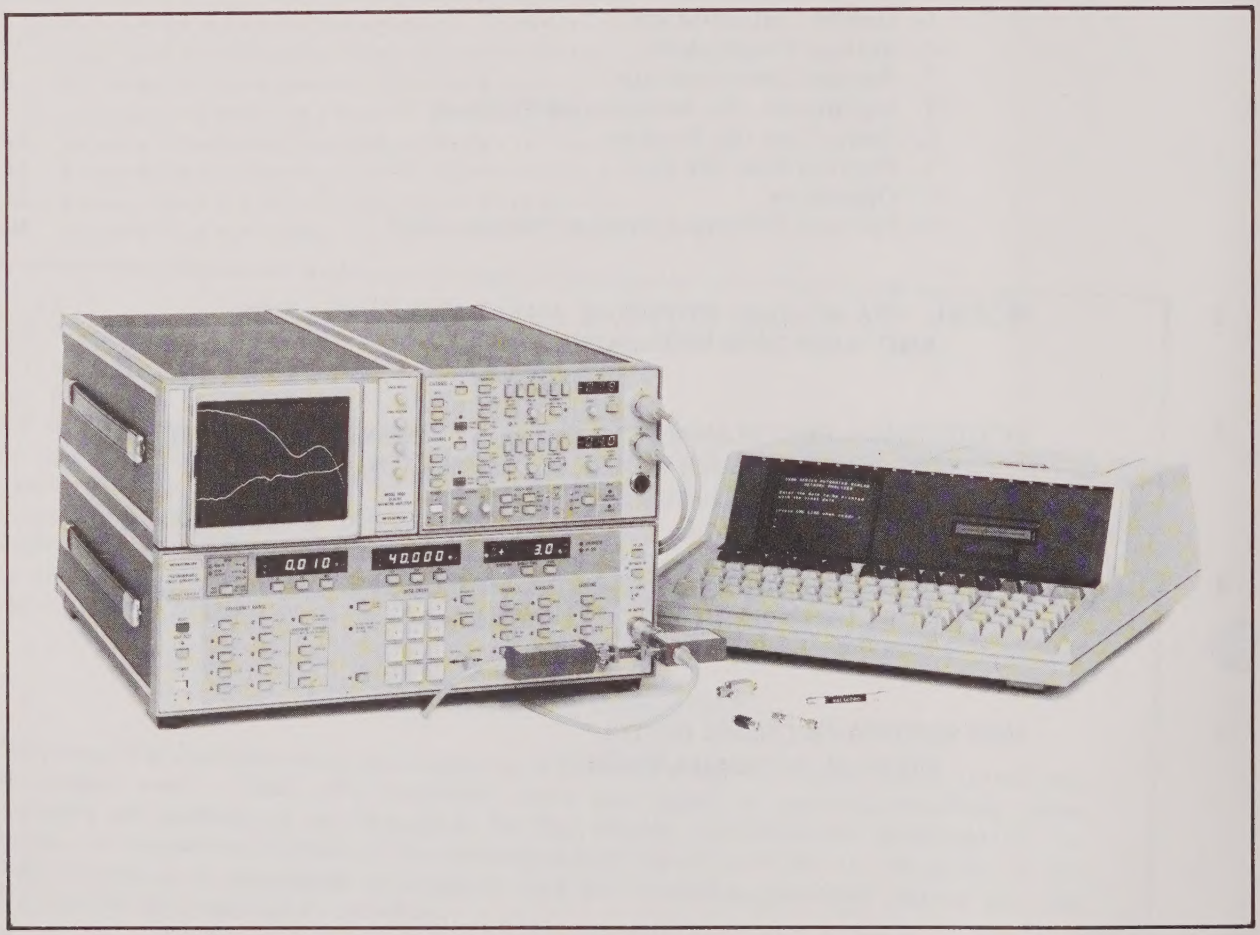


Figure 1. Model 5600 Automated Scalar Network Analyzer System

PART 1

SYSTEM INFORMATION

1. GENERAL INFORMATION

This manual provides operation and maintenance information for the 5600 Series Automated Scalar Network Analyzer System (Figure 1). This manual is organized in five parts, as follows:

Part 1 - System Information: contains information pertaining to the description, specifications, accessories, unpacking, preparation for use, and operation of the 5600 Series system.

Part 2 - 560A Scalar Network Analyzer: contains the Operation and Maintenance (O&M) Manual for the network analyzer.

Part 3 - 6600A Series Sweep Generator: contains the O&M manual for the applicable sweep generator model.

Part 4 - 85 Desktop Controller: the HP 85 Owner's Manual and Programming Guide. This manual, along with other pertinent HP 85 data, is contained in a separate binder.

Part 5 - 5600 Software User's Guide: the User's Guide for the 5600 Series preprogrammed software cartridge. This manual is bound separately.

2. SYSTEM DESCRIPTION

The 5600 Series is a completely automated system for making return loss, transmission (insertion) loss or gain, absolute power, and power sweep measurements over a model-dependent frequency range between 10 MHz and 40 GHz (Table 1). Each 5600 in the series includes a Model 560A Scalar Network Analyzer (with detectors and SWR Autotester),* a Model 85 Desktop Controller (with a preprogrammed software cartridge), a sweep generator from the 6600A Series family (Table 1), and all necessary interconnecting cables and accessories.*

*There is no SWR Autotester or detector supplied with the 5640 system and no SWR Autotester supplied with the 5636 system. Note also that all required waveguide for the 5640 must be supplied by the user.

Table 1. 5600 Series Models

SYSTEM MODEL NUMBER	SWEEP GENERATOR MODEL NUMBER	FREQUENCY RANGE
5609	6609A	10 to 2000 MHz
5617	6617A	.01 to 8 GHz
5636	6636A	18 to 26.5 GHz
5637	6637A	2 to 18 GHz
5647	6647A	.01 to 18 GHz
5640	6640A	26.5 to 40 GHz
5653	6653A	2 to 26.5 GHz
5659	6659A	.01 to 26.5 GHz
5663	6663A	2 to 40 GHz
5669	6669A	.01 to 40 GHz

3. SYSTEM SPECIFICATIONS

The specifications for the 5600 Series are listed in Table 2. Specifications for the individual instruments in the system are listed in the individual O&M or owner's manuals.

Table 2. System Specifications

GENERAL

Channels: Two channels (A&B) are used for programmed measurements between .01 and 40 GHz. Return loss is measured on channel A, and transmission (insertion) loss or gain and absolute power are measured on channel B. For measurements on the 5640 between 26.5 and 40 GHz, three channels are used. Detected samples of reflected, transmitted, and incident power are respectively displayed on channels A, B, and R.

Dynamic Measurement Range:
10 MHz to 40 GHz:*

A channel: 71dB (+16 dBm to -55 dBm)

B channel: 71 dB (+16 dBm to -55 dBm)

26.5 GHz to 40 GHz (5640 only):

A, B, R Channels: Determined by user-selected waveguide detectors. WILTRON 560-7S50 Option 3 WSMA Detectors are specified over the 10 MHz to 34 GHz range.

*As seen by SWR Autotester's internal detector, typically 13 dB below input power.

Amplitude Resolution: 0.01 dB

Frequency Resolution: 1 MHz

Data Correction: System residuals, including the average of open and short reflections, are stored with 0.01 dB resolution for automatic subtraction from test data.

Measurement Time: 100 msec for signals greater than -30 dBm, 270 msec for signals less than -30 dBm.

Smoothing Filters: Automatically switched in for signal levels below -30 dBm.

Network Analyzer CRT: 8 vertical by 10 horizontal divisions. One division = 1.22 cm. Single-beam standard persistance (P31) phosphor CRT with internal graticule.

CRT Camera: Compatible with Tektronix C5A, B and C.

OPERATION

Software: A preprogrammed software cartridge is supplied which prompts the operator on the desktop controller screen for all required inputs. All measurements, data storage, accuracy enhancements, dwell time and filter selection, averaging of residuals, determination of scale divisions and limits, and data plots or tabulations are performed automatically. Refer to the Model 85, 560A, & 6600A manuals for custom-programming guidance.

Two optional software cartridges are also available. Option P1 Enhanced Accuracy Program and Component Kit achieves return loss measurement accuracy that is equivalent to that of a test system with 60 dB directivity. Over the 10 MHz to 18 GHz range, the system measures return loss from 0 to 55 dB and produces hard-copy plots of error-corrected data.

Option P2 provides the capability of locating faults at distances up to 500 feet along transmission lines operating anywhere over the 10 MHz to 18 GHz range.

Hard-copy Output: Curves and/or tabulations of return loss, transmission loss or gain, and absolute power are printed by desktop controller. Values for the Y-axis scale range limits, resolution, and data centerline are determined automatically to optimize data presentation. Operator-selected values may be substituted. Option 8 adds an HP 7470A Plotter.

Manual Operation: Via instrument front panel controls when instruments are returned to the local mode.

Operating Temperature Range: 0° C to +50° C (5° C to 40° C for Model 85 Controller).

System Power:
100V/120V/220V/240V +5%, -10%,
48-66 Hz, 350 watts maximum.

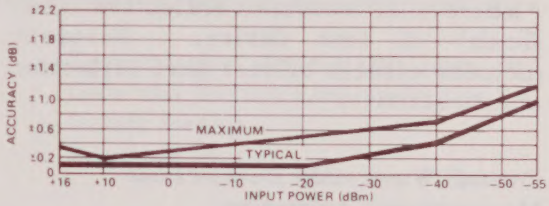
SYSTEM ACCURACY

Overall Transmission Loss or Gain Measurement Accuracy: Uncertainties resulting from frequency response of detectors, SWR Autotester, sweep generator and from other test system components are subtracted automatically from test data. Overall accuracy is then:

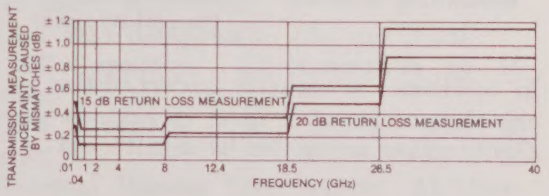
Transmission Loss or Gain Accuracy = **Channel Accuracy + Mismatch Uncertainty***

*Effects of sweep generator, test device, SWR Autotester and detector mismatch can be significant. This mismatch uncertainty is minimized by the exceptionally low reflection characteristics of the WILTRON detector, sweep generator and SWR Autotester.

Channel Accuracy (25° C):



Mismatch Uncertainty (Typical):**



**Varies with the return loss of the detector, SWR Autotester, connecting cables, the source impedance of the sweep generator, and the value of the measured reflection.

Overall Coax Return Loss Measurement Accuracy: Uncertainties resulting from SWR Autotester and sweep generator frequency response and from system open and short characteristics are subtracted automatically from test data. Overall Accuracy is then:

Return Loss Accuracy = **SWR Accuracy + Channel Accuracy**

Table 2. System Specifications (Continued)

SWR Autotester :

System Model	SWR Autotester Model	Test Port Connector	Directivity and Accuracy*				
			.01–2 GHz	2–8 GHz	8–18 GHz	18–26.5 GHz	26.5–40 GHz
5609(M)	560–6N50	Type N Male	40dB $0.01 \pm 0.06P^2$	N/A	N/A	N/A	N/A
5617(M) 5637(M) 5647(M)	560-97A50-1	GPC7	40 dB $0.01 \pm 0.06P^2$ (Not 5637)	40 dB $0.01 \pm 0.06P^2$	40 dB $0.01 \pm 0.1P^2$	N/A	N/A
Option 6	560-97N50-1	Type N Male	38 dB $0.013 \pm 0.08P^2$	38 dB $0.013 \pm 0.08P^2$	38 dB $0.013 \pm 0.12P^2$	N/A	N/A
Option 5 5636(M) 5653(M) 5659(M)	560-98S501	WSMA Male	38 dB $0.013 \pm 0.1P^2$	38 dB $0.013 \pm 0.1P^2$	35 dB $0.13 \pm 0.1P^2$	35 dB $0.018 \pm 0.12P^2$	N/A
5663(M) 5669(M)	560-98K50	K Male	35 dB $0.018 \pm 0.05P^2$ (Not 5663)	35 dB $0.018 \pm 0.05P^2$	35 dB $0.018 \pm 0.05P^2$	32 dB $0.025 \pm 0.05P^2$	30dB $0.032 \pm 0.18P^2$

*Where ρ is measured reflection coefficient of test device. Accuracy includes effects of test port reflection and directivity.

Overall Waveguide Return Loss Measurement Accuracy:

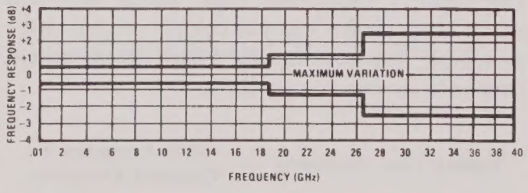
Return Loss Accuracy = User-Selected Coupler Accuracy + Channel Accuracy

In addition, mismatch uncertainties of the detectors used in a waveguide reflectometer setup can be significant.

Overall Absolute Power Measurement Accuracy:

Absoulte Power Accuracy = Channel Accuracy + Detector Frequency Response

Detector Frequency Response:



PHYSICAL

Network Analyzer and Sweep Generator:

Size: Standard Locked Stack: 429 W x 500 D x 266 mm H + 10 mm for feet (16.9 W x 19.7 D x 10.5 in. H + 3/8 in. for feet).

Weight:

MODEL	lb	kg
5609	52.5	23.6
5617	52.5	23.6
5636	54.5	24.5
5637	56.5	25.4
5640	54.5	24.5
5647	56.5	25.4
5653	58.5	26.3
5659	58.5	26.3
5663	59.5	26.8
5669	59.5	26.8

Rack Mounting (Option 1): Units supplied with mounting ears and chassis track slides (90° tilt) installed. Units fit standard 19-inch rack.

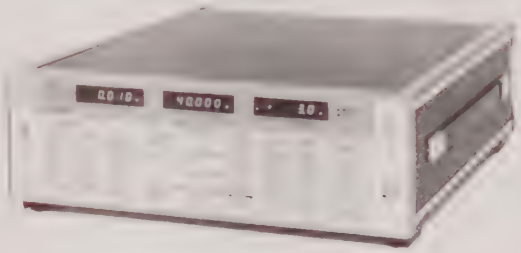
Controller:

Size: 419 W x 452 D x 159 mm H (16.5 W x 17.8 D x 6.3 in H)

Weight: 9.06 kg (20 lb)

SYSTEM ELEMENTS

Sweep Generator:

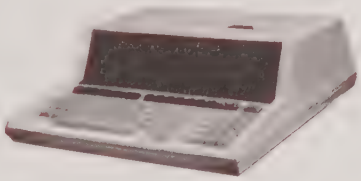


A WILTRON 6600A Series Programmable Sweep Generator is the signal source for system measurements. The specifications and all related operation and maintenance data for the sweep generator are located in Part 3.

Network Analyzer:

The WILTRON 560A Scalar Network Analyzer is the measuring instrument in the system. It provides test data via the IEEE 488 Bus (GPIB) for the controller's CRT plot, hard-copy plot, and tabular printout. The 560A also provides a simultaneous display of return loss, transmission (insertion) loss or gain, and absolute power in either a refreshed or real time display mode. The specifications and all related operation and maintenance data for the network analyzer are located in Part 2.

Desktop Controller:



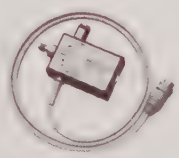
The Model 85 Desktop Controller and Preprogrammed Tape Cartridge provide GPIB control for programmed system measurements. The Preprogrammed Tape Cartridge provides programs for the following types of measurements:

- Transmission (insertion) Loss or Gain and Return Loss
- Power Sweep
- Absolute Power

Selected Specifications:

Memory: 32k bytes
CRT Size (Diagonal): 12.7 cm (5 in)
CRT Capacity: 32 characters by 16 lines
CRT Graphics: 256 x 192-dot plotting area
Thermal Printer Line Width: 32 characters
Thermal Printer Graphics: Dot-for-dot reproduction of controller CRT image.
Interface: GPIB (IEEE-488), IEC-625

SWR Autotester:



A WILTRON 560 Series SWR Autotester (refer to paragraph 4 to determine specific model) provides a combined bridge

and detector for return loss measurements. The 560 Series SWR Autotesters integrate in one small package a broadband, high-directivity bridge; a detector; a low-reflection test port; a reference termination; and a connecting cable. The unit makes accurate return loss (SWR) measurements on channel A. The output is a detected signal, varying in proportion to reflections from the test device connected to the test port. Optional extender cables may be used without degradation in performance. An open/short termination is provided with each unit.

Detectors:

A WILTRON 560 Series Detector (refer to paragraph 4 to determine specific model) provides the detector for coax (or with a suitable adapter, waveguide) measurements of transmission (insertion) loss or gain and absolute power. The specifications and all related operation and maintenance data for the detectors are located in Part 2.

Optional Graphics Plotter:

Description: HP 7470 Plotter
Plotting sizes: Accommodates media sizes 8.5 x 11 in. (ANSI A) and 210 x 297 mm (ISO A4)
Mechanical limits: (approx.) Y-axis, 191 mm (7.5 in.); X-axis, 273 mm (10.7 in.) for metric setting or 258 mm (10.2 in.) for English setting
Addressable resolution (step size): 0.025 mm (0.001 in.)
Repeatability: For a given pen, 0.10 mm (0.004 in.); pen-to-pen, 0.20 mm (0.008 in.)
Power requirements: Source, 100, 120, 220, 240 V ~ -10%, +5%; frequency, 48-66 Hz; consumption 25 W maximum
Size: 127 H x 432 W x 343 mm D (5" x 17" x 13.5")
Weight: Net, 6.1 kg (13.5 lb)
Pens: Two, fiber-tip
Media: Paper and Hewlett-Packard overhead transparency film

Plotter Supplies Furnished: Paper and an assortment of pens are furnished.

OPTIONS

Option 1: Rack Mounting for 560A Network Analyzer and Sweep Generator (tilt sides included.)

Option 2: Adds to sweep generator a 10 dB step attenuator with a 70 dB range. Not available on 5640, 5663 or 5669.

Option 4: GPC-7 Test Ports on 5617(M), 5637(M) or 5647(M).

Adds: 34AN50 Adapter, GPC-7/Type N Male;
34ANF50 Adapter, GPC-7/Type N Female;
34AS50 Adapter, GPC-7/WSMA Male;
34ASF50 Adapter, GPC-7/WSMA Female.

Option 5: WSMA Test Ports on 5617(M), 5637(M) or 5647(M).

Adds: 560-98S50-1 SWR Autotester, WSMA Male Test Port Connector with Option 1, 38 dB directivity ;

Table 2. System Specifications (Continued)

	560-7S50 Detector, WSMA Male Connector; 34SFSF50 Adapter, WSMA Female/Female; 22SF Open/Short.
Deletes:	560-97A50-1 GPC-7 SWR Autotester, 560-7A50 GPC-7 Detector, 560-22A Open/Short.
Option 6:	Type N Test Ports on 5617(M), 5637(M), or 5647(M)
Adds:	560-97N50-1 SWR Autotester, Type N Male Test Port Connector with Option 1, 38 dB directivity; 560-7N50 Detector, Type N Male Connector; 34NFNF50 Adapter, Type N Female/Female 22NF Open/Short.
Deletes:	560-97A50-1 GPC-7 SWR Autotester. 560-7A50 GPC-7 Detector, 560-22A Open/Short.
Option 8:	Adds HP 7470A Plotter and WILTRON 2100-2 GPIB Cable

Table 3. Model 5609 (5609-75) System, Equipment and Accessories

MODEL OR PART NO.*	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6609A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
	Microwave Components Kit, consisting of:
560-6N50 (560-6N75)	SWR Autotester, with N-male test port connector
22NF (22N75)	Open/Short Termination
560-71N50 (560-71N75)	RF Detector with N-Male connector
(12N75)	Adapter, 50 ohm to 75 ohm, N male-to-male connector
34NN50A	Adapter, N male-to-mal- connectors
34NFNF50 (34NFNF75)	Adapter, N female-to-female connectors
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359	Multiwire, 25-pin to 9-pin Interconnect Cable
5600X	Combiner Kit

*The 75-ohm equipment shown in parentheses is supplied with the 5609-75 system.

4. EQUIPMENT AND ACCESSORIES SUPPLIED

Listings of the equipment and accessories supplied with the various 5600 models are given in Tables 3 thru 11. Photographs of the equipment and accessories are given in Figure 2.

Table 4. Model 5617 System, Equipment and Accessories

MODEL OR PART NO.	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6617A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
	Microwave Components Kit, consisting of:
560-97A50-1	SWR Autotester with GPC-7 test port connector
22A	Open/Short Termination
560-7A50	RF Detector with GPC-7 connector
34NN50A	Adapter, N male-to-male
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359	Multiwire, 25-pin to 9-pin Interconnect Cable
5600X	Combiner Kit

Table 5. Model 5636 System, Equipment and Accessories

MODEL OR PART NO.	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6636A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
560-7S50-2	RF Detector with WSMA-male connector (3 each)
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359	Multiwire, 25-pin to 9-pin Interconnect Cable
5600X	Combiner Kit
	NOTE All required waveguide components must be supplied by the user.

Table 6. Model 5637 System, Equipment and Accessories

MODEL OR PART NO.	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6637A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
	Microwave Components Kit, consisting of:
560-97A50-1	SWR Autotester, with GPC-7 test port connector
22A	Open/Short Termination
560-7A50	RF Detector with GPC-7 connector
34NN50A	Adapter, N male-to-male
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359	Multiwire, 25-pin to 9-pin Interconnect Cable
5600X	Combiner Kit

Table 7. Model 5640 System, Equipment and Accessories

MODEL OR PART NO.	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6640A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
560-10BX	Adapter Cable (3 each)
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359	Multiwire, 25-pin to 9-pin Interconnect Cable
5600X	Combiner Kit
	NOTE All required waveguide components must be supplied by the user.

Table 8. Model 5647 System, Equipment and Accessories

MODEL OR PART NO.	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6647A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
	Microwave Components Kit, consisting of:
560-97A50-1	SWR Autotester with GPC-7 connector
22A	Open/Short Termination
560-7A50	RF Detector with GPC-7 connector
34NN50A	Adapter, N male-to-male
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359	Multiwire, 25-pin to 9-pin Interconnect Cable
5600X	Combiner Kit

Table 9. Model 5653 System, Equipment and Accessories

MODEL OR PART NO.	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6653A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
	Microwave Components Kit, consisting of:
560-98S50-1	SWR Autotester with WSMA, Male connector
22S	Open/Short Termination
560-7S50-2	RF Detector with WSMA, male connector
34RSRS50	Adapter, WSMA male-to-male
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359	Multiwire, 25-pin to 9-pin Interconnect Cable
5600X	Combiner Kit

Table 10. Model 5659 System, Equipment and Accessories

MODEL OR PART NO.	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6659A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
	Microwave Components Kit, Consisting of:
560-98S50-1	SWR Autotester with WSMA, Male test port connector
22S	Open/Short Termination
560-7S50-2	RF Detector with WSMA, male connector
34RSRS50	Adapter, WSMA male-to-male
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359	Multiwire, 25-pin to 9-pin Interconnect Cable
5600X	Combiner Kit

Table 11. Model 5663 System, Equipment and Accessories

MODEL OR PART NO.	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6663A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
	Microwave Components Kit, consisting of:
560-98K50	SWR Autotester with K male test port
22KF	Open/Short Termination
560-7K50	Detector with K male connector
34KFKF50	Adapter, K female-to-K female
34RKRK50	Adapter, Ruggedized K to Ruggedized K
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359-1	Interconnect Cable
5600X	Combiner Kit

Table 12. Model 5669 System, Equipment and Accessories

MODEL OR PART NO.	DESCRIPTION
560A	Scalar Network Analyzer with Option 3, GPIB
6669A	Programmable Sweep Generator with Option 3, GPIB
85	Desktop Controller
	Microwave Components Kit, consisting of:
560-98K50	SWR Autotester with K male test port
22KF	Open/Short Termination
560-7K50	Detector with K male connector
34KFKF50	Adapter, K female-to-K female
34RKRK50	Adapter, Ruggedized K to Ruggedized K
2300-4	Software Cartridge for Model 85
2100-5	GPIB Interconnect Cable, 0.5 m
560-B-11359-1	Interconnect Cable
5600X	Combiner Kit

5. UNPACKING THE SYSTEM

The basic 5600 system comes packed in 3 boxes. One box holds the network analyzer, one the sweep generator, and one the desktop controller. Also, a box of microwave components (Figure 2) may be packed with either the network analyzer or the sweep generator. A box containing the remaining accessories that are listed in paragraph 4 and the accessories for the desktop controller that are listed in Appendix A of the HP 85 Owner's Manual is packed with the controller.

Unpack the system and verify that all of the equipment and accessories are included. When this has been accomplished, proceed to paragraph 6.

6. PREPARATION FOR USE

To set up and prepare the 5600 system for operation, perform the steps in subparagraphs a. thru e. below.

a. Install the Combiner Kit.

1. On the 560A (Figure 3),

   (a) unscrew the #8 posi-drive retaining screws and remove the two bottom corner brackets;

   (b) slide the two back feet to the rear and remove;

   (c) slide the right and left bottom corner trim strips to the rear and remove;

   (d) remove the tilt bail from between two front feet, by squeezing the two sides together and lifting straight away.

   (e) slide the two front feet to the rear and remove.

2. On the sweep generator,

   (a) unscrew the #8 posi-drive retaining screws and remove the two top rear corner brackets.

   (b) slide the right and left top corner trim strips to the rear and remove.

3. Place the 560A on top of the sweep generator and position it so that the sides of the instruments are aligned.

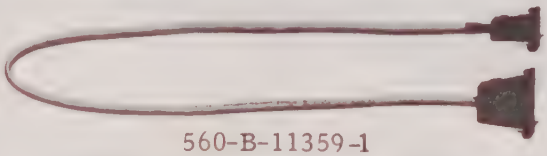
4. Refer to Figure 4 and perform the following:

   (a) On the right side (from the rear), slide the inner-interlock bar between the two instruments.

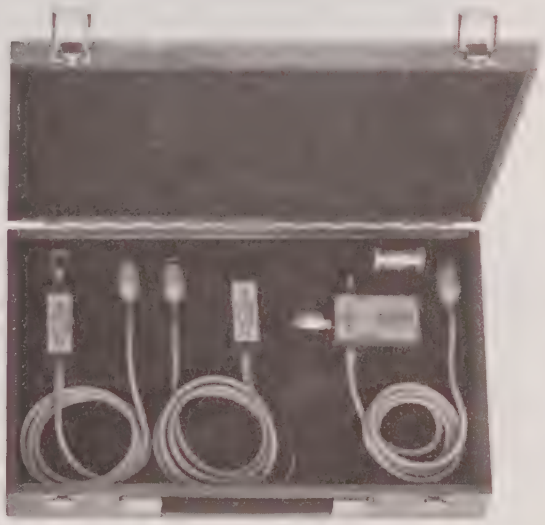
6600A SERIES SWEEP GENERATOR

560A SCALAR NETWORK ANALYZER

MODEL 85 DESKTOP CONTROLLER

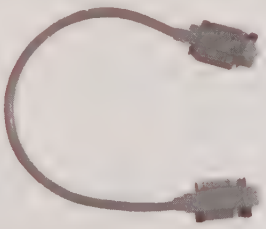


560-B-11359-1
INTERCONNECT CABLE

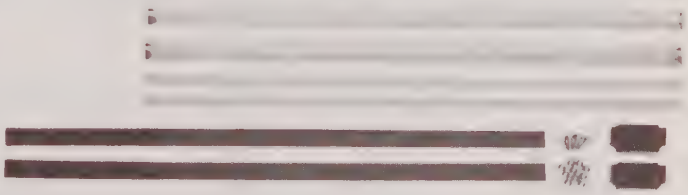


MICROWAVE COMPONENTS KIT

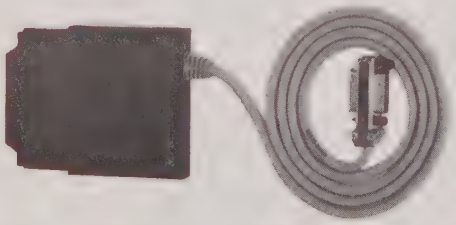
2300-4 SOFTWARE CARTRIDGE



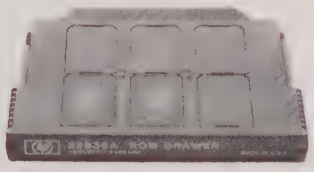
2100-5 GPIB INTERFACE CABLE



5600CX COMBINER KIT



GPIB INTERFACE FOR CONTROLLER



ROM DRAWER FOR CONTROLLER

Figure 2. 5600 System Equipment and Accessories

(b) Fasten the outer-interlock bar to the inner-interlock bar using four #6 flathead screws--do not tighten

(c) Repeat steps (a) and (b) above for the left side.

(d) Tighten the four outer-inter-lock-bar screws on each side.

(e) On each side, install the flat trim strip by sliding it in from the rear.

(f) Using four #8 posi-drive screws, install the two retainer plates.

b. Configure the Desktop Controller. Configure the desktop controller by inserting (1) the GPIB Interface module and (2) the ROM Drawer module, as shown in Figure 5. Refer to Appendix A of the HP 85 Owner's Manual, if necessary, for installation procedures.

NOTE

Covers for the ROM Drawer slots that have ROMs installed, along with the fuse and fuseholder for the alternate line voltage (115 or 220 Vac, whichever in not used), are stored in the thermal tape well in the top of the controller. Remove before use.

c. Interconnect the Equipment. Refer to Figure 6 and interconnect the network analyzer, sweep generator, and desktop controller.

d. Verify that System Equipment is Properly Addressed. Before leaving the factory, each item of the 5600 equipment is properly addressed to respond to programmed instructions. To insure that an address switch did not get changed in shipment, check that addresses are set as shown in Figure 7. Check also that the CR-CR/LF switches are set to CR/LF.

e. Verify that System Equipment is Set for Proper Line Voltage. Before leaving the factory, each item of 5600 equipment is set for the line voltage known to be present in the customer's country or region. To verify that the line voltage is properly set, refer to the 560A manual in Part 2, paragraph 2-3.1; the sweep generator manual in Part 3, paragraph 2-3; and the HP 85 Owner's Manual, Appendix B, page 271.

7. OPERATION

System operation - along with detailed instructions on how to perform return loss, transmission (insertion) loss or gain, absolute power, and power sweep measurements - is described in the 5600 Software User's Guide.

NOTE

The Model 85B controller, identified by a white label on the rear panel, should not be used with 2300-4 software previous to Revision 8. Revision 8 is compatible with both the 85A and 85B controller.

8. FACTORS AFFECTING SYSTEM PERFORMANCE

a. Desktop Controller Tape-Head Cleanliness. The occurrence of "READ" and "STALL" errors on the controller can indicate a dirty tape head. Instructions for tape-head care are given in the HP 85 Owner's Manual and Programming Guide, Appendix B, pages 281-283.

b. Write Protection for Tapes. To prevent the inadvertent loss of data stored on tape, "write-protect" the tape cartridge before installing it in the controller. To write-protect the tape, slide the "RECORD" tab on the tape (Figure 8) all the way to the left.

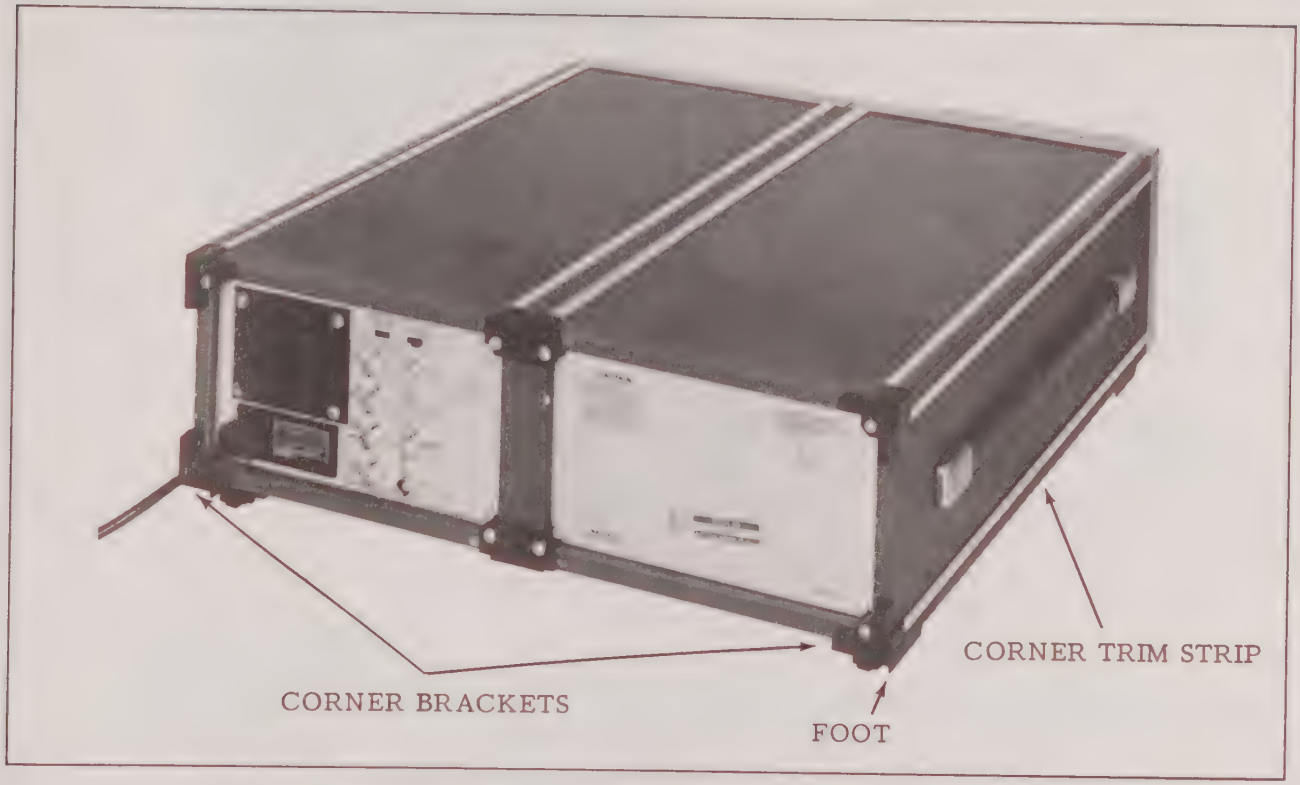


Figure 3. Network Analyzer, Rear View

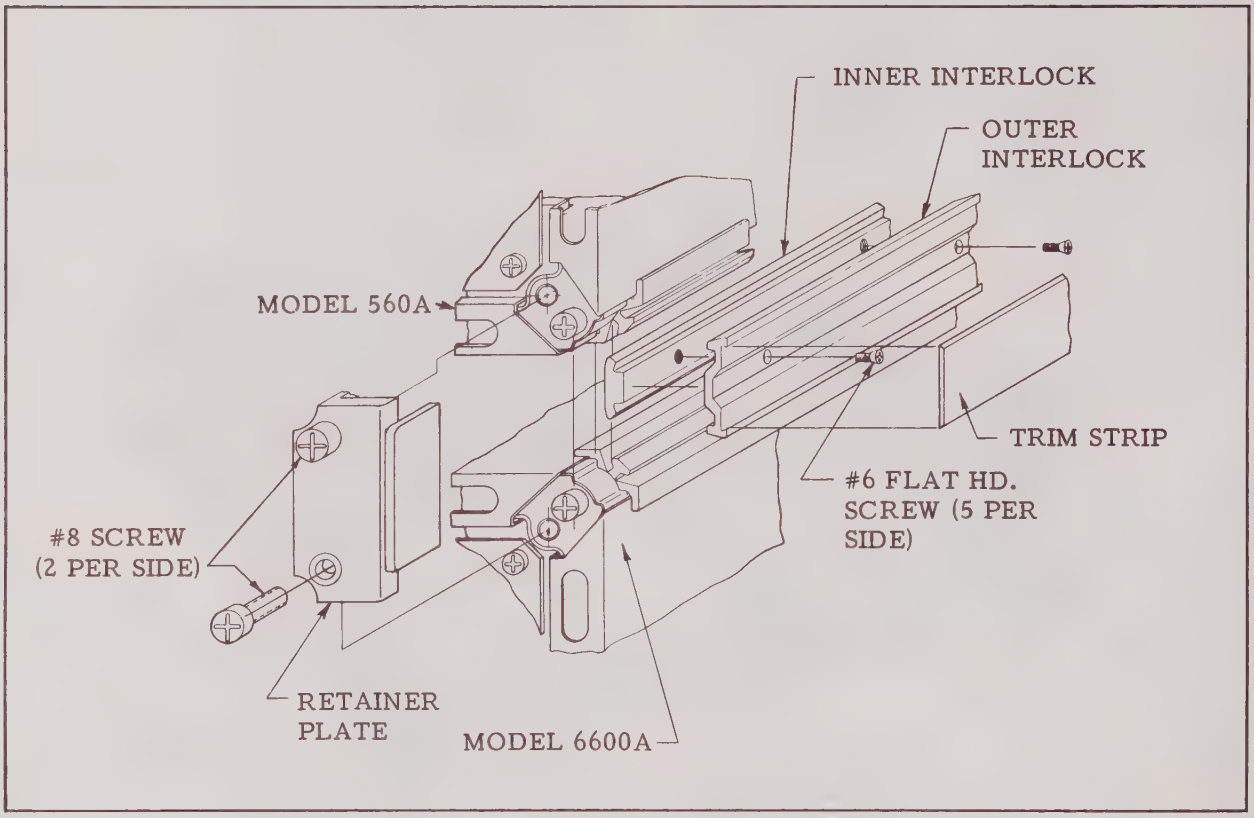


Figure 4. Combiner Kit Installation

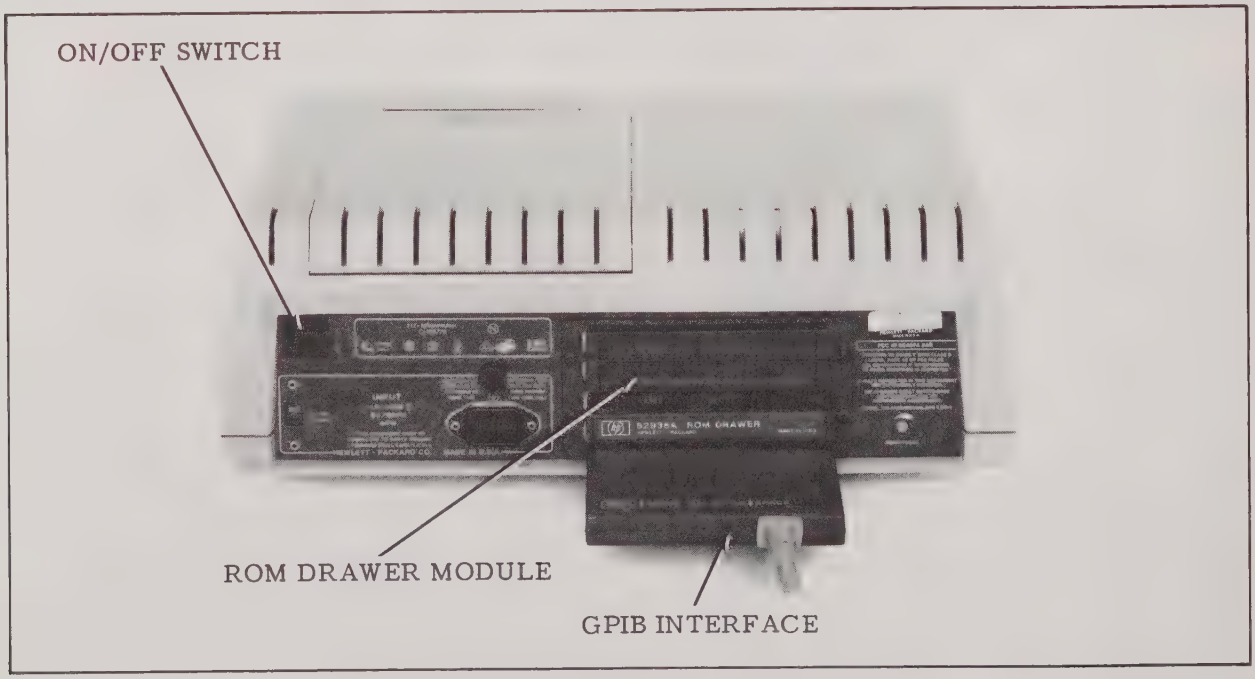


Figure 5. Desktop Controller, Rear Panel

CONNECTS TO OPTIONAL GRAPHICS PLOTTER OR OTHER GPIB INSTRUMENT

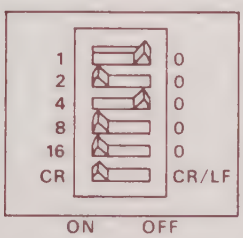
Rear Panel Switch Settings

Network Analyzer	Sweep Generator
LOW LEVEL CAL: NORMAL V/H OUT: RDCR	HORIZ OUTPUT DURING CW: OFF

Figure 6. 5600 System, Equipment Interconnections

WILTRON Model 6600A Sweep Generator
Address Switch Setting (Address 5)

CR-CR/LF to CR/LF



WILTRON Model 560A Network Analyzer
Address Switch Setting (Address 6)

CR-CR/LF to CR/LF

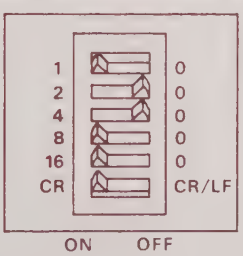


Figure 7. 5600 System Equipment Addresses

HP Model 7470
Address Portion of Address Switch:
Set for Address 8

A4-US Portion of Address Switch:
Set for A4

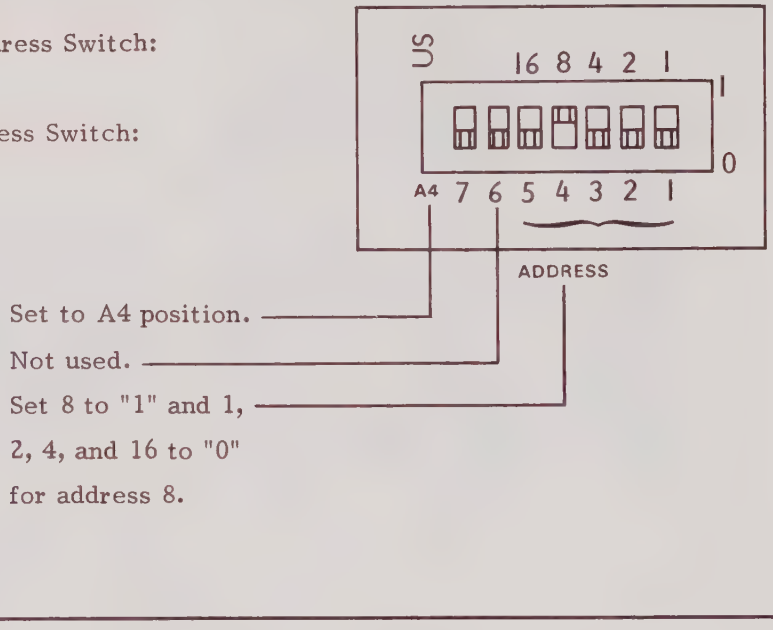


Figure 7. 5600 System Equipment Address (Continued)

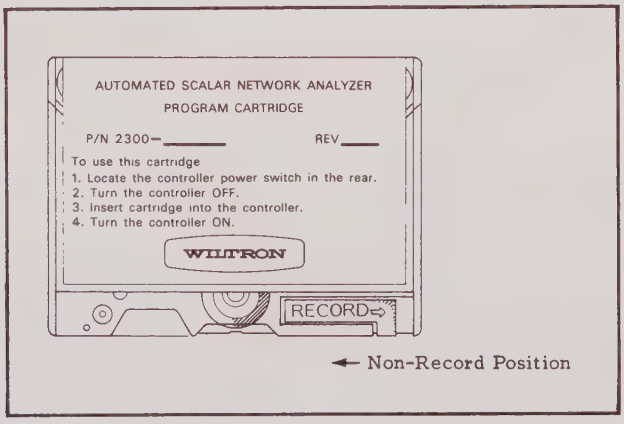


Figure 8. Program Cartridge

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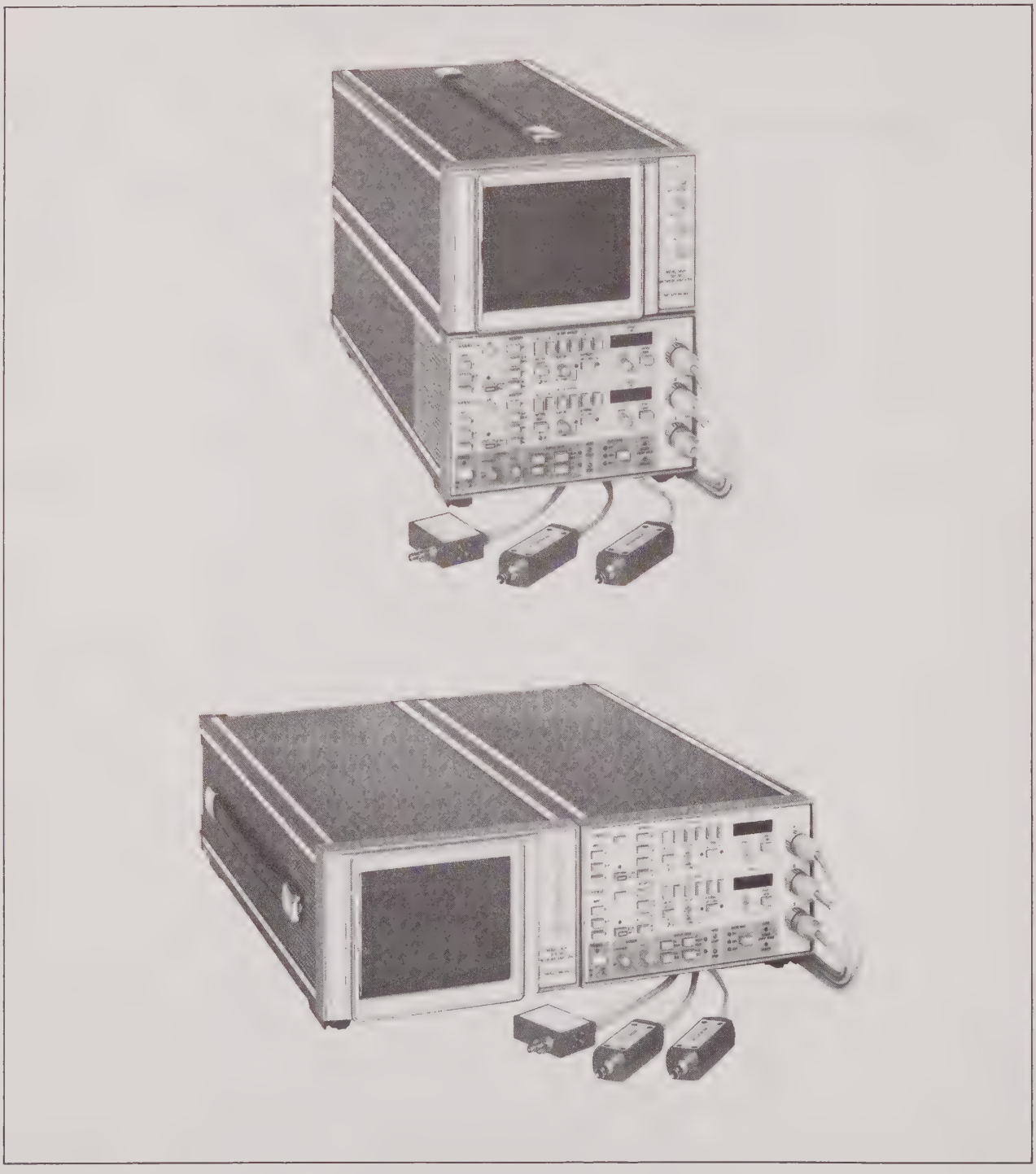


Figure 1-1. Top: Model 560A Scalar Network Analyzer Option 2 Vertical Configuration. Bottom: Model 560A Horizontal Configuration. (Components shown are ordered as separate items. See paragraph 1-2.)

SECTION I
GENERAL INFORMATION

1-1 INTRODUCTION

This manual describes the Model 560A Scalar Network Analyzer and Model 560 series microwave components. The manual is organized as follows:

SECTION I, GENERAL INFORMATION, provides a general description and specifications for the network analyzer; 560-97, -98, and -6 series SWR Autotesters; and 560-7 and 560-71 series RF detectors. Also included is a description of the IEEE-488 (IEC 625) General Purpose Interface Bus (GPIB).

SECTION II, INSTALLATION, contains initial inspection, preparation for use, and GPIB interconnection data. This section also includes information on shipment and storage of the network analyzer and its dedicated microwave components.

SECTION III, OPERATION, provides information on the controls and connectors, and on the Option 3 GPIB capability. This section also provides checkout and troubleshooting data using front panel controls.

SECTION IV, PERFORMANCE VERIFICATION, contains performance verification philosophy and procedures for the 560A, including the Option 3 GPIB circuits (A6 printed circuit board).

SECTION V, CALIBRATION, provides adjustment instructions for the Front Panel (A1), Digital (A2), Log Amplifier (A3), and Optional GPIB Interface (A6), printed circuit boards.

SECTION VI, PARTS LISTS, contains listings of replaceable electrical and mechanical parts for the 560A, including the CRT mainframe and Option 3 GPIB Interface (A6) printed circuit board.

SECTION VII, SERVICE, provides service instructions for the 560A, including CRT mainframe and Option 3 GPIB Interface (A6) printed circuit board. This section contains troubleshooting charts; disassembly instructions; circuit descriptions; and schematic, block and timing diagrams.

1-2 DESCRIPTION OF THE MODEL 560A SYSTEM

The Model 560A Scalar Network Analyzer system measures return loss, insertion loss, gain, and absolute power over a broad frequency range. The system (Figure 1-1) is composed of a network analyzer and one, two, or three microwave components. These microwave components (depending upon application) may consist of either an SWR Autotester, an RF detector, or a combination of the two. The Model 560A Scalar Network Analyzer is described in paragraph 1-4.1, and the two models of SWR Autotesters (560-97, -98, and -6 series) and two models of RF detectors (560-7 and 560-71 series) are described in paragraphs 1-4.2 and 1-4.3, respectively.

1-3 EQUIPMENT REQUIRED BUT NOT SUPPLIED

The Model 560A Scalar Network Analyzer system requires interconnection with a sweep generator to provide the necessary vertical, horizontal, and blanking voltages (Table 1-1). While the 560A is designed for use with the WILTRON 6600/6600A Series Programmable Sweep Generator, it is also compatible with other sweep generators.

1-4 SPECIFICATIONS

The following paragraphs provide a description and specifications for the 560A Scalar Network Analyzer; 560-97, -98, and -6 series SWR Autotesters; and 560-7 and -71 series RF detectors.

1-4.1 Model 560A Scalar Network Analyzer

The Model 560A Scalar Network Analyzer is a GPIB-compatible, three-channel microwave measurement instrument. The three channels consist of two measurement channels (A, B) and one reference channel (R), which allow the network analyzer to simultaneously display the results of two measurements. The 560A also contains internal memory circuits that provide two different functions — measurement-normalization memory and display-refresh memory. The measurement-normalization memory stores transmission measurement system residuals and return loss calibration data. The display-refresh memory provides a non-flickering display, regardless of sweep generator sweep speed. The refresh memory also provides for a slow, 30-second sweep for an external X-Y plotter.

A complete listing of the 560A specifications is contained in Table 1-1.

Table 1-1. Model 560A Scalar Network Analyzer Specification Chart

FREQUENCY RANGE: See SWR Autotester and RF detector specifications, Table 1-2 and Table 1-3, respectively.

CHANNELS: Three (A, B, R) with pushbutton selection of A, B, R, A-R and B-R. Detected input signals supplied by detectors or SWR Autotester, which may be interchanged without adjustment. Two channels are displayed simultaneously.

DYNAMIC MEASUREMENT RANGE AND SENSITIVITY:
A and B with Detectors:*
71 dB (+16 dBm to −55 dBm)
A and B with SWR Autotester:
65 dB (+10 dBm to −55 dBm)**
R with Detector:*
46 dB (+16 dBm to −30 dBm)

*With 75Ω detectors, maximum output is +13 dBm.

**As seen by internal detector, typically 13 dB below input power with 0 dB return loss at test port.

OFFSET CONTROL: Positioning of A and B traces is independently and continuously adjustable over $> \pm 65$ dB range. When trace is on reference line, power is displayed in dBm on 3-digit LED readout with 0.1 resolution. Offset is displayed in dB relative to a 0 dB reference level or in dBm relative to a 0 dBm reference level.

ZERO dB REFERENCE SET: Positions reference trace at selected 0 dB reference line.

REFERENCE POSITION LOCATOR: Displays reference trace to locate reference line. Position of reference line screwdriver-adjusted.

OFFSET ZERO POSITION: Moves trace to the position it would have if OFFSET were adjusted to 0 dB.

RESOLUTION: Independent control for A and B in steps of 0.2, 0.5, 1, 2, 5, 10 dB per division. Other values (3, 6, 15 dB, etc.) obtained by depressing multiple pushbuttons.

MEMORY:

STORE TRACE: Stores displayed trace(s) in 1024-point memory. Used to store system residuals and the average of open/short reflections for subtraction from input test data.

AVERAGE: Averages data in memory with input test data and displays the result. Used to average system open/short return loss characteristics for subtraction from input test data.

SUBTRACTION: Subtracts data in memory from input test data and displays result.

RECALL: Displays stored data.

UNCALIBRATED SWEEP INDICATOR: Lights when external sweep generator sweep rate is too fast for memory.

DISPLAY MODES:

REAL TIME: Horizontal sweep is synchronized with ramp from external sweep generator.

REFRESH: External sweep generator ramp is digitized and stored in 1024-point memory (512 points for dual trace). Stored data is updated continuously at sweep generator sweep rate. Steady, nonflickering display is provided regardless of sweep generator sweep rate. Vertical resolution is 512 points for single or dual traces.

REFRESH HOLD: Updating of display data is stopped. Display is frozen.

X-Y PLOT (REAL TIME): Provides pen lift, vertical, and horizontal signals for X-Y plot. Dual traces are automatically recorded by sweeping A and B channels sequentially.

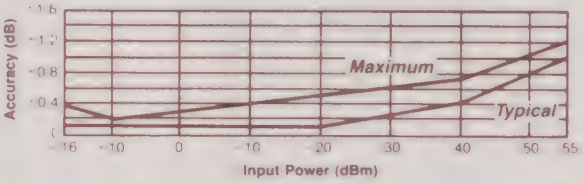
X-Y PLOT (REFRESH): Display is frozen and then plotted at 30-second sweep rate. Dual traces are automatically recorded by sweeping A and B channels sequentially. After 1 second, sweep may be aborted and returned to start.

SMOOTHING FILTERS: Three levels of filtering optimize low-level signal displays.

MARKERS: Threshold and tilt control of externally-applied birdie or video markers.

ACCURACY

A AND B CHANNEL ACCURACY:
±0.2 dB at +10 dBm, decreasing at a rate of 0.1 dB per each 10 dB increment to ±0.7 dB at −40 dBm, to ±1.0 dB at −50 dBm, and to ±1.2 dB at −55 dBm.



OVERALL RETURN LOSS MEASUREMENT ACCURACY: Uncertainties resulting from SWR Autotester and sweep generator frequency response and system open/short characteristics are subtracted automatically from test data. Overall accuracy is then:

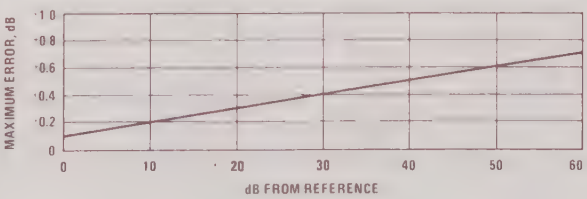
SWR Autotester Accuracy (Table 1-2)
+
A and B Channel Accuracy (above)

OVERALL TRANSMISSION LOSS/GAIN MEASUREMENT ACCURACY: Uncertainties resulting from frequency response of detectors, SWR Autotester, sweep generator and other test system components are subtracted automatically from test data. Overall accuracy is then:

A and B Channel Accuracy*

* Effects of sweep generator, test device, and detector mismatch may be significant. Mismatch errors are either minimized by the exceptional low reflection characteristics of the 560 detectors (see detector return loss specifications) or padded by the insertion loss of the SWR Autotester (paragraph 1-4.2).

RATIO MEASUREMENT ACCURACY (A-R, B-R):



Above curve includes all log amplifier uncertainties. Errors due to Detector Mismatch variations must be accounted for separately. The use of memory eliminates errors due to detector frequency variations.

OVERALL ABSOLUTE POWER MEASUREMENT ACCURACY:
Absolute power measurement accuracy is determined by the frequency response accuracy of the detector and the absolute accuracy of the log amplifier. Absolute power accuracy is then:

Detector Frequency Response Accuracy (Table 1-3)
+
A and B Channel Accuracy (above)

CRT DISPLAY

CATHODE RAY TUBE (CRT): 8 vertical by 10 horizontal divisions. One division = 1.22 cm. Single beam, standard persistence (P31) phosphor CRT with internal graticule.

CRT BEAM CONTROLS: Intensity, Focus, Trace Rotation, and Horizontal Position.

CAMERA: Compatible with Tektronix C5A, B, or C model camera.

HOOD: Compatible with Tektronix 016-0260-00 Hood.

INPUT CONNECTIONS

HORIZONTAL INPUT: HORIZONTAL SELECT switch selects one of three types of sweep ramp inputs at rear panel HORIZONTAL INPUT connector: 0 to +10V, 0 to +15V, and −8 to +8V. BNC connector, 100k ohms input impedance.

MARKER INPUT: 1mV to 10V peak input, rear panel BNC connector, 100k ohms input impedance. In addition, a −3V to −10V input to Z AXIS rear panel connector provides markers.

Z AXIS INPUT: +3 to +10V blanks and maintains trace amplitude during switching of sweep generator oscillators. −3V to −10V introduces markers which are controlled by THRESHOLD and TILT. Rear panel BNC connector, 10k ohms input impedance.

OUTPUT CONNECTIONS

RECORDER/CRT MONITOR CONTROL: Rear Panel OUTPUT MODE switch selects appropriate horizontal, vertical, blanking, and pen lift output voltages for external CRT monitor or mechanical recorder.

HORIZONTAL SWEEP RAMP OUTPUT: 0 to 10V in synchronism with sweep display. Rear panel BNC connector.

VERTICAL OUTPUT: Varies from 0 to ±8V (1V/div.) in proportion to display trace position. When OUTPUT MODE switch is in CRT position, voltage alternates between A and B. When the switch is in RCDR position and an X−Y plot is initiated, voltage first varies in proportion to A over full swept range and then in proportion to B. Pen-lift voltage lifts recorder pen between sweeps. Rear panel BNC connector.

BLANK/PEN LIFT OUTPUT: Provides either CRT

Table 1-1. Model 560A Scalar Network Analyzer Specification Chart (continued)

blanking output or pen lift control signal, depending upon the position of the OUTPUT MODE switch. In the CRT mode, the positive TTL-compatible voltage is HIGH during retrace and LOW during forward sweep. In the RCDR mode, the pen lift relay contacts are normally-open during retrace. Lifted pen is held off paper until new sweep is started. Internal jumper is available for normally-closed contacts. Rear panel BNC connector.

ALTERNATING SWEEP INPUT/OUTPUT

AUX I/O: Provides interconnection between compatible sweep generators, such as the WILTRON 6600A Series Programmable Sweep Generator, and the 560A. Eliminates rear panel BNC connections between the compatible sweep generator and the 560A.

GPIB

DIGITAL INTERFACE: Conforms to IEEE 488 and IEC 625 standard digital interface for programmable instrumentation. Function subsets implemented: SH1, AH1, T6, TEØ, L4, LEØ, SR1, RL2, PPØ, DC1, and DTØ.

GPIB ADDRESS: TALK and LISTEN addresses selected by rear panel switches.

DATA DELIMITER: Rear panel switch selects either CARRIAGE return (CR) or CARRIAGE RETURN and LINE FEED (CR/LF) as data delimiters when in the TALK mode.

SRQ: Instrument can be programmed to generate a service request (SRQ) when data is available. If SRQ implementation is not desired, handshake will be completed when data is available.

REMOTE INDICATOR: Lights when test set is operating on GPIB.

PHYSICAL

TEMPERATURE RANGE:
Operating: 0°C to +50°C
Storage: −40°C to +70°C

POWER: 100V/120V/220V/240V +5%, −10% selectable on rear panel. 44–68 Hz, 85VA maximum.

WEIGHT:
560A Horizontal or 560A Option 2 Vertical Configuration: 11 kg (24.5 lb)
560A Option 1 Rack Mounting: 13.5 kg (30 lb)

SIZE:
560A Horizontal Configuration
133 mm H x 429 mm W x 500 mm D
(5.26 x 16.9 x 19.7 in)
560A Option 2 Vertical Configuration
267 mm H x 213 mm W x 500 mm D
(10.5 x 8.4 x 19.7 in)
560A Option 1 Rack Mount
133 mm H x 483 mm W x 500 mm D
(5.25 x 19 x 19.7 in)

RACK MOUNTING (OPTION 1): Units supplied with mounting ears and chassis track slide (90° tilt) installed.

VERTICAL CONFIGURATION (OPTION 2): Unit supplied with CRT chassis mounted atop the network analyzer chassis (Figure 1-1).

GPIB PROGRAMMABILITY (OPTION 3): Unit supplied with IEEE 488 (IEC 625) BUS (GPIB) Interface.

DC FAN (OPTION 4): Unit supplied with a DC Fan allowing 50–400 Hz operation.

1-4.2 Model 560 SWR Autotesters

The Model 560-97, -98, and -6 series SWR Autotesters are broadband, high-directivity reflection bridges with a built-in detector and a low-reflection test port. These SWR Autotesters are specifically designed to be compatible with all three channels of the 560A Scalar Network Analyzer. These 560 Model SWR Autotesters are well suited to making very accurate return loss (SWR) measurements. With their typical 6.5 dB insertion loss, these components provide a pad between the source and the device under test. Padding of the sweep generator output results in a more accurate transmission loss/gain measurement because it reduces the effect of the impedance mismatch at the source.

A listing of the Model 560-97, -98, and -6 series SWR Autotester specifications is presented in Table 1-2.

Table 1-2. SWR Autotester Specifications

MODEL	TEST PORT CONNECTOR	INPUT CONNECTOR	DIRECTIVITY	ACCURACY [1] 10 MHz to 8 GHz	ACCURACY [1] 8 GHz to 18 GHz	INPUT Z	FREQUENCY SENSITIVITY	PHYSICAL
560-97A50	GPC-7	N Female	35 dB	0.018 $\pm 0.1\rho^2$	0.018	50 Ω	±0.0 dB (max.)	Length: 7.6 cm (3 in.) Width: 5 cm (2 in.) Depth: 2.8 cm (1-1/8 in.) Weight: 425 g (15 oz.)
Option 1			40 dB	0.01 $\pm 0.06\rho^2$	0.01 $\pm 0.1\rho^2$			
560-97N50 560-97NF50	N Male Female	N Female	35 dB	0.018 $\pm 0.08\rho^2$	0.018 $\pm 0.14\rho^2$			
Option 1			38 dB	0.013 $\pm 0.06\rho^2$	0.018 $\pm 0.1\rho^2$			
				10 MHz to 18 GHz	18 GHz to 26.5 GHz			
560-98S50	Male WSMA	WSMA Female	35 dB (.01-18 GHz)	0.018 $\pm 0.1\rho^2$	0.026 $\pm 0.12\rho^2$	50 Ω	±1.0 dB	Length: 5.3 cm (2-3/32 in.) Width: 3.7 cm (1-15/32 in.) Depth: 1.2 cm (15/32 in.) Weight: 198 g (7 oz.)
560-98SF50	Female		32 dB (18-26.5 GHz)				±2.0 dB	
			38 dB (.01-18 GHz				±1.0 dB	
Option 1			35 dB (18-26.5 GHz)	0.013 $\pm 0.1\rho^2$	0.018 $\pm 0.13\rho^2$		±2.0 dB	
				10 MHz to 26.5 GHz	26.5 GHz to 40.0 GHz			
560-98K50 560-98KF50	K Male, Female	K Female	35 dB	0.018 $\pm 0.15\rho^2$	0.032 $\pm 0.15\rho^2$	50 Ω	±3.0 dB	Length: 3.8 cm (2-1/8 in.) Width: 2.9 cm (1-1/2 in.) Depth: 1.9 cm (3/4 in.) Weight: 198 g (7 oz.)
				1 MHz to 2000 MHz				
560-6N50 560-6NF50	N Male Female		40 dB	0.01 $\pm 0.06\rho^2$		50 Ω	±1.0 dB (max.)	Length: 3.8 cm (1-1/2 in.) Width: 2.9 cm (1-5/32 in.) Depth: 3 cm (1-3/16 in.) Weight: 227 g (8 oz.)
560-6N75 [2] 560-6NF50 [2]	N Male Female		40 dB	0.01 $\pm 0.06\rho^2$		75 Ω		
All Models								
Insertion Loss: 6.5 dB [3] nominal; Cable Length: 122 cm (4 ft.); Maximum Input Power: 27 dBm								

[1] Where ρ is measured reflection coefficient of test device. Accuracy includes effects of test port reflections and directivity.
[2] 75 ohm impedance.
[3] From RF input port to test port.

1-4.3 Model 560 RF Detectors

The Model 560-7 and 560-71 series RF detectors are specifically designed to be used interchangeably between Channel A, B, and R without need for adjustment. Both detector models are equipped with a specially-designed zero-bias Schottky diode that provides -55 dBm sensitivity. In the 560-7 series detectors, this diode is encased in a field-replaceable module; in the 560-71 series detectors this diode is a discrete component, and is also field replaceable. The 560-7K50 is not field replaceable.

A listing of the 560-7 and 560-71 series RF detector specifications is provided in Table 1-3.

Table 1-3. RF Detector Specifications

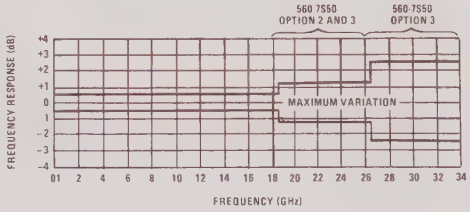
Model 560-	Input Connector	Input Z	Frequency
7A50	GPC-7	50Ω	10 MHz to 18.5 GHz
7N50	Type N Male	50Ω	10 MHz to 18.5 GHz
7S50 Option 1	WSMA Male	50Ω	10 MHz to 18.5 GHz
7S50 Option 2	WSMA Male	50Ω	10 MHz to 26.5 GHz
7S50 Option 3	WSMA Male	50Ω	10 MHz to 34.0 GHz
7K50	K Male	50Ω	10 MHz to 40.0 GHz
71N50	Type N Male	50Ω	1.0 MHz to 2.0 GHz
71N75	Type N Male	75Ω	1.0 MHz to 2.0 GHz

All Models

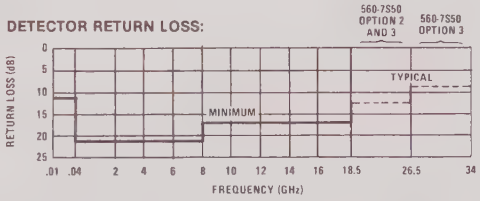
Maximum Input Power: 20 dBm (100 mW)
Cable Length: 122 cm (4 ft.)
Dimensions: 7.6 x 2.9 x 2.2 cm (3 x 1-1/8 x 7/8 in.)
Weight: 170 grams (6 oz.)

560-7 Series

FREQUENCY RESPONSE:

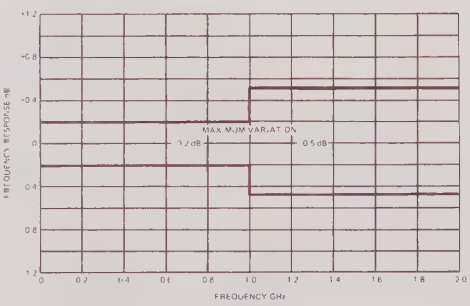


DETECTOR RETURN LOSS:

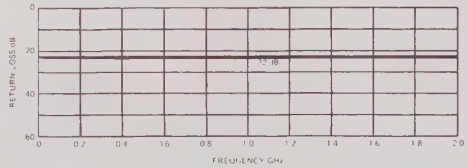


560-71 Series

FREQUENCY RESPONSE:

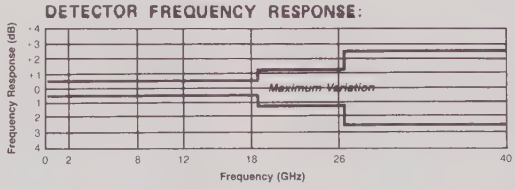


DETECTOR RETURN LOSS:

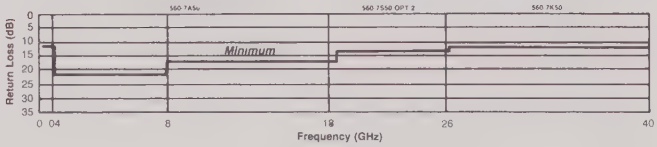


560-7K Series

DETECTOR FREQUENCY RESPONSE:



DETECTOR RETURN LOSS:



1-5 ACCESSORIES

Table 1-4 lists accessories used with the 560A Scalar Network Analyzer.

Table 1-4. Listing of Accessories

EXTENDER CABLES:

DESCRIPTION: Extender cables may be installed between SWR Autotesters or Detectors and the 560A, permitting measurements from up to 200 feet distance.

CABLE LENGTH	MODEL
7.6 m (25 ft)	800-109
15.2 m (50 ft)	800-110
30.5 m (100 ft)	800-111
61 m (200 ft)	800-112

GPIB CABLES:

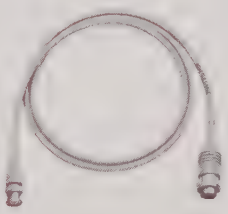
DESCRIPTION: GPIB cables interconnect instruments on GPIB.

CABLE LENGTH	MODEL
1 m (3.3 ft)	2100-1
2 m (6.6 ft)	2100-2
4 m (13.2 ft)	2100-4
0.5 m (1.6 ft)	2100-5

OPEN/SHORT:

DESCRIPTION: Open/short with connectors to match the test port of the selected SWR Autotester.

MODEL	CONNECTOR
22A	APC-7
22N	Type N Male
22NF	Type N Female
22S	WSMA Male
22SF	WSMA Female



10BX and 10BX-1 CABLES:

The 10BX and 10BX-1 cables enable SWR Autotesters and RF detectors other than the 560 series components to be used with the Model 560A Scalar Network Analyzer. The 10BX cable is used with Si detectors, and the 10BX-1 cable is used with GaAs detectors.

Cable Length — 122 cm (4 ft.)

9-TO-25-PIN ADAPTER CABLE:

Provides interconnection between the 560A and the 6600A series sweep generators. P/N 560A-B-11359-1.

1-6 DESCRIPTION OF THE INTERFACE BUS

The IEEE 488 bus (General Purpose Interface Bus--GPIB) is an instrumentation interface for integrating instruments, calculators, and computers into systems. The bus uses sixteen signal lines to effect transfer of data and commands to as many as fifteen instruments. The instruments on the bus are connected in parallel, as shown in Figure 1-4. Eight of the signal lines (DIO 1 thru DIO 8) are used for the transfer of data and other messages in a byte-serial, bit-parallel form. The remaining eight lines are used for communications timing (handshake), control, and status information. Data is transmitted on the eight GPIB data lines as a series of eight-bit characters referred to as bytes. Normally, a seven-bit ASCII (American Standard Code for Information Interchange) code is used. The eighth (parity) bit is not used. Data is transferred by means of an interlocked handshake technique. This sequence permits asynchronous communications over a wide range of data rates. The following paragraphs provide an overview of the data, management, and handshake buses and describe how these buses interface with the network analyzer.

1-6.1 Data Bus Description

The data bus contains eight bi-directional active-low signal lines, DIO 1 thru DIO 8. One byte of information (eight bits) is transferred over the bus at a time. DIO 1 represents the least-significant bit (LSB) in the byte; DIO 8 represents the most-significant bit (MSB) in the byte. Each byte represents a peripheral address (either primary or secondary), a control word, or a data byte. Data bytes are usually formatted in ASCII code, without parity. The data bus provides the conduit for transmitting control information and data between the controller and the instrument (network analyzer).

1-6.2 Management Bus Description

The management bus is a group of five signal lines that are used to control the operation of the bus system. Functional information regarding the individual management bus control lines is provided below.

a. ATN (attention). When this line is true, the 560A will respond to appropriate interface messages (e.g., device clear and serial poll) and to its own listen/talk address.

b. EOI (end or identify). This line is set true during the last byte of a multi-byte message. This line is also used in conjunction with ATN to indicate a parallel-poll.

c. IFC (interface clear). When this line is true, the 560A interface functions are placed in a known state, i.e., unaddressed to talk, unaddressed to listen, and service request idle.

d. REN (remote enable). When this line is true, the 560A is enabled for entrance into the remote state (i.e., certain front panel functions disabled) upon receipt of its listen address. The remote state is exited when either: (1) the REN line is false (high), (2) the go-to-local (GTL) message is received, or (3) the 560A programming command RL (return to local) is received.

e. SRQ (service request). If programmed for interrupt mode (IM) operation (refer to paragraph 3-7.1, d, 2), the 560A will set this line true to indicate that it requires service.

1-6.3 Data Byte Transfer Control (Handshake) Bus Description

Information is transferred on the data lines under control of a technique called the three-wire handshake. The three handshake bus signal lines are described below; Figure 1-5 shows a typical interlocking handshake operation.

a. DAV (data valid). This line is set true (arrow 1) when the talker has (1)sensed that NRFD is false, (2) placed a byte of data on the bus, and (3) waited an appropriate length of time for the data to settle.

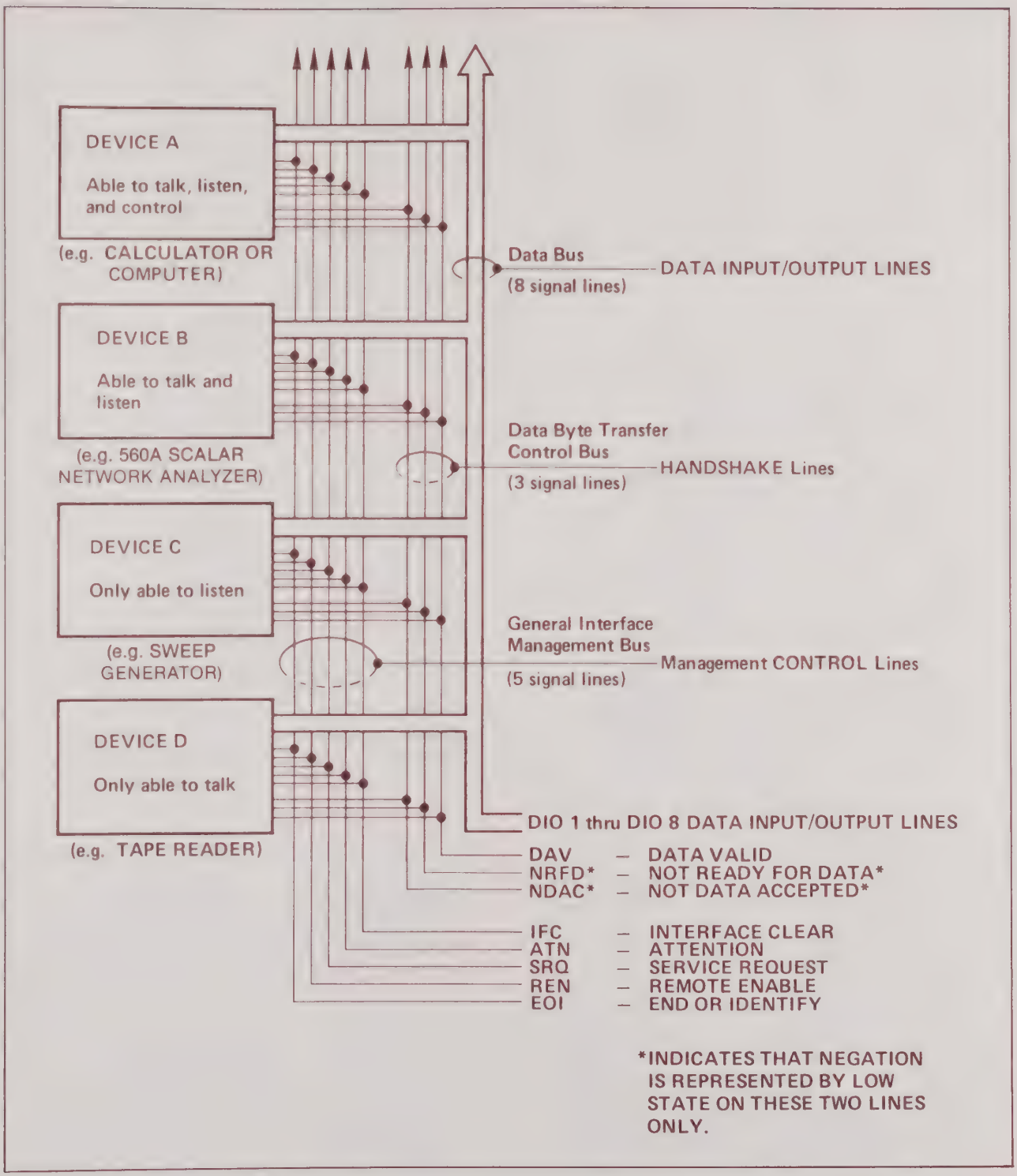

DEVICE A
Able to talk, listen, and control
(e.g. CALCULATOR OR COMPUTER)
DEVICE B
Able to talk and listen
(e.g. 560A SCALAR NETWORK ANALYZER)
DEVICE C
Only able to listen
(e.g. SWEEP GENERATOR)
DEVICE D
Only able to talk
(e.g. TAPE READER)
Data Bus
(8 signal lines)
DATA INPUT/OUTPUT LINES
Data Byte Transfer Control Bus
(3 signal lines)
HANDSHAKE Lines
General Interface Management Bus
(5 signal lines)
Management CONTROL Lines
DIO 1 thru DIO 8 DATA INPUT/OUTPUT LINES
DAV – DATA VALID
NRFD* – NOT READY FOR DATA*
NDAC* – NOT DATA ACCEPTED*
IFC – INTERFACE CLEAR
ATN – ATTENTION
SRQ – SERVICE REQUEST
REN – REMOTE ENABLE
EOI – END OR IDENTIFY
*INDICATES THAT NEGATION IS REPRESENTED BY LOW STATE ON THESE TWO LINES ONLY.

Figure 1-4. Interface Connections and Bus Structure

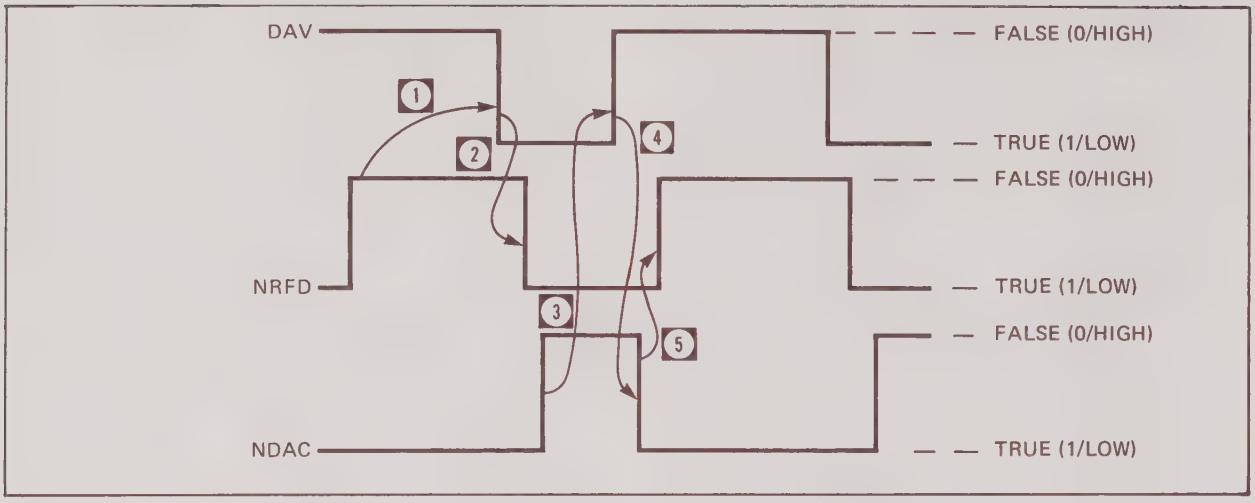


Figure 1-5. Typical Handshake Operation

b. NRFD (not ready for data). This line is set true (arrow 2) by a listener to indicate that valid data has not yet been accepted. The time between the events shown by arrows 1 and 2 is variable and depends upon the speed with which a listener can accept the information.

c. NDAC (not data accepted). This line is set false by a listener when the listener has accepted the current data byte for internal processing. When the data byte has been accepted, the listener releases its hold on NDAC and allows the line to go false. However, because the GPIB is constructed in a wired-OR configuration, this line will not go false until all listeners participating in the interchange have also released the line. As shown by the arrow labeled 3, when the NDAC line goes false the DAV line follows suit a short time later. The false state of the DAV line indicates to the bus that valid data has been removed; consequently, with valid data no longer on the line, the NDAC line is pulled low again in preparation for the next data interchange. This action is shown by the arrow labeled 4.

The next action that occurs is shown by arrow 5. This arrow shows NRFD going false following NDAC returning to its true state. The false state on NRFD indicates to the bus that all listeners are ready for the next information interchange. The time period between these last two events (NDAC going true and NRFD going false) is variable and is dependent upon the length of time that it takes a listener to process the data byte. Therefore, the result of the wired-OR construction of the handshake bus is that a talker is forced to wait for the slowest instrument to accept the current data before it can place a new byte of information on the bus.

1-7 RF DETECTOR-DIODE REPLACEMENT

Field replacement of the detector diode is possible with both the 560-6 series SWR Autotesters, and the 560-7 and 560-71 series RF detectors. In the 560-7 series detectors, the diode is encased in a module; WILTRON part numbers are 560-7219A (0. to 18.5 GHz), -7219B (0.01 to 26.5 GHz), and -7219C (0.01 to 34.0 GHz). In both the 560-6 series SWR Autotesters and the 560-71 series RF detectors, the diodes are discrete components. For the SWR Autotesters, the diode part number is 10-9; for the detectors, the diode part number is 10-21. Parts ordering information is contained in Section VI, Parts Lists, and replacement instructions are contained in Section VII, Service.

1-8 PRECAUTIONS

The 560-98 Series SWR Autotesters and 560-7 Series RF detectors are high-quality, precision, laboratory instruments and should receive the same care and respect afforded other such instruments. Complying with the following precautionary notes will guarantee longer component life and less equipment downtime due to connector or component failure. Also, such compliance will ensure that failures on these components are not due to misuse or abuse, two failure causes not covered under WILTRON warranty.

a. Beware of Destructive Pin depths on Mating Connectors.* Measure the pin depth (Figure 1-6) of the test device connector before mating it with the detector or SWR Autotester test port connector. When any detector or SWR Autotester connector is mated with a connector having a destructive pin depth, the detector or SWR Autotester connector will probably be damaged. (A destructive pin depth has a center pin that is too long in respect to the connector's reference plane.)

The center pin on all of the detector and SWR Autotester connectors has a precision tolerance measured in mils (1/1000 inch). Connectors on test devices that mate with the detector connector and the SWR Autotester test port connector, however, may not have the proper pin depth. These connectors must be measured before mating to ensure suitability. Gauging sets for measuring pin depth are available (Section IV).

When gauging pin depth, if the test device connector measures out of tolerance (Table 1-5) in the "+" region (Figure 1-7), the center pin is too long. Mating under this condition will probably damage the detector or SWR Autotester connector. On the other hand, if the test device connector measures out of tolerance in the "-" region, the center pin is too short. A mating, while not causing any damage, will result in a poor connection and will degrade the quality of the measurement.

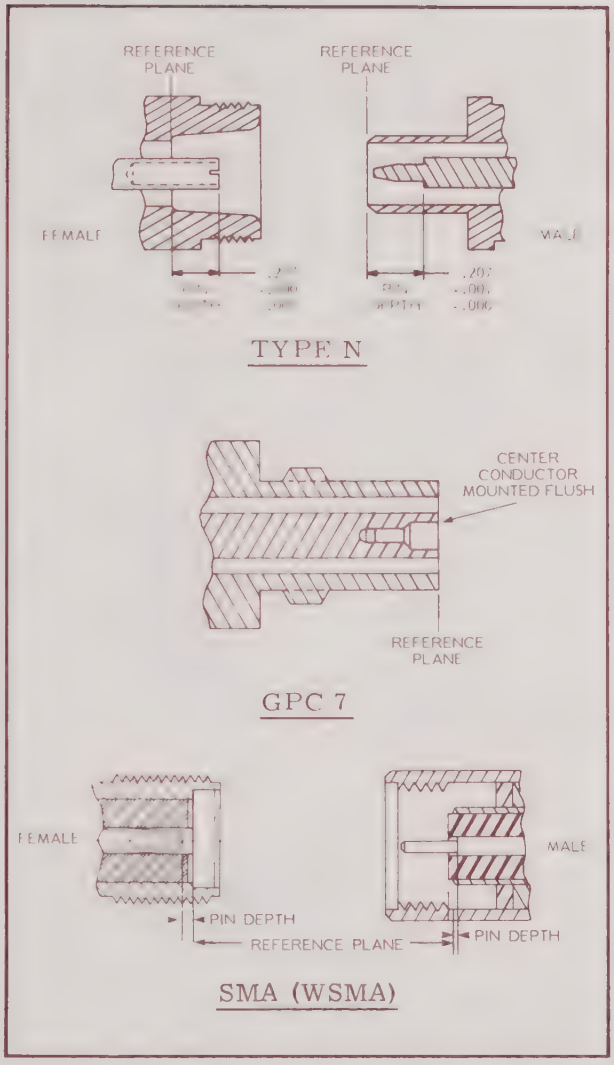


Figure 1-6. Connector Pin Depth

*The term "pin" is used in a generic sense. It refers to both the center conductor pins on type N and SMA (WSMA) male connectors and the center conductor sleeves on type N, GPC 7, and SMA (WSMA) female connectors.

Table 1-5. Pin Depth Tolerances for 560 Detectors and SWR Autotesters

SERIES	PORT/CONNECTOR TYPE	PIN DEPTH (Mils)	MMC GAUGE READING[1]
560-98 SWR Autotesters	TEST-A	+0.000 -0.003	Same as Pin Depth
	TEST-N	207 -0.000 +0.002	210 -0.003 +0.001
	TEST-NF	207 +0.000 -0.002	Same as Pin Depth
	TEST-S[2]	-0.0025 -0.0035	
	TEST-SF[2]	-0.0003 -0.0007	
	INPUT-RS	-0.0003 -0.0007	
560-7 RF Detectors	INPUT-N	207 -0.000 +0.006	210 -0.003 +0.003
	INPUT-A	+0.000 -0.003	Same as Pin Depth
	INPUT-S	-0.001 +0.004	

LEGEND AND NOTES

Typical Model Number:

560-98 SF 50

- 50 — Impedance
- SF — Connector Type (Test Port Connector on Bridges and SWR Autotesters)
- 560-98 — Series Number

Connector-Type Abbreviations:

N = Type N male
NF = Type N female
A = GPC7
S = WSMA male
SF = WSMA female

[1]MMC is Maury Microwave Corp.
[2]SMA connectors that mate with WSMA connectors should have the same pin depth tolerance.

may damage the connector center pin or may cause the connector body to turn in its housing. Finger-tight is usually sufficient, especially on type N and GPC 7 connectors. Should it be necessary to use a wrench to tighten SMA or WSMA connectors, however, use a torque wrench that breaks at 8 inch-pounds. As a general rule, NEVER USE PLIERS TO TIGHTEN CONNECTORS.

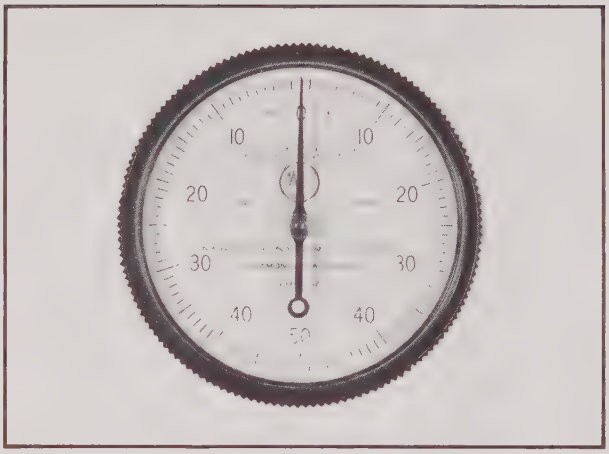


Figure 1-7. Pin-Depth Guage

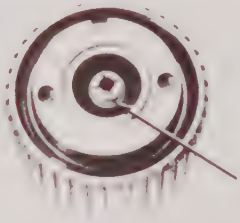
c. Avoid Applying Excessive Power. The 560-98 series SWR Autotesters are rated at +27 dBm (0.5 watts) and the 560-7 series RF Detectors at +20 dBm (100 mW) maximum input power. Applying power levels beyond these values, for even short durations, can seriously damage the instruments' internal components.

d. Do Not Disturb Teflon Tuning Washers on Connector Center Pins. The center conductor on most 560 SWR Autotester test port connectors contains a small teflon tuning washer located near the point of mating (interface). This washer (Figure 1-8) compensates for minor impedance discontinuities at the interface. The washer's location is critical to the SWR Autotester performance, DO NOT DISTURB.

When making field repairs of WSMA test port connectors, however, discard the washer. Although discarding this washer may degrade the original return loss specification by 3 to 4 dB, the return loss will be better than if the washer is incorrectly placed. If the degradation to return loss is unacceptable, the SWR Autotester should be returned to WILTRON for alignment.

e. Avoid Mechanical Shock. The 560 detectors and SWR Autotesters are designed to withstand years of normal bench handling.

point of mating (interface). This washer (Figure 1-8) compensates for minor impedance discontinuities at the interface. The washer's location is critical to the SWR Autotester performance, DO NOT DISTURB.



NOTE

The washer shown is on a GPC 7 connector. A similar washer is installed on almost all WILTRON precision components.

Figure 1-8. Teflon Tuning Washer on GPC 7 Connector

When making field repairs of WSMA test port connectors, however, discard the washer. Although discarding this washer may degrade the original return loss specification by 3 to 4 dB, the return loss will be better than if the washer is incorrectly placed. If the degradation to return loss is unacceptable, the SWR Autotester should be returned to WILTRON for alignment.

e. Avoid Mechanical Shock. The 560 detectors and SWR autotester are designed to withstand years of normal bench handling.

Do not drop or otherwise roughly handle them, however. They are laboratory-quality instruments. The detectors and SWR Autotesters are shipped from the factory in sturdy, foam-rubber padding. These boxes should be used for storage when the components are not in use.

f. Keep Component Connectors Clean. The precise geometry that makes possible the detector's and SWR Autotester's high performance can be easily disturbed by dirt and other contamination adhering to connector interfaces. When not in use, keep the component connectors covered. Refer to paragraph 7-5.8 for cleaning instructions.

g. Avoid Touching the Outer Conductor (Coupling Nut) on the RF Detector or SWR Autotester to a ±Voltage Greater Than 4 Volts. This coupling nut, via the shield lead on the A, B, or R connector, connects to two back-to-back 3.3V Zener diodes on the A3 Log Amp PCB. Voltages larger than 4 volts may destroy the diodes and cause damage to the surrounding circuitry.

SECTION II
INSTALLATION

2-1 INTRODUCTION

This section provides information on initial inspection, preparation for use, and General Purpose Interface Bus (GPIB) interconnections. Also included is information concerning reshipment and storage of the network analyzer and its dedicated microwave components.

2-2 INITIAL INSPECTION

Inspect the shipping container for damage. If the container or cushioning material is damaged, retain it until the contents of the shipment have been checked against the packing list, and the instrument has been checked for mechanical and electrical operation.

If the 560A is damaged mechanically, notify your local sales representative or WILTRON Customer Service. If either the shipping container is damaged or the cushioning material shows signs of stress, notify the carrier as well as WILTRON. Keep the shipping materials for carrier's inspection.

2-3 PREPARATION FOR USE

Preparing the Model 560A Scalar Network Analyzer for use consists of three operations. These three operations - selecting the operating voltage, interconnecting the 560A with a sweep generator, and normalizing the input horizontal sweep voltages - are described in the following paragraphs.

2-3.1 Selection of Operating Voltage

The Model 560A comes equipped with a voltage selector module that enables the network analyzer to be used with any of four international line voltages: 100, 115/120, 220, and 230/240 Vac. Each 560A is preset and tagged at the factory for the line voltage used in the customer's country. If the line voltage in the user's area is the same as that stated on the tag, the user can proceed to paragraph 2-3.2. If, however, the line voltage is different from that stated on the tag, the user can reconfigure the voltage selector module (Figure 2-1) using the following procedure.

a. Disconnect the power cord from the voltage selector module (1) and slide the cover (2) to the left to gain access to the fuse compartment.

b. Pull forward on FUSE PULL (3) and remove line fuse (4).

c. To select operating voltage:

1. Pull FUSE PULL to left and remove PC board.

NOTE

The PC board is tightly secured within the module housing. It may be necessary to use needle-nose pliers or a similar tool as a pry.

2. Orient PC board so that the desired voltage is facing up and on the left side of the board.

3. With desired voltage facing up, reinstall PC board into its slot. Press firmly to seat the board.

4. Push FUSE PULL back to its normal position and insert a fuse of the proper value (as indicated on the bottom of the module) into the fuse holder.

2-3.2 Sweep Generator Interconnection

The Model 560A Scalar Network Analyzer requires input from a microwave sweep

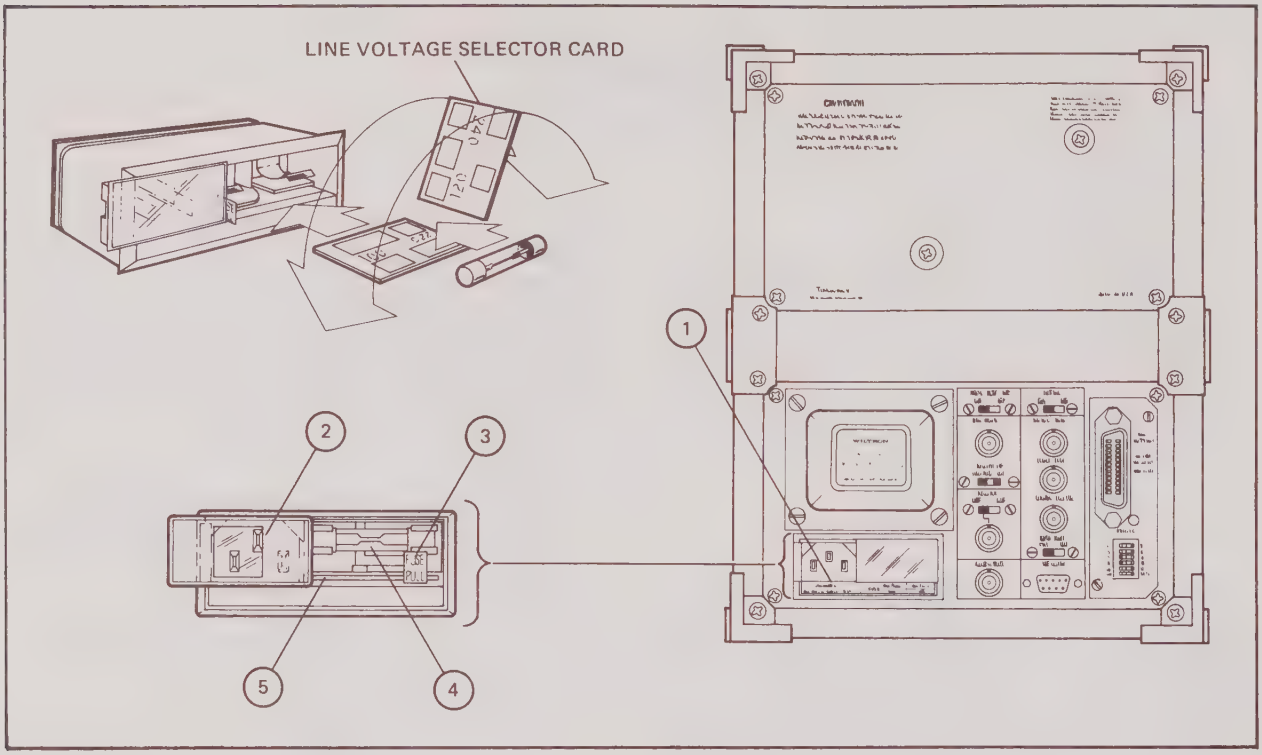


Figure 2-1. Line Voltage Selector Module

generator. Although the 560A was designed to operate with the WILTRON 6600/6600A Series Programmable Sweep Generator, it is compatible with most other sweep generators. A plate is attached to the 560A rear panel. This plate lists the interconnections between the sweep generator and the 560A, and the rear-panel switch settings. The only requirement is that the sweep generator be able to supply the required horizontal sweep ramp, retrace blanking, and marker voltages. These voltages are specified in Table 1-1, Model 560A Scalar Network Analyzer Specification Chart. Figure 2-2 shows the interconnections between the 560A and the WILTRON 6600A Series Programmable Sweep Generators.

NOTE

The rear panel HORIZONTAL SELECT switch must be set to the position that corresponds to the particular horizontal input ramp: 0 to +10V, 0 to +15V, or -8V to +8V.

2-3.3 Horizontal Sweep Ramp Normalization

Normalization of the horizontal sweep ramp sets the input ramp voltage to start at 0 volts and to stop at 10 volts. Normalization is necessary to make the analog real time ramp "fit" the digital storage and refresh memory circuits. The two front panel screwdriver potentiometers labeled HORIZ-START and -STOP are the normalization adjustments. The START potentiometer, in conjunction with an internal clamping circuit, adjusts the ramp to start at 0 volts; the STOP potentiometer, also in conjunction with an internal clamping circuit, adjusts the ramp to stop at 10 volts. If the START potentiometer is misadjusted, horizontal and vertical data at the low end of the frequency band will be lost; if the STOP potentiometer is misadjusted, horizontal and vertical data at the high end of the frequency band will be lost. Adjust the START and STOP potentiometers as follows:

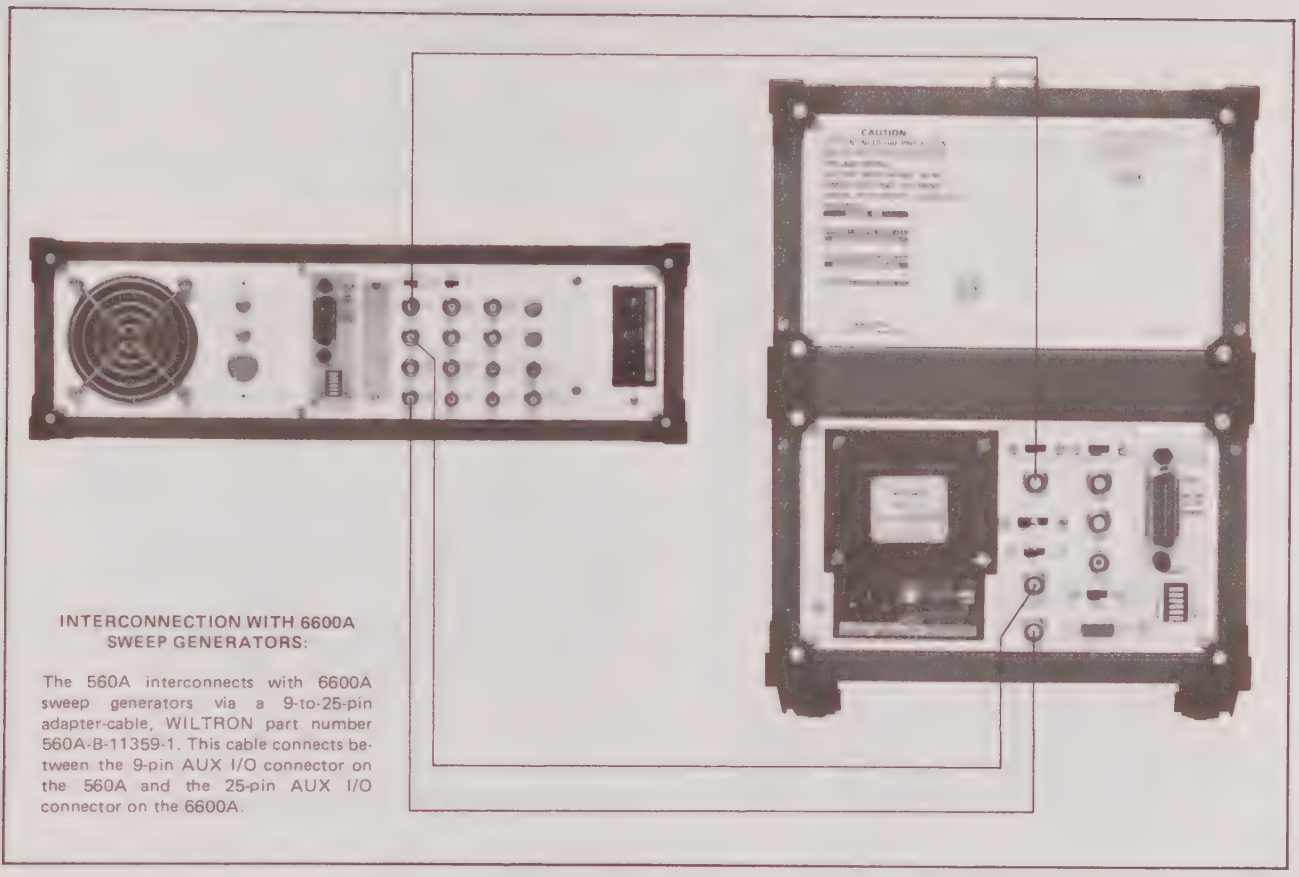

INTERCONNECTION WITH 6600A SWEEP GENERATORS:
The 560A interconnects with 6600A sweep generators via a 9-to-25-pin adapter-cable, WILTRON part number 560A-B-11359-1. This cable connects between the 9-pin AUX I/O connector on the 560A and the 25-pin AUX I/O connector on the 6600A.

Figure 2-2. Interconnections between WILTRON 6600A Series Programmable Sweep Generator and Model 560A Scalar Network Analyzer

a. Interconnect the 560A with a sweep generator (paragraph 2-3.2) and adjust the sweep generator controls to provide a 50 ms (approximate) sweep.

b. Turn on the 560A by depressing POWER pushbutton switch. Power ON indicator should light.

c. Turn on Channel A by depressing CHANNEL A ON pushbutton switch. The Channel A OFFSET dB display and either the dB or dBm indicator should light.

d. Insure Channel B is off by observing that the CHANNEL B ON pushbutton switch is not depressed and that none of the Channel B indicators are lit.

e. Place the 560A in real time display mode by depressing REAL TIME pushbutton switch.

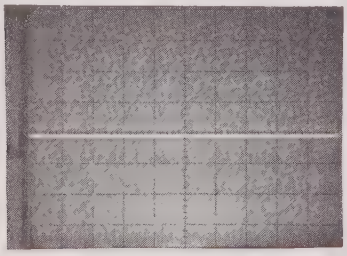
f. Locate horizontal trace by depressing and holding the REF POS LOCATE pushbutton switch. Position trace on center graticule line by adjusting SET screwdriver potentiometer.

g. Adjust START and STOP potentiometers as follows:

1. With REF POS LOCATE depressed, observe CRT and rotate START potentiometer clockwise until left trace-end dot begins to move right; then stop.

2. Rotate START potentiometer counter-clockwise until trace-end stops moving left and dot begins to intensify; stop counter-clockwise rotation. Left trace movement should stop on or within 1 minor division from left-hand graticule edge. If trace-end dot movement is not as described, refer to Table 3-5.

3. Rotate STOP potentiometer clockwise until trace-end stops moving right. Right trace movement should stop on or within 1 minor division from right graticule edge. If trace-end dot movement is not as described, refer to Table 3-5. An example of a properly aligned trace is shown below.



4. Release REF POS LOCATE.

2-4 GPIB SETUP AND INTER CONNECTION

With Option 3 installed (the option can be installed in the field), the Model 560A Scalar Network Analyzer is capable of providing automated microwave measurements via the GPIB. Specific GPIB information — including interface connections, cable requirements, and addressing instructions — is contained in the following paragraphs.

2-4.1 GPIB PCB Installation

To install the GPIB PCB, proceed as follows:

a. Gain access to the 560A printed circuit boards (PCBs), as described in paragraph 5-2.

b. Using the 4-40 kit hardware, secure the A6 PCB (Part No. 560-D-7006-3) to the 560A mounting plate, as shown in Figure 5-3.

c. On the 560A rear panel, remove the plate covering the Option 3 mounting hole. This plate is shown in Figure 2-4.

d. Using the 6-32 kit hardware, secure the A7 PCB (Part No. 560-B-7007) into the Option 3 mounting hole on the 560A rear panel.

e. Orient the connector on the red flatwire harness so that the arrowhead (▽) is aligned with pin 1 on A6P1 (Figure 2-3). Connect the two connectors together.

f. Connect the multicolored flatwire harness (Part No. 802-18C-6.0) between P2 of the A6 PCB and J1 on the Digital (A2) PCB. Connector A2J1 is shown in Figure 7-55.

2-4.2 Interface Con..ctor

Interface between the Model 560A and other devices on the GPIB is via a 24-wire interface cable. The interface cable is specially constructed with each end containing a connector shell with two connector faces. These double-faced connectors allow for the parallel connection of two or more cables to a single device. Figure 2-3 shows the pin assignments for the Type 57 connector installed on the 560A rear panel. Table 1-4, Accessories, contains leading particulars on the WILTRON cable assemblies. The WILTRON cables may be ordered by special request. Refer to Section VI for parts-ordering information.

2-4.3 Cable-Length Restrictions

The GPIB system can accommodate up to fifteer instruments at any one time. To achieve design performance on the bus, the proper timing and voltage-level relationships must be maintained. If either the cable length between separate instruments or the accumulated cable length between all

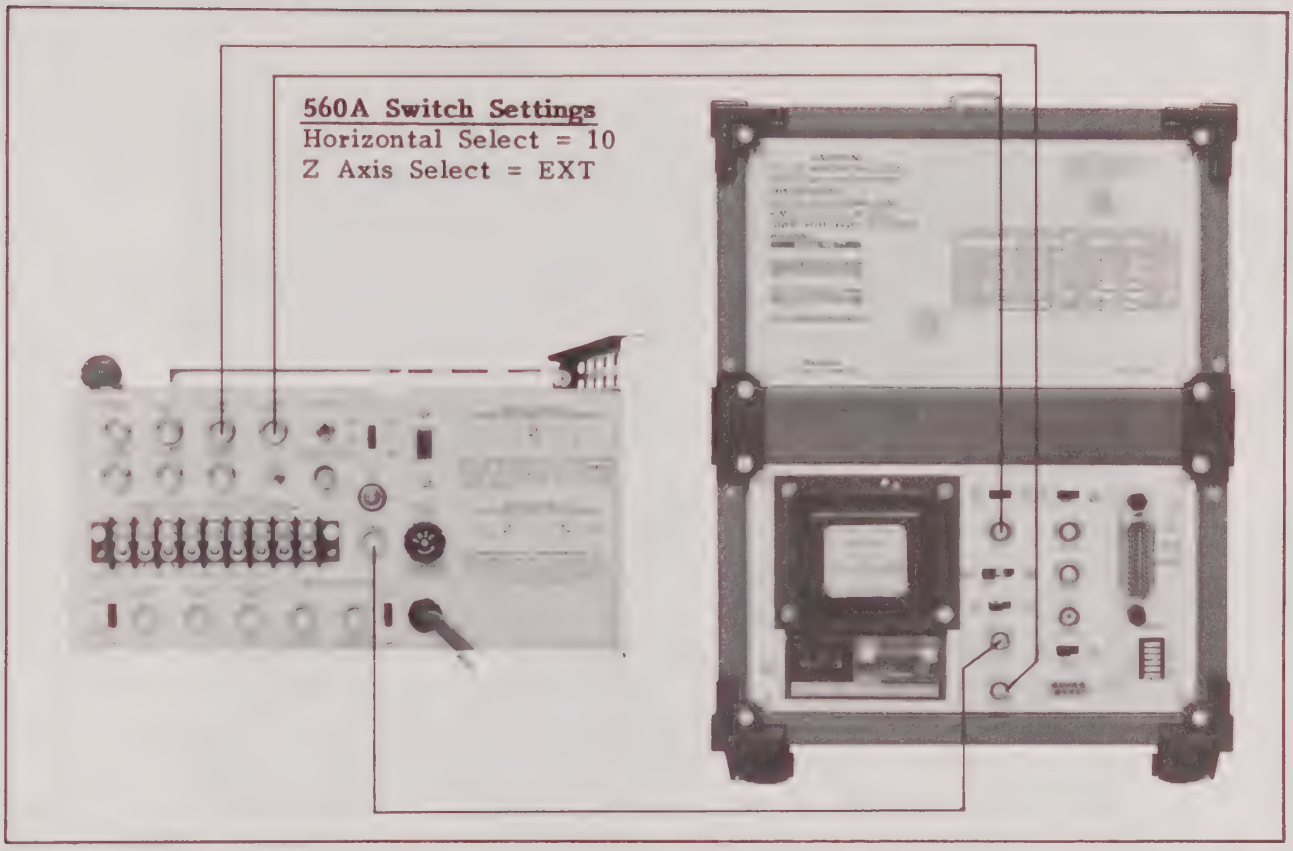
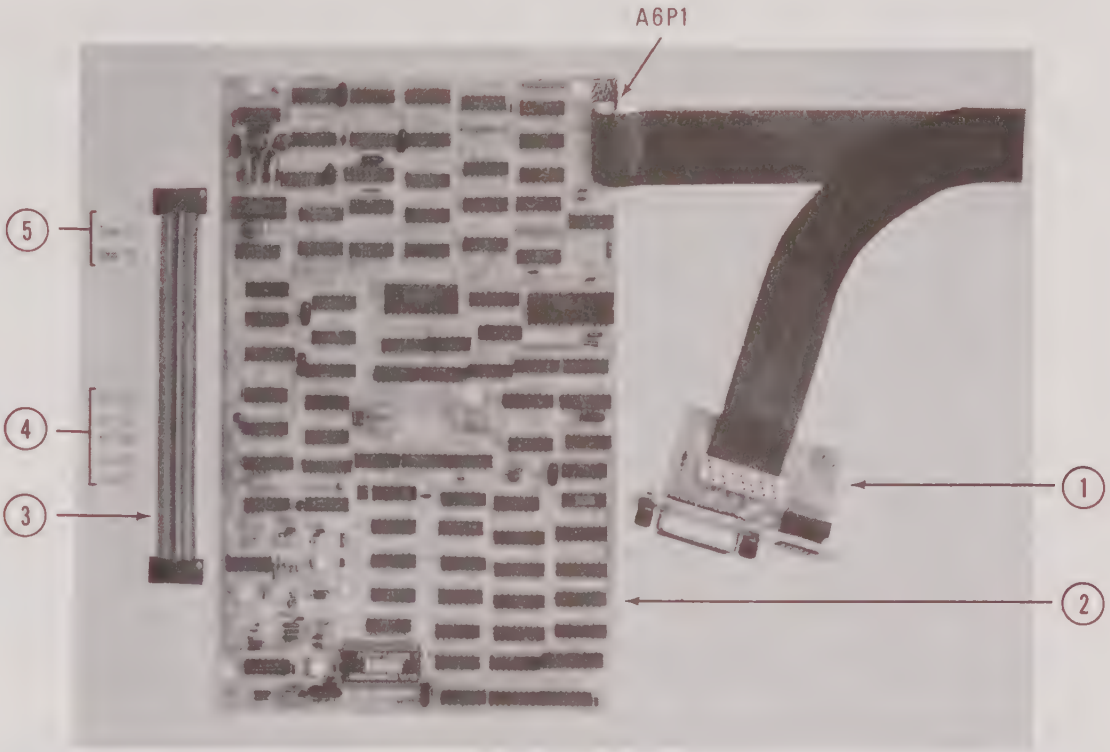


Figure 2-2A. Interconnections between WILTRON 610D Sweep Generator and Model 560A Scalar Network Analyzer.



Item No.	Description	WILTRON Part No.
1	GPIB Interconnect (A7) Printed Circuit Board	560-B-7005
2	GPIB Interface (A6) Printed Circuit Board	560-D-7006-3
3	Cable Assembly, GPIB Interface (A6) to Digital (A2) Printed Circuit Board	802-18C-6.0
4	Screws, 4-40 x 3/8-inch (5 each) Flatwashers, #4 (5 each)	900-141 900-346
5	Screws, 6-32 x 5/16-inch (2 each) Split Washers, #6 (2 each)	900-68 900-392
	Clips, Cable	553-118

Figure 2-3. Model 560A Scalar Network Analyzer, Option 3 Retrofit Kit

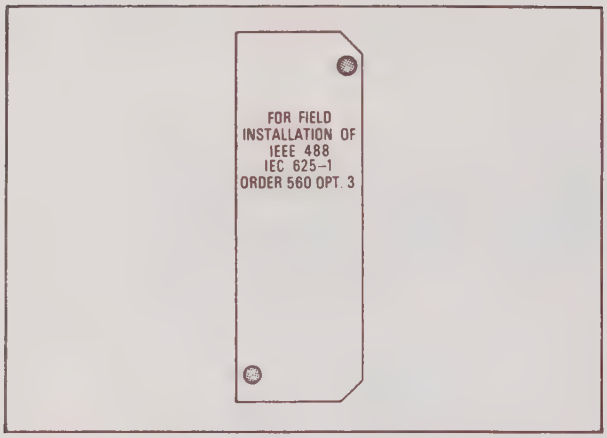


Figure 2-4. Option 3 Cover Plate on Model 560A Rear Panel

instruments is too long, the data and control lines cannot be driven properly and the system may fail to perform. Cable length restrictions are as follows:

- No more than 15 instruments may be installed on bus.
- Total accumulative cable length may not exceed 2 times the number of bus instruments in meters or 20 meters, whichever is less.

2-4.4 Interconnecting the Model 560A on the GPIB

The Model 560A is interconnected with a suitable sweep generator and GPIB system controller. Interconnection with other peripheral equipment, e.g. an X-Y plotter, is via the controller. GPIB interconnection is accomplished as follows:

a. Interconnection with Sweep Generator. To connect the Model 560A to the sweep generator, refer to paragraph 2-3.2.

b. Interconnection with Controller. To connect the Model 560A with the GPIB controller, connect a 1-, 2-, or 4-meter (as required) GPIB interconnect cable between the Option 3 interface connector on the 560A rear panel (Figure 2-5) and a like connector on the controller (refer to controller instruction manual to locate this connector).

NOTE

Since the GPIB is of parallel construction, the interconnect cable from the 560A

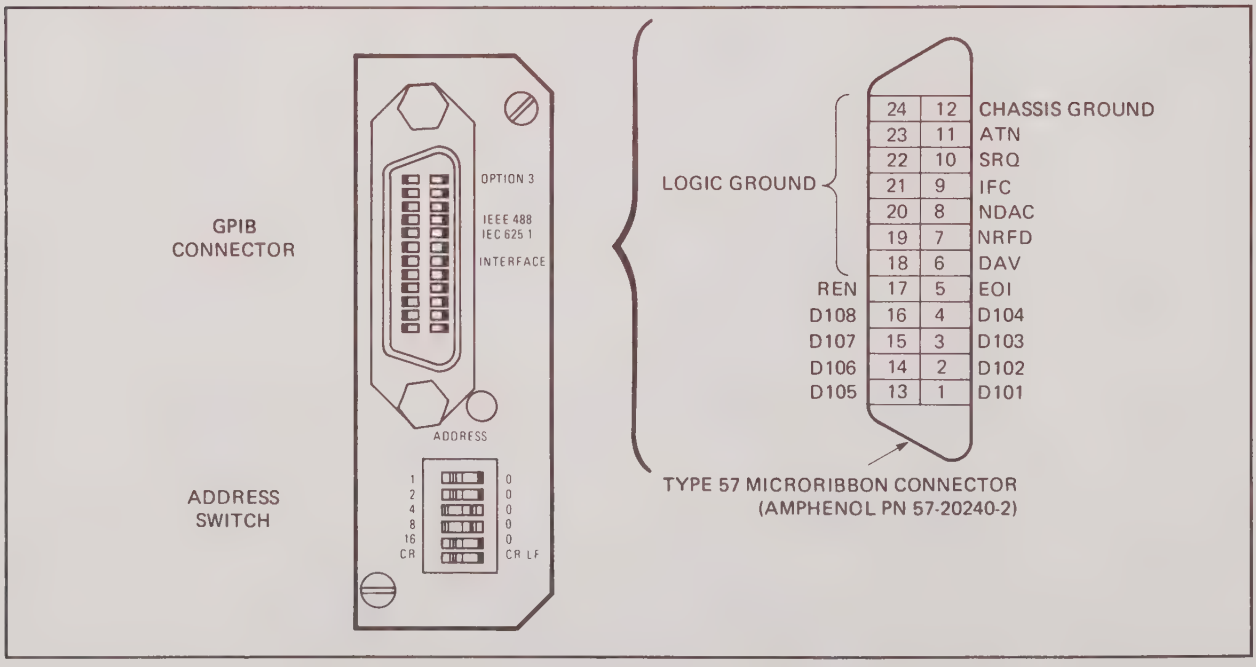


Figure 2-5. Option 3 Panel (Address Switch and GPIB Connector)

can also connect to the open face on any other bus instrument's interface connector cable.

2-4.5 Addressing the Model 560A

Addressing the Model 560A to talk and listen is accomplished from the rear panel. The Option 3 panel (Figure 2-5), located on the rear of the Model 560A, contains a vertical row of six white ON/OFF rocker-type switches. The top five switches are used to assign the talk/listen address (talk and listen addresses use the same address number); the bottom switch is used for data delimiting (paragraph 2-4.6).

The five Option 3 address switches are arranged from top to bottom in a binary format, the least significant bit (LSB) located at the top. As shown in Figure 2-5, there are two sets of numbers assigned to switches within the ADDRESS switch row.

The numbers 1, 2, 4, 8, and 16, left and 0, right, represent binary weights; i.e., when a switch's rocker arm is depressed in the direction of the number, the number represents the binary weight of the switch. To determine the talk/listen address that has been assigned, note the positions of the switch rocker arms and add, in decimal addition, the binary weights. The sum of that addition is the talk/listen address that the Model 560A responds to. For example, assume that the first, third, and fifth switches, from top to bottom, have been depressed to the left. The decimal sum of the weighted digits 1, 4, and 16 is 21--the talk/listen address.

When assigning a talk/listen address, any number from 0 to 30 may be used. However, no two GPIB instruments can share the same address number. The tabulation in Figure 2-6 shows the available decimal address numbers, the ASCII character assigned to each number, and the binary

		(MSB)				(LSB)
Decimal Address	ASCII Character	16	8	4	2	1
0	Space	0	0	0	0	0
1	!	0	0	0	0	1
2	"	0	0	0	1	0
3	#	0	0	0	1	1
4	$	0	0	1	0	0
5	%	0	0	1	0	1
6	&	0	0	1	1	0
7	'	0	0	1	1	1
8	(	0	1	0	0	0
9	)	0	1	0	0	1
10	*	0	1	0	1	0
11	+	0	1	0	1	1
12	,	0	1	1	0	0
13	-	0	1	1	0	1
14	.	0	1	1	1	0
15	/	0	1	1	1	1

		(MSB)				(LSB)
Decimal Address	ASCII Character	16	8	4	2	1
16	0	1	0	0	0	0
17	1	1	0	0	0	1
18	2	1	0	0	1	0
19	3	1	0	0	1	1
20	4	1	0	1	0	0
21	5	1	0	1	0	1
22	6	1	0	1	1	0
23	7	1	0	1	1	1
24	8	1	1	0	0	0
25	9	1	1	0	0	1
26	:	1	1	0	1	0
27	;	1	1	0	1	1
28	<	1	1	1	0	0
29	=	1	1	1	0	1
30	>	1	1	1	1	0

Switch ON = 1
Switch OFF = 0

Figure 2-6. Available Address Codes and Corresponding Address Switch Positions

arrangement of 1's and 0's to which the number is equivalent. Keep in mind that the most significant bit (MSB) is the left-most digit. This is the binary position that corresponds to the fifth-from-the-top switch on the Option 3 panel. The 560A is shipped from the factory with address switches set to 6.

2-4.6 Data Delimiting (CR-CR/LF Switch)

As described in the preceding paragraph, the bottom switch on the Option 3 panel is used for data delimiting. Data delimiting, as it applies to the GPIB, is the method by which a talker signals to the controller that data or control transmission has finished.

Two ASCII characters are used for the data-delimiting function. These characters are: carriage return (CR) and line feed (LF). The position of the CR-CR/LF switch determines which character or combination of characters is sent over the bus by the Model 560A. Some controllers want CR, some controllers want both CR and LF, and other controllers do not care. For example, the Commodore PET 2001 controller wants CR only, the Hewlett-Packard 9825A and 85 want both CR and LR (CR/LF), and the Tektronix 4051 will accept either CR or CR/LF.

2-5 PREPARATION FOR STORAGE AND/OR SHIPMENT

2-5.1 Preparation for Storage

Preparation for storage involves cleaning the unit, packing the inside of the unit with moisture-absorbing dessicant crystals, and storing the unit in a proper environment. Environmental storage conditions for the Model 560A are listed in Table 1-1.

2-5.2 Preparation for Shipment

To provide maximum protection against damage in transit, the Model 560A should be repackaged in the original shipping container. If this container is no longer available and the 560A is being returned to WILTRON for repair, contact Customer Service and a new shipping container will be sent to you free of charge. In the event neither of these two options is possible, follow the instructions below.

a. Use a Suitable Container. Obtain a corrugated cardboard carton with a 275-pound test strength and inside dimensions of no less than six inches more than the instrument dimensions; this allows for cushioning.

b. Protect the Instrument. Surround the instrument with polyethylene sheeting to protect the finish.

c. Cushion the Instrument. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches of cushioning on all sides.

d. Seal the Container. Seal the carton with shipping tape or with an industrial stapler.

e. Address the Container. If the instrument is being returned to WILTRON for service, mark the WILTRON address, as shown below, and your return address on the carton in one or more prominent locations. The WILTRON address is:

WILTRON Company
ATTN: Customer Service
825 E. Middlefield Road
Mountain View, CA 94043

CAUTION

If the microwave components, i.e., SWR Autotester and RF Detector(s), are being returned with the network analyzer, package them separately. Packaging network analyzer and microwave components in the same carton can result in damage to the equipment.

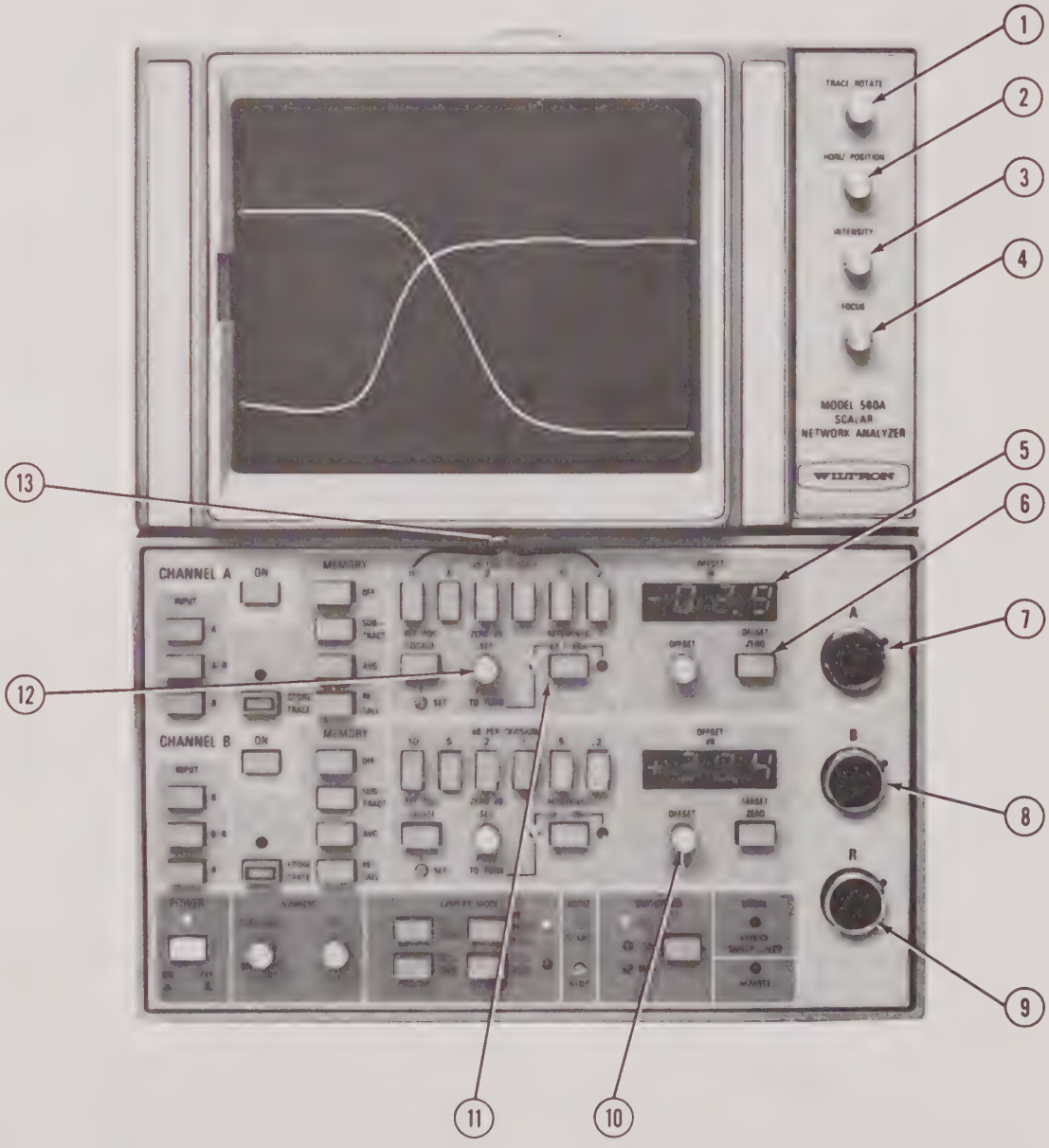


Figure 3-1a. Front Panel Controls, Connectors, and Indicators

SECTION III
OPERATION

3-1. INTRODUCTION

This section provides information on 560A front and rear panel controls, operational checkout, and Option 3 GPIB operation. The GPIB information includes general information and a description and summary of GPIB command codes.

3-2. CONTROLS AND CONNECTORS

3-2.1 Front Panel Controls and Connectors

Front panel controls and connectors are indexed in Figures 3-1a and 3-1b. As shown by front panel shading, controls are arranged in three functional groups. The top group of controls are for Channel A, the middle group are for Channel B, and the bottom group of controls are common to both channels. Controls for Channels A and B function identically for their respective channels; consequently, only the Channel A controls are described.

(1) TRACE ROTATE - adjusts slope of displayed trace (paragraph 3-4.3).

(2) HORIZ POSITION - adjusts horizontal position of displayed trace (paragraph 3-4.3).

(3) INTENSITY - controls intensity of displayed trace.

(4) FOCUS - controls focus of displayed trace.

(5) OFFSET dB - indicates offset in dB from zero dB reference when REFERENCE dB/dBm pushbutton switch is in dB position. When REFERENCE dB/dBm is in dBm position, OFFSET dB indicates absolute power in dBm at point where trace crosses reference line.

(6) OFFSET ZERO - returns OFFSET dB display readout to 00.0 and moves trace to 0 dB reference position.

(7) A - input connector for Channel A.

(8) B - input connector for Channel B.

(9) R - input connector for reference channel.

(10) OFFSET - controls vertical position of displayed trace. Used in conjunction with REFERENCE dB/dBm pushbutton switch and OFFSET dB display to provide either absolute power (dBm) or relative power (dB) measurements at point where trace crosses reference line (refer to paragraph 3-3.3).

(11) REFERENCE dB/dBm - determines which measurement units (dB or dBm) will be used. When dB indicator is lit, OFFSET dB display readout is in dB. When dBm indicator is lit, OFFSET dB display readout is in dBm. When dBm indicator flashes, OFFSET dB display readout is uncalibrated for absolute power measurements. The 560A is uncalibrated for dBm measurements when INPUT is in A-R (B-R) mode or when MEMORY is in SUBTRACT, AVG, or RECALL mode.

(12) ZERO dB SET - used during relative power (dB) measurements (REFERENCE dB/dBm pushbutton switch in dB position) to control the position of the 0 dB reference; control is inoperative in the dBm mode (refer to paragraph 3-3.3).

(13) dB PER DIVISION - group of pushbutton switches which determine vertical resolution of displayed signals. Each switch has a value, as indicated. For values other than those indicated, e.g., 3, 6, 12, etc., depress two or more switches. The sum of the depressed-switch values equals the dB per division resolution.

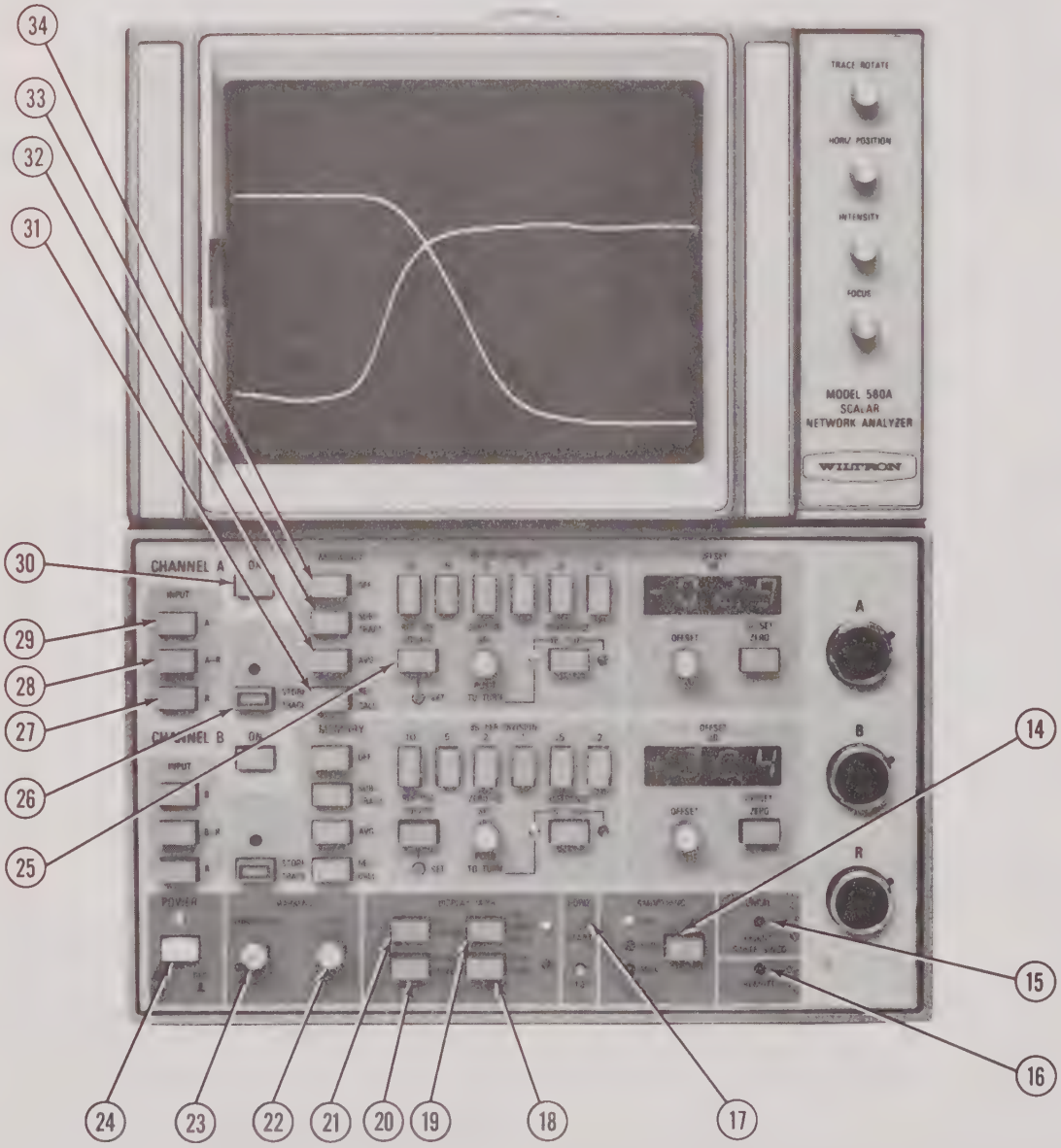


Figure 3-1b. Front Panel Controls, Connectors, and Indicators

(14) SMOOTHING - three-position switch (OFF, MIN, MAX) provides two levels of filtering, thereby improving the display at low signal levels.

(15) UNCAL - lights to indicate that the input horizontal ramp voltage is changing faster than internal memory can process and store data.

(16) REMOTE - lights to indicate that the 560A is operating under GPIB control.

(17) HORIZ START and STOP - potentiometers used to normalize the input horizontal sweep range voltage. START adjusts start of sweep (left side of CRT) and STOP adjusts end of sweep (right side of CRT). (Refer to paragraph 2-3.3.)

(18) X-Y PLOT - switches X and Y data to rear panel BNC connectors for input to X-Y plotter. This control operates in conjunction with REFRESH and REAL TIME pushbutton switches (refer to paragraph 3-3.5).

(19) REFRESH HOLD - stops updating of refresh display, thereby freezing it.

(20) REAL TIME - displays input data in real (sweep generator frequency sweep) time. Also, provides real time data to rear panel HORIZONTAL OUTPUT connector.

(21) REFRESH - displays input data at a constant 14 ms rate. When both REFRESH and X-Y PLOT pushbutton switches are depressed, refresh data is held (not updated) in memory and read out at a 30 s rate. The 30 s sweep is applied to the rear panel HORIZONTAL OUTPUT connector (refer to paragraph 3-3.5).

(22) TILT - tilts displayed marker pips from -45° to +45°.

(23) THRESHOLD - controls on/off and threshold level of input markers.

(24) POWER - applies line power to instrument.

(25) REF POS LOCATE - locates the reference line used for absolute (dBm) or relative (dB) power measurements. This is the line about which the display expands. When depressed, displayed trace disappears and reference appears as a horizontal line. Reference line can be repositioned by adjusting the SET potentiometer.

(26) STORE TRACE - stores displayed trace in internal memory. Red indicator remains lit until data is stored.

(27) R - displays reference channel on Channel A.

(28) A-R (Ratio Mode) - subtracts reference channel input from A channel input; result is displayed on Channel A.

(29) A - displays Channel A.

(30) CHANNEL A ON - switches dc power to Channel A circuits. When both this switch and the CHANNEL B ON switch are off (not depressed), the Model 560A will display Channel A.

(31) RECALL - used to recall data stored in memory.

(32) AVG - averages data stored in memory with selected channel input (R, A-R, A).

(33) SUBTRACT - subtracts data stored in memory from selected channel input (R, A-R, A).

(34) OFF - allows selected channel output (R, A-R, A) to bypass MEMORY SUBTRACT or MEMORY AVG circuits and be displayed on Channel A.

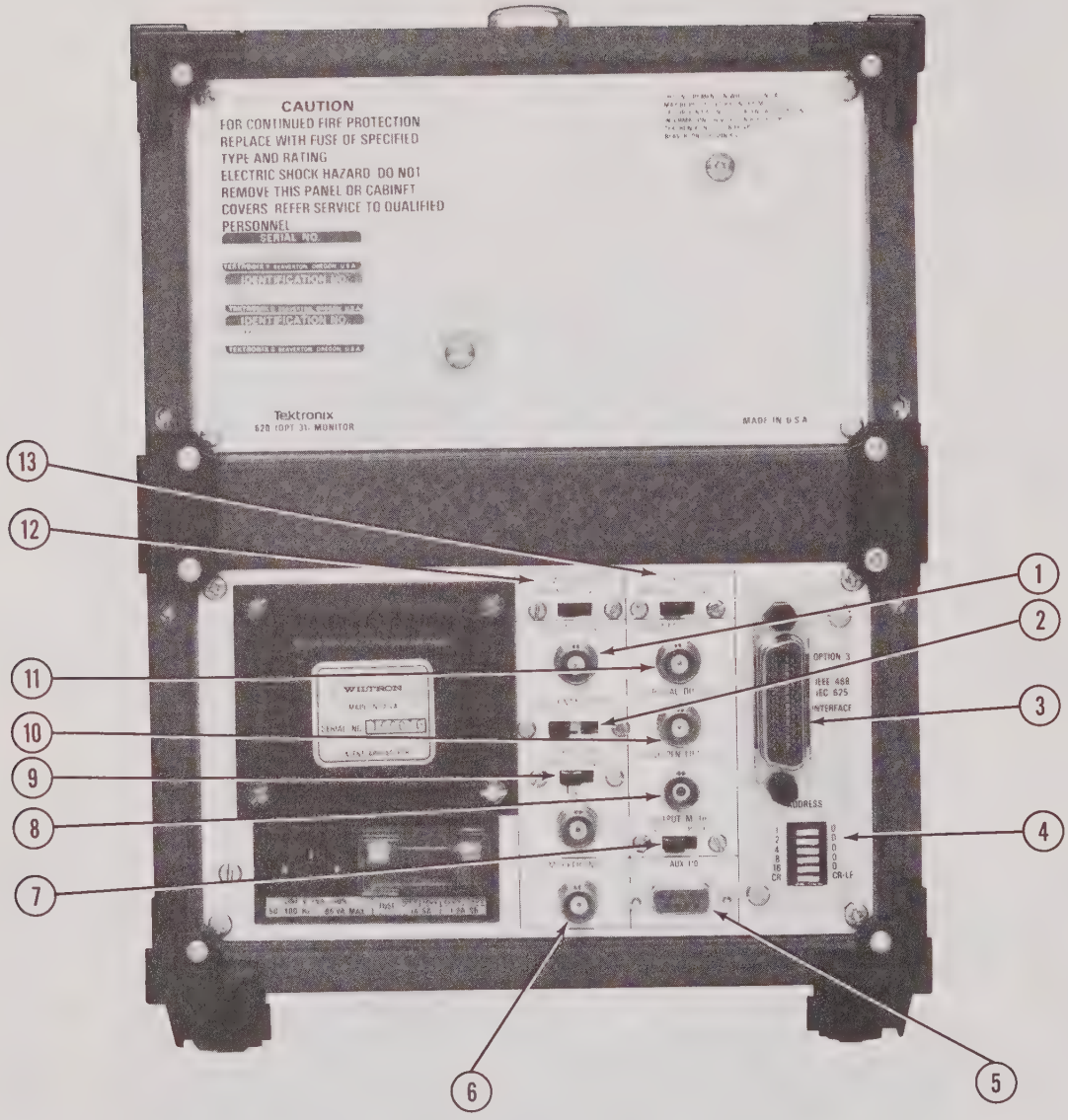


Figure 3-2. Rear Panel Controls and Connectors

3-2.2 Rear Panel Controls and Connectors

The Model 560A rear panel controls and connectors are described below. Refer to Figure 3-2 for the location of each item.

(1) HORIZONTAL INPUT - provides input for horizontal sweep ramp from sweep generator.

(2) HORIZONTAL SELECT - 3-position switch. Selects the proper sweep start and stop range for three possible horizontal sweep ramp inputs: 0 to +10V, 0 to +15V, and -8V to +8V.

(3) IEEE 488, IEC 625 INTERFACE (Option 3) - provides input/output connector for GPIB interface (paragraph 2-4.3).

(4) ADDRESS (Option 3) - six rocker switches. Each of the top five switches determines the 560A's GPIB talk/listen address; for an explanation of these switches, refer to paragraph 2-4.4. The sixth switch, (CR, CR/LF) selects the data-delimiting character; for an explanation of this switch, refer to paragraph 2-4.5.

(5) AUX I/O - D-type subminiature connector. Provides horizontal input, external Z-axis, marker, blanking/pen lift, and alternate-sweep connections between the sweeper and the 560A. To display alternate sweeps on the 560A, the sweeper must have two alternate-sweep control signals: (1) an alternate-sweep line that goes TTL-low to indicate the alternate-sweep input, and (2) an alternate line that goes TTL-high for Channel A display and TTL-low for Channel B display.

(6) MARKER INPUT - provides input for externally-generated marker signals.

(7) OUTPUT MODE - 2-position switch. In CRT position, the horizontal and vertical signals are present at the HORIZONTAL OUTPUT and VERTICAL OUTPUT jacks while positive-TTL blanking pulses are present during retrace. In the RCDR position, the horizontal and vertical signals are disconnected from their output jacks, and the normally-open relay contacts at the BLANK/PEN LIFT OUT jack (8) cause the recorder pen to lift off the paper during retrace. The lifted pen is then held off the paper until the next sweep. Can be modified internally for normally-closed contact operation.

(8) BLANK/PEN LIFT OUT - provides either blanking pulses or connection to pen lift relay contacts, depending upon the setting of the OUTPUT MODE switch (7).

(9) Z AXIS SELECT - 2-position switch. Selects (1) internally generated signals for retrace blanking and bandswitch points (INT position), or (2) external Z-axis input (EXT position). If a sweeper (WILTRON 6600 series) places a dwell on the sweep ramp to produce an intensity marker, the Z-axis signal from the sweeper must be connected to the Z AXIS INPUT connector, and the switch must be set to EXT position to display the intensity marker on the 560A. Also, if the HP 8620's harmonic markers are to be displayed, its Z-axis signal must be connected to the 560A as described above for the EXT position.

(10) VERTICAL OUTPUT - provides output connections for vertical, Y-axis signal. This signal varies from 0 to ±8V (1V/division), in proportion to the amplitude of the displayed signal plus the overrange (CRT has an 8-division vertical display overrange).

(11) HORIZONTAL OUTPUT - provides output connection for CRT horizontal signal. Horizontal signal is a ramp that varies from 0 to +10V in sync with the displayed sweep. Connects to X-input of external oscilloscope or X-Y plotter.

(12) LOW LEVEL CAL - 2-position switch. In NORM position, 560A processes input signals that fall within the specified range of the 560A. This setting is for normal instrument operation. In the EXT position, 560A processes extremely low-level signals. For these low levels, the RF output of the sweeper must be off (<60 dBm) during retrace.

(13) INPUT - 2-position switch. In the NORM position, the CRT displays either Channel A, B, or both, depending upon the front panel control settings. In the A ONLY position, only the A input is detected and displayed on the CRT. Also, if the CHANNEL B INPUT button is depressed and the Channel B display controls are properly set, a second display of the A input will appear.

3-2.3 Side Panel Controls

The Model 560A right side panel controls are described below. Refer to Figure 3-3 for the location of each item.

(1) LOW LEVEL TRIM, CH A - Optimizes Channel A for measurements below -45 dBm.

(2) LOW LEVEL TRIM, CH B - Optimizes Channel B for measurements below -45 dBm.

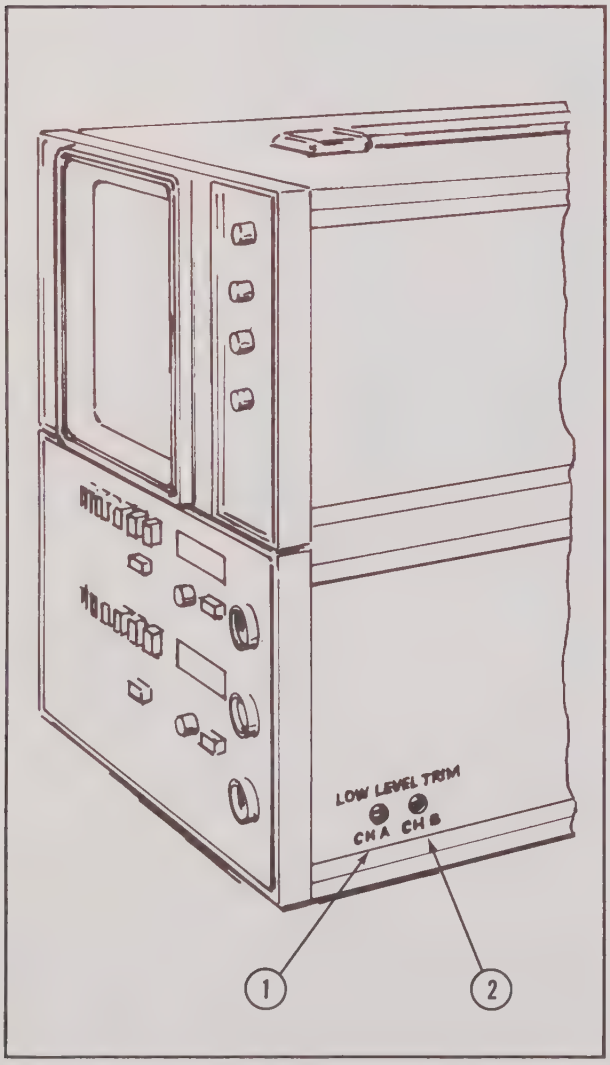


Figure 3-3. Side Panel Controls

3-3 USING FRONT PANEL CONTROLS

Front panel controls are arranged in six functional groups: input, memory, vertical scale factor, marker, display mode, and smoothing. The following paragraphs contain both a detailed description and instructions on how to use each control.

3-3.1 Input Controls

Input controls allow selection of the manner in which the RF measurement inputs are connected to the display and memory circuits. There are three input channels and two display channels available. Input controls allow the selection of A, B, R, A-R, or B-R — where R is the reference channel. The rear panel INPUT switch selects the A ONLY mode (paragraph 7-12.1).

a. A or B Measurement Controls. These pushbuttons connect the output of the SWR Autotester to A or B Channel for return loss measurements, or the output of the RF Detector to A or B Channel for transmission loss/gain or absolute power measurement. See Figure 3-4 for a typical transmission loss/gain and return loss measurement setup.

b. R Reference Controls. These pushbuttons connect the output of the RF detector to R Channel logarithmic amplifier

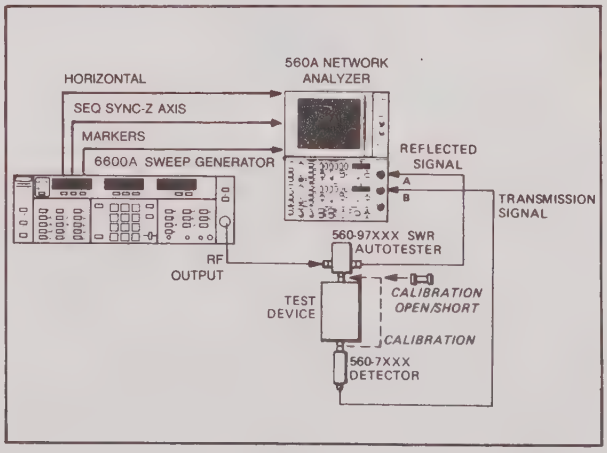


Figure 3-4. Return Loss and Transmission Loss/Gain Measurement Equipment Setup

for display on A or B Channel trace. A typical test setup using a power splitter is shown in Figure 3-5. In an equipment setup of this type, the R Channel is available to monitor the incident signal for return loss measurements or the absolute power signal for transmission measurements without having to reconfigure test cables. By depressing the R pushbutton, this data is made available to the CRT.

c. A-R or B-R Ratio Controls. These pushbuttons subtract the output of the R Channel logarithmic amplifier from the output of the A or B Channel logarithmic amplifier. Subtracting the logarithm of R from the logarithm of A is the same as taking the ratio of the logarithm of A/R; for this reason, A-R and B-R are known as ratio inputs. These ratio inputs have several applications. In transmission measurements, they can be used to improve source match and eliminate the effects of sweep generator power drift, measure very small insertion loss signals more accurately, and track between two components, i.e., measure differences or similarities between two filters, amplifiers, attenuators, etc. In return loss measurements, ratioing can be used (1) to compensate for fluctuations in source power where long transmission lines are used (e.g., measurement of aircraft systems where test equipment is outside the aircraft and system is inside the aircraft) or (2) to eliminate the need for recalibration when source power is deliberately changed by adding attenuation or by changing the sweep generator RF power level control.

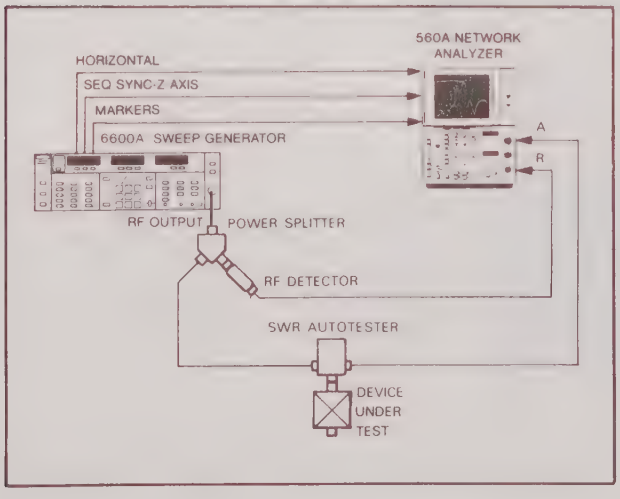


Figure 3-5. Typical Equipment Setup for Using R Channel

3-3.2 Memory Controls

Memory controls are available in both Channel A and Channel B; they provide four operations: (1) storage of input data (STORE TRACE), (2) subtraction of stored data from input data (SUBTRACT), (3) averaging of stored data with input data (AVG), and (4) recall of stored data upon request (RECALL). Two uses for these controls are described below.

a. Using Memory To Store and Subtract Transmission System Residuals. A primary use of memory is to store microwave transmission measurement system residuals. These residuals, caused by inherent frequency response variations within the measurement system, are later subtracted from measured data. The process of storing residuals and making them available for later subtraction from input data is known as display normalization. An equipment setup for transmission loss/gain and return loss measurements is shown in Figure 3-6. A procedure for normalizing the 560A display is presented in Table 3-1. This procedure, with its notes and waveform photographs, is designed to provide a demonstration of how the memory controls are used during actual measurement applications. The interaction between display and memory that occurs during the Display Normalization Procedure is summarized in Figure 3-7.

b. Using Memory To Calibrate the Return Loss Measurement System. Another use of memory is in calibrating the SWR Autotester for return loss measurements. The reference reflection for

return loss measurements is the 100% reflection that occurs when the SWR Autotester test port is terminated in either an open or a short. When this reflection is used without compensation, an error is introduced because of test port match. To compensate for this error, a technique known as open/short averaging is used. This technique is based on the fact that the reflection from an open is 180 degrees out of phase from the reflection from a short. Consequently, when these two reflections are averaged together, the test port match error signals cancel. The remaining signal is the 100% reflection from the device under test. In the 560A, the open/short averaging technique is accomplished with the aid of memory.

The return loss measurement system test setup is shown in Figure 3-8. A procedure for calibrating the SWR Autotester is presented in Table 3-2. This procedure, like the one used for display normalization, is designed to provide a demonstration of how the memory controls are used during actual measurement applications. The interaction between display and memory that occurs during the Return Loss Calibration Procedure is summarized in Figure 3-9.

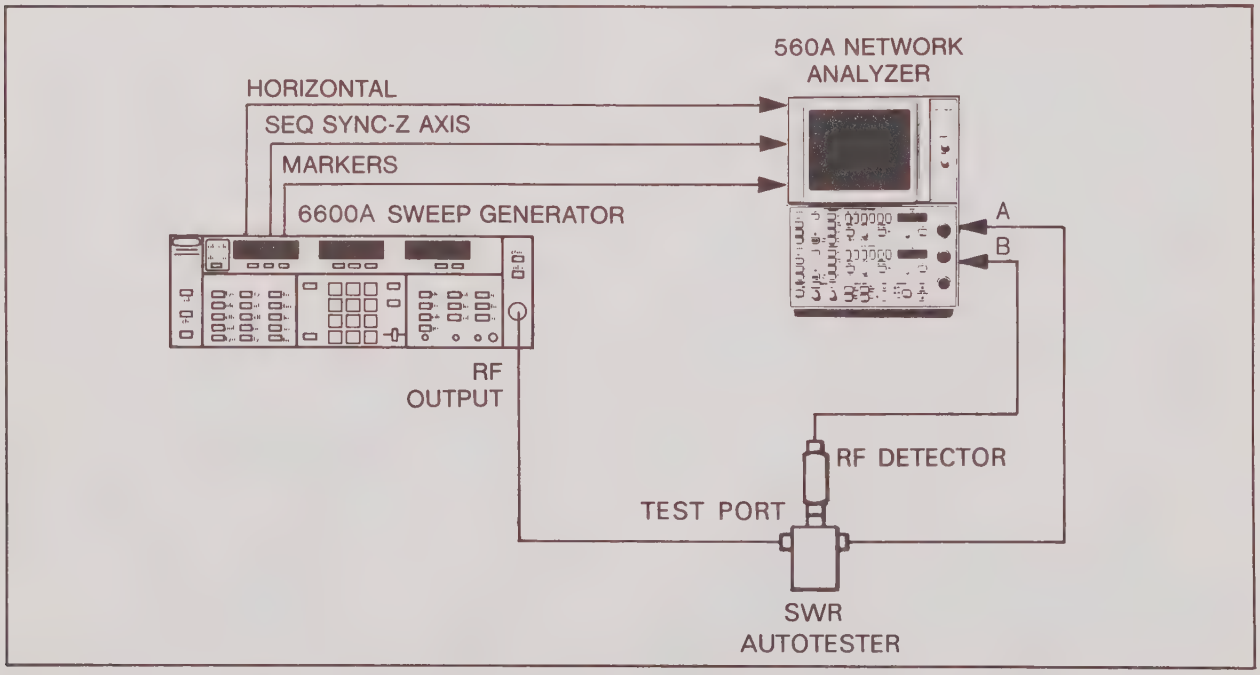


Figure 3-6. Equipment Setup for Storing Transmission System Residuals

Table 3-1. Display Normalization Procedure

1. Set up equipment and perform initial switch positioning:

6600A Sweep Generator

POWER: ON
Press RESET.

Network Analyzer

CHANNEL A ON: Not depressed
INPUT: A
MEMORY: OFF
dB PER DIVISION: 10
REFERENCE dB/dBm: Not depressed
OFFSET ZERO: Not depressed

CHANNEL B ON: Depressed
INPUT: B
MEMORY: OFF
dB PER DIVISION: 10
REFERENCE dB/dBm: Not depressed
(dB indicator lit)
OFFSET ZERO: Not depressed
THRESHOLD: OFF (fully CCW)
TILT: Center of range
DISPLAY MODE: REFRESH
SMOOTHING: OFF
POWER: ON

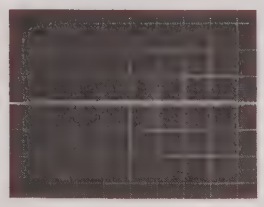
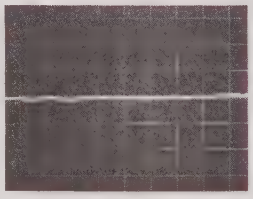
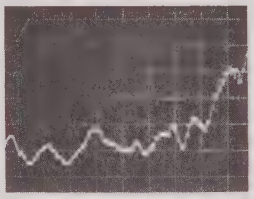
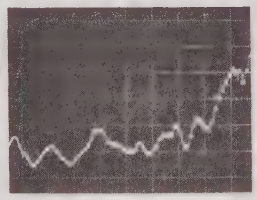
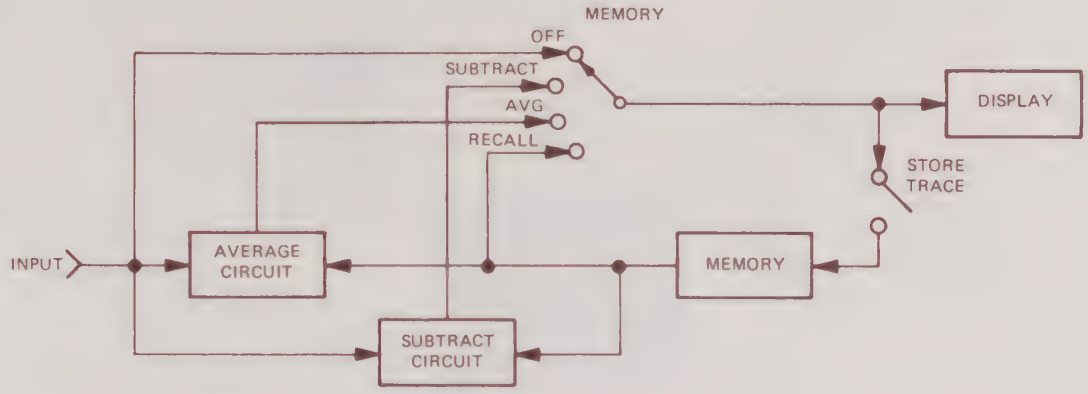
Step	Procedure	Display	Notes
2.	Connect Channel B RF Detector to test port of SWR Autotester.	N/A	Normalization should include any adapters that will be used in the measurement, i.e., any component that will appear between the output of the sweeper and the input to the DUT must be included in the normalization process.
3.	Depress Channel B REF POS LOCATE pushbutton switch and adjust SET screwdriver potentiometer to position reference line as shown.		The SET potentiometer is analogous to Vertical Position control on oscilloscope; consequently, initial positioning is arbitrary. Center-screen is used for convenience.
4.	Release REF POS LOCATE pushbutton switch.	N/A	Reference line disappears and Channel B signal returns.

Table 3-1. Display Normalization Procedure (Continued)

Step	Procedure	Display	Notes
5.	Adjust OFFSET control for a 00.0 OFFSET dB display.	N/A	This sets the OFFSET control to its null point.
6.	Adjust ZERO dB SET control to position trace on REF POS LOCATE reference line.		This places the dB reference line coincident with the primary reference line.
7.	Decrease dB PER DIVISION setting until display fills screen, (If necessary, adjust SLOPE for a level trace.)		To allow for full resolution, the 560A has a 50% display overrange capability; consequently, signals can deflect a maximum of 8 divisions from the reference line.
8.	Depress Channel B STORE TRACE pushbutton switch.		Sweep generator waveform, as modified by system residuals, is stored in Channel B memory.
9.	Depress Channel B SUBTRACT pushbutton switch.		The straight-line trace is the normalized display. This display occurs because the store signal, which is the same as the input signal, is subtracted from input signal; consequently, the difference is zero.
10.	Remove RF Detector from test port of SWR Autotester.	N/A	N/A



SEQUENCE OF EVENTS	CONNECTED TO TEST PORT OF SWR AUTOTESTER	POSITION OF MEMORY CONTROLS	DISPLAYED ON CRT	STORED IN MEMORY
1	RF DETECTOR	OFF	TRANSMISSION RESIDUALS	UNDEFINED
2	RF DETECTOR	OFF / STORE TRACE	TRANSMISSION RESIDUALS	TRANSMISSION RESIDUALS
3	RF DETECTOR	OFF	TRANSMISSION RESIDUALS	TRANSMISSION RESIDUALS
4	RF DETECTOR	SUBTRACT	TRANSMISSION RESIDUALS − TRANSMISSION RESIDUALS (STRAIGHT LINE)	TRANSMISSION RESIDUALS
5	DUT	SUBTRACT	DUT − TRANSMISSION RESIDUALS	TRANSMISSION RESIDUALS

During the Display Normalization Procedure (Table 3-1), the interaction between the display of data on the CRT and the storage of data in memory is summarized in the tabulation of events shown above.

With an RF detector connected to the test port of an SWR Autotester (Figure 3-6) and the MEMORY switch in the OFF position (as shown in the block diagram), transmission residuals are applied only to the display. This is shown by Event 1. When the momentary STORE TRACE switch is activated — Event 2 — the transmission residuals are also stored in memory. When STORE TRACE is released in Event 3, the transmission residuals are in both places: display and memory. In Event 4, the MEMORY switch is changed from OFF to SUBTRACT. The transmission residuals already stored in memory are subtracted from the input transmission residuals. The difference signal, zero, is a straight line that is displayed on the CRT. Event 5 shows the results when a DUT is connected between the RF detector and the SWR Autotester test port. The transmission residuals are now subtracted from the DUT transmission signal, leaving the true DUT characteristics for display. Note: REF POS LOCATE reference line and dB PER DIVISION switch-bank settings can be altered without affecting calibration.

Figure 3-7. Summary of Memory and Display Interaction That Occurred during the Display Normalization Procedure

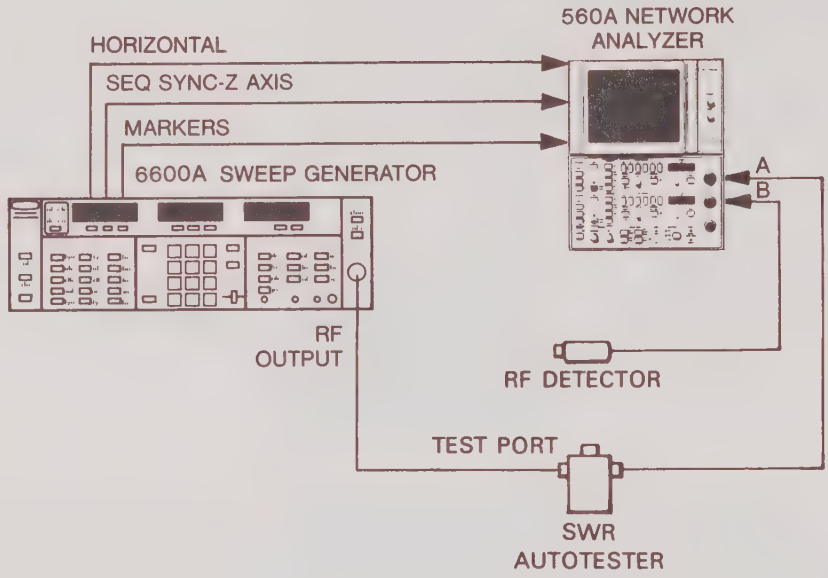


Figure 3-8. Equipment Setup for Return Loss Measurement System Calibration

Table 3-2. Return Loss Measurement Calibration Procedure

1. Set up equipment and perform initial switch positioning:

6600A Sweep Generator

POWER: ON
Press RESET.

Network Analyzer

CHANNEL A: ON
INPUT: A
MEMORY: OFF
dB PER DIVISION: 10
REFERENCE dB/dBm: Not depressed
(dB indicator lit)
OFFSET ZERO: Not depressed

CHANNEL B: OFF
INPUT: B
MEMORY: OFF
dB PER DIVISION: 10
REFERENCE dB/dBm: Not depressed
OFFSET ZERO: Not depressed
THRESHOLD: OFF (fully CCW)
TILT: Center of range
DISPLAY MODE: REFRESH
SMOOTHING: OFF
POWER: ON

Table 3-2. Return Loss Measurement Calibration Procedure (Continued)

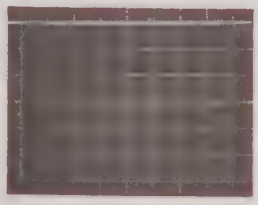
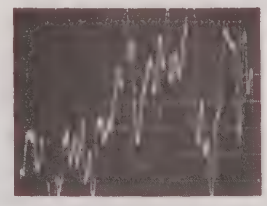
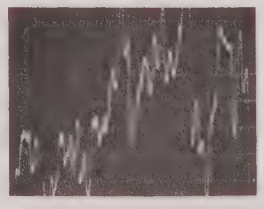
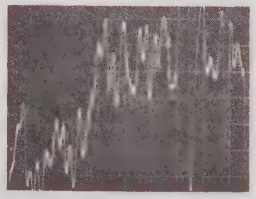
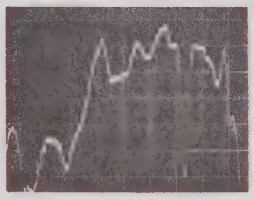
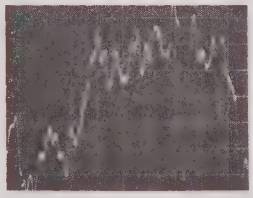
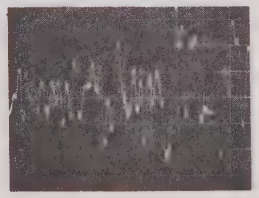
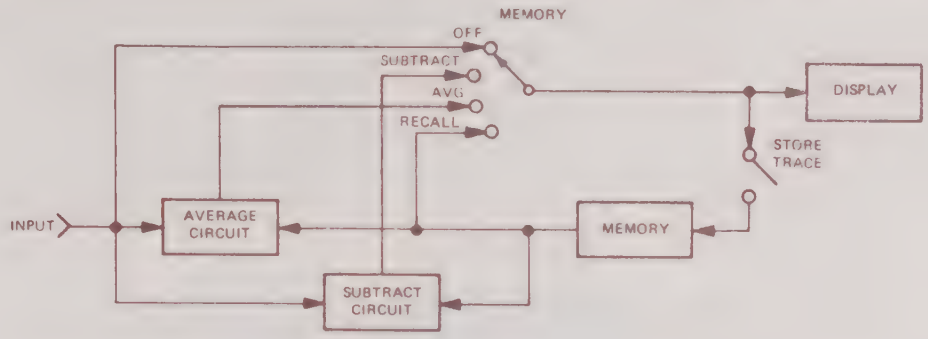
Step	Procedure	Display	Notes
2.	Connect open to test port of SWR Autotester	N/A	The fully-reflected sweep generator signal is displayed.
3.	Depress Channel A REF POS LOCATE pushbutton switch; adjust SET screwdriver potentiometer and position reference line as desired.		Reference line placed in this position to observe the downward deflection of the return loss signal.
4.	Release REF POS LOCATE pushbutton switch.	N/A	N/A
5.	Adjust OFFSET control for a 00.0 OFFSET dB display.	N/A	This sets the OFFSET control to its null point.
6.	Adjust ZERO dB SET control to position trace on REF POS LOCATE reference line.		This places the dB reference line coincident with primary reference line.
7.	Decrease dB PER DIVISION setting until display fills screen. Readjust OFFSET control, if necessary, to keep display on screen.		To allow for full resolution, the 560A has a 50% overrange capability; consequently, signals can deflect a maximum of 8 divisions from the reference line in both a positive and a negative direction without undergoing compression.
8.	Depress Channel A STORE TRACE pushbutton switch.		Reflected signal from open is stored in memory.

Table 3-2. Return Loss Measurement Calibration Procedure (Continued)

Step	Procedure	Display	Notes
9.	Remove open; connect short in its place.		Except for phase reversal, this signal is similar to the reflected signal from the open.
10.	Depress Channel A AVG pushbutton switch.		The average of the open/short reflections is displayed.
11.	Depress Channel A STORE TRACE pushbutton switch once and wait for light to extinguish.		Display is showing the result of the open/short average being averaged with the reflections from the short. The average of the open/short reflections is in memory. It is important that STORE TRACE be depressed only once. If depressed a second time, the data on the display will be stored in memory. This will result in erroneous return loss measurements.
12.	Depress Channel A SUBTRACT pushbutton switch.		Display is showing the result of the open/short average having been subtracted from the short.
13.	Remove short from test port. Reflectometer is now ready for return loss measurements.	N/A	N/A



SEQUENCE OF EVENTS	CONNECTED TO TEST PORT OF SWR AUTOTESTER	POSITION OF MEMORY CONTROLS	DISPLAYED ON CRT	STORED IN MEMORY
1	OPEN	OFF	OPEN	UNDEFINED
2	OPEN	OFF / STORE TRACE	OPEN	OPEN
3	SHORT	OFF	SHORT	OPEN
4	SHORT	AVG	$\frac{\text{SHORT + OPEN}}{2}$	OPEN
5	SHORT	AVG / STORE TRACE	$\frac{\text{SHORT + OPEN}}{2} \Rightarrow \text{SHORT} + \frac{\frac{\text{SHORT + OPEN}}{2}}{2}$	$\frac{\text{SHORT + OPEN}}{2}$
6	SHORT	AVG	$\text{SHORT} + \frac{\frac{\text{SHORT + OPEN}}{2}}{2}$	$\frac{\text{SHORT + OPEN}}{2}$
7	SHORT	SUBTRACT	$\text{SHORT} - \frac{\text{SHORT + OPEN}}{2}$	$\frac{\text{SHORT + OPEN}}{2}$
8	DEVICE UNDER TEST	SUBTRACT	$\text{DUT} - \frac{\text{SHORT + OPEN}}{2}$	$\frac{\text{SHORT + OPEN}}{2}$

Legend: AVG = $\frac{\text{Input + Memory}}{2}$ SUBTRACT = Input − Memory DUT = Device Under Test $\Rightarrow$ = Changes To

During the Return Loss Calibration Procedure (Table 3-2) the interaction between the display of data on the CRT and the storage of data in memory is summarized in the tabulation of events shown above.

When the open is connected to the test port of the SWR Autotester (Figure 3-8) and the MEMORY switch is in the OFF position (as shown in the block diagram), the reflection from the open is displayed on the CRT. This is shown in Event 1. When the momentary STORE TRACE switch is activated, Event 2, the reflection from the open is also stored in memory. When the open is replaced by a short in Event 3, the reflection from the short is displayed; however, the reflection from the open is still stored in memory. When the MEMORY switch is changed from OFF to AVG in Event 4, the reflection from the short is averaged with the reflection from the open, and the result displayed on the CRT. In Event 5, STORE TRACE is activated again. The display changes as shown. The average of the open and short changes to the average of the short plus the average of the open and short. When STORE TRACE is released in Event 6, the average of the short plus the average of the open and short is still on the display; however, the average of the open and short is still in memory. When the MEMORY switch is changed from AVG to SUBTRACT in Event 7, the average of the open and short, stored in memory, is subtracted from the short, present at the input, and displayed on the CRT. Event 8 shows the results when a DUT is connected to the test port of the SWR Autotester. The average from the open and short is subtracted from the DUT, leaving the true DUT return loss signal for display. Note: REF POS LOCATE reference line and dB PER DIVISION switch-bank settings can be altered without affecting calibration.

Figure 3-9. Summary of Memory and Display Interaction That Occurred During the Return Loss Measurement Procedure, Table 3-3.

3-3.3 Vertical Scale Factor Controls

Vertical scale factor controls provide each channel (A, B, R) with either an absolute (dBm) or a relative (dB) power-measuring capability. These controls include the dB PER DIVISION switch-bank; the REF POS LOCATE, REFERENCE dB/dBm, and OFFSET ZERO pushbutton switches; the OFFSET and ZERO dB SET controls; the REF POS SET screwdriver potentiometer; and the OFFSET dB display. An equipment setup for measuring the output power of the sweep generator is shown in Figure 3-10. Table 3-3 is a procedure for demonstrating the use of the vertical scale factor controls.

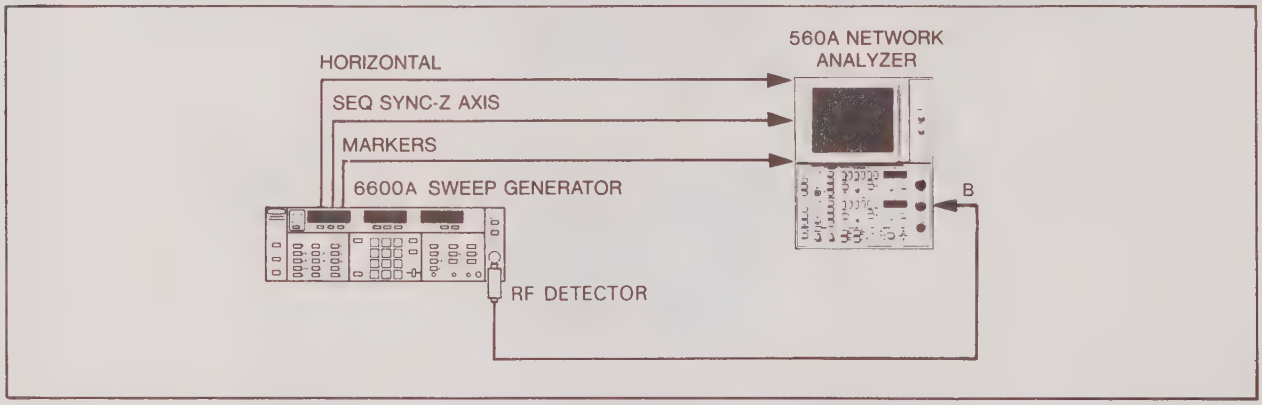


Figure 3-10. Equipment Setup for Measuring Power Output of Sweep Generator RF Plug-In

Table 3-3. Power Measurement Procedure

1. Set up equipment and perform initial switch positioning:

6600A Sweep Generator

POWER: ON
Press RESET.

Network Analyzer

CHANNEL A: OFF
- INPUT: A
- MEMORY: OFF
- dB PER DIVISION: 10
- REFERENCE dB/dBm: Not depressed
- OFFSET ZERO: Not depressed
- OFFSET dB: 00.00

CHANNEL B: ON
- INPUT: B
- MEMORY: OFF
- dB PER DIVISION: 10
- REFERENCE dB/dBm: Not depressed (dB indicator lit)
- OFFSET ZERO: Not depressed
- OFFSET dB: 00.00

THRESHOLD: OFF (fully CCW)
TILT: Center of range
DISPLAY MODE: REFRESH
SMOOTHING: OFF
POWER: ON

Table 3-3. Power Measurement Procedure (Continued)

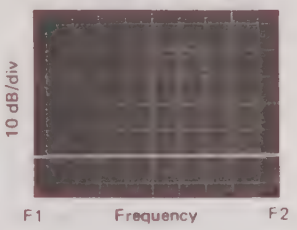
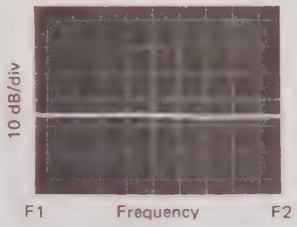
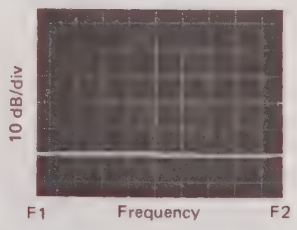
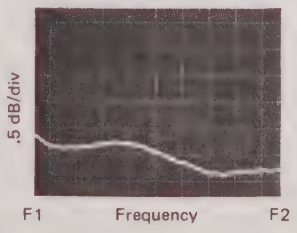
Step	Procedure	Display	Notes
2.	Depress Channel B REFERENCE dB/dBm pushbutton switch.	N/A	This selects dBm as the reference for future measurements.
3.	Depress and hold Channel B REF POS LOCATE pushbutton switch and adjust SET screwdriver potentiometer to position reference line as shown.		The reference line may be positioned anywhere on the display; the position shown is for convenience only.
4.	Release REF POS LOCATE pushbutton switch.		Reference line is replaced by Channel B signal. Position of this signal in relation to reference line is determined by dB PER DIVISION pushbutton switches.
5.	Adjust OFFSET control to position the mid-frequency point (center) on the trace to the same graticule line that the REF POS LOCATE reference line is positioned to.		The OFFSET dB display indicates the input signal's absolute power level in dBm.
6.	Depress dB PER DIVISION pushbutton switch labeled .5.		Trace expands about the reference line.

Table 3-3. Power Measurement Procedure (Continued)

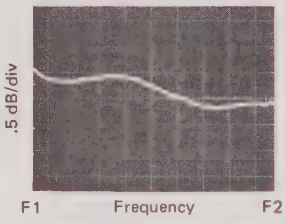
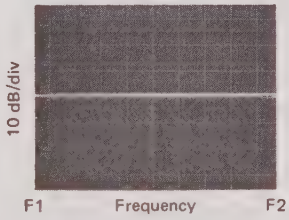
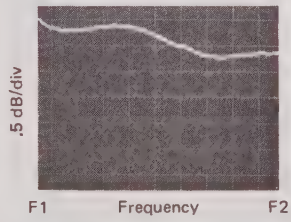
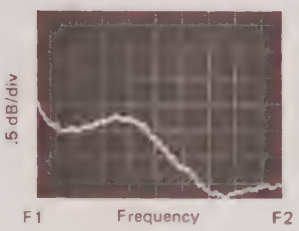
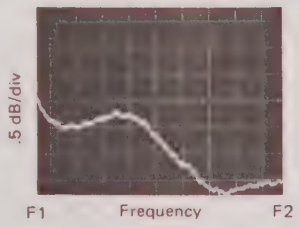
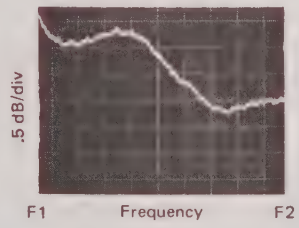
Step	Procedure	Display	Notes
7.	Depress REFERENCE dB/dBm pushbutton switch.	N/A	Trace may be off screen; it is displaced from the REF POS LOCATE reference line by the ZERO dB SET control.
8.	Push and turn ZERO dB SET control to position trace near center screen.		(To find trace more easily, reduce dB PER DIVISION resolution to 10. After positioning trace, return to .5.) This step and the two that follow demonstrate the relationship between this control and the REF POS LOCATE reference line.
9.	Depress and hold REF POS LOCATE pushbutton switch and adjust SET potentiometer to position reference line on center graticule line.		Trace is replaced by reference line.
10.	Release REF POS LOCATE pushbutton switch.		Trace reappears near top of screen. This shows that the reference line for dB measurements is offset from the reference line for dBm measurements by the positioning of the ZERO dB SET control.
11.	Depress OFFSET ZERO pushbutton switch.	N/A	OFFSET dB display indicates ±00.0.

Table 3-3. Power Measurement Procedure (Continued)

Step	Procedure	Display	Notes
12.	Push and turn ZERO dB SET control to position low-frequency end of trace on reference line.		This step and the three that follow present a technique for "adding and subtracting" in dB using the OFFSET dB display. In this technique, ZERO dB SET is used to establish a 00.0 dB reference at any desired point on the trace. After establishing this point, OFFSET is used to measure to any other point on the waveform; the measurement value is indicated on the OFFSET dB display.
13.	Depress OFFSET ZERO pushbutton switch.	N/A	Trace disappears from screen.
14.	Adjust OFFSET control to position low-frequency end of trace on reference line.		(As noted in Step 8, it will be easier to find trace if dB PER DIVISION resolution is temporarily reduced to 10.) This adjustment of the OFFSET control establishes a 0 dB reference at the low-frequency end of the trace.
15.	Adjust OFFSET control to position high-frequency end of trace on reference line.		The dB value indicated on the OFFSET dB display is the variation in power from the low end to the high end of the frequency band. Typically, this value is less than 1.0 dB.
	End of Procedure		

3-3.4 Marker Controls

Marker controls provide control over sweep generator markers that appear on the 560A CRT. If the WILTRON 6600A Series sweeper provides the markers, threshold control is provided by the front panel OFF-THRESHOLD control. If the Hewlett-Packard Model 8620 provides the markers, markers appear on screen when the OFF-THRESHOLD control is is moved from the OFF (detent) position. In the case of either sweep generator, markers are fixed in amplitude. The THRESHOLD control, when used, determines only the threshold voltage at which internal marker circuitry responds to external marker inputs. The front panel TILT control provides up to plus or minus (±) 45 degrees of tilt for displayed markers. This tilting of markers is very helpful in identifying markers where the displayed signal has steep skirts, e.g. measurements of an electronic filter (Figure 3-11). Additionally, when the 6600A Series sweeper with its three different types of markers is used, the 560A response is different for each marker-type. This response is described below.

a. INTENSITY Markers. The 560A responds to intensity markers only in the REAL TIME display mode. Markers appear as an intensified dot; see page 3-5, (9).

b. VIDEO Markers. The 560A responds to video markers in REAL TIME or REFRESH display modes. Markers appear as a VIDEO pulse; they respond to both THRESHOLD and TILT controls.

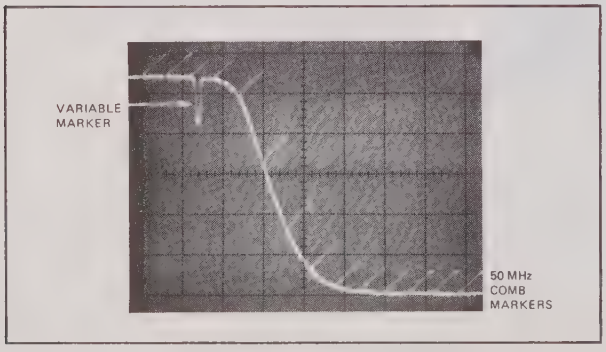


Figure 3-11. Bandpass Filter Measurement Showing Marker Tilting

c. RF Markers. The 560A responds to RF markers in both REAL TIME and REFRESH display modes. Markers appear as a notch in the displayed trace, and, since the markers modulate the RF signal, they do not respond to either MARKER TILT or THRESHOLD control.

CAUTION

Marker data could be altered, or destroyed, if the storage memory is used to store a signal containing marker information. Since the RF marker pips modulate the signal, they are stored along with the signal; consequently, when the stored signal is recalled and either averaged with (MEMORY AVG depressed) or subtracted from (MEMORY SUBTRACT depressed) the input markers, the stored markers are also averaged with or subtracted from the input markers.

3-3.5 Display Mode Controls

Display mode controls provide for five display modes: REAL TIME, REFRESH, REFRESH HOLD, X-Y PLOT-REFRESH, and X-Y PLOT-REAL TIME. These modes are described below.

a. REAL TIME Mode. In this mode, the horizontal sweep ramp from the sweep generator provides drive for the CRT X-axis display; the input data from the logarithmic amplifier provides drive for the Y-axis display. The horizontal display time is determined by the sweep generator sweep time control – SWEEP TIME on the WILTRON 6600A Series or TIME-SECONDS on the HP 8620C.

b. REFRESH Mode. In this mode, an internally generated 14 ms sweep ramp provides drive for the CRT X-axis display. An internal memory, known as refresh memory, provides drive for the

CRT Y-axis display. The Y-axis data is effectively read into refresh memory in real time, and read out of refresh memory in refresh (14 ms) time. The data is, therefore, proportional to sweep generator frequency. The refresh capability provides a horizontal display time proportional to, but independent of, the sweep generator's sweep time control. This provides for a non-flickering display.

c. REFRESH HOLD Mode. In this mode, the refresh (14 ms) ramp provides drive for the CRT X-axis display; refresh memory provides drive for the Y-axis display. In REFRESH HOLD, the display data is being read out of the refresh memory and applied to the display at a 14-ms rate; however, the refresh memory is prevented from having new data written into it, thereby allowing only previously-stored data to be made available for display. The indicator associated with the REFRESH HOLD switch remains lit while this mode is activated. This mode is useful when the display is to be photographed.

d. X-Y PLOT-REFRESH Mode. In this mode, X-axis and Y-axis voltages come from the refresh circuitry. The 14 ms refresh ramp is slowed to 30 s and applied to the HORIZONTAL OUTPUT connector; the stored data in the refresh memory is applied to the VERTICAL OUTPUT connector. As described for REFRESH HOLD, above, new data is prevented from being written into the refresh memory during this mode. This mode is entered into when the X-Y PLOT pushbutton switch is depressed while the REFRESH pushbutton switch is depressed. Approximately one second after the 30 s sweep begins, the pen-lift relay causes the X-Y plotter's pen to drop. A delay of 500 ms prevents an erroneous line from being traced on the X-Y plotter's paper. In dual channel operation (both CHANNEL ON pushbutton switches depressed), the channels are plotted sequentially: first Channel A then Channel B. A one-second delay is provided between these two plots. Also, in either single or dual channel operation, the plot may be aborted by depressing X-Y PLOT a second time. For single channel operation, the indicator associated with the X-Y PLOT switch remains lit until the plot is completed; for dual channel operation, the indicator remains lit until both plots are completed. When the indicator goes out, the REFRESH sweep returns to the display. A procedure for setting the X and Y parameters on the recorder in preparation for making an X-Y plot is provided in Table 3-4; the equipment setup is shown in Figure 3-12.

e. X-Y PLOT-REAL TIME Mode. This mode is entered when the X-Y PLOT pushbutton switch is depressed while in the REAL TIME display mode. Approximately 500 ms after the sweep generator begins a new horizontal forward sweep, the pen-lift relay causes the X-Y plotter's pen to drop. This delay prevents an erroneous line from being traced on the X-Y plotter's paper. The delay allows the X-Y plotter time in which to move the pen from its rest position to the position where the plot actually begins. In dual channel operation (both CHANNEL ON pushbuttons depressed), the channels are plotted sequentially: first Channel A then Channel B. A delay is provided between these two plots. For single channel operation, the indicator associated with the X-Y PLOT switch remains lit until the plot is completed; for dual channel operation, the indicator remains lit until both plots are completed. The intended sweep generator mode when using the X-Y plot mode is triggered sweep. With a triggered sweep, the X-Y plot circuitry is armed when the mode is entered, but the sweep does not begin until the sweep generator's trigger switch is activated.

3-3.6 Smoothing Control

Smoothing control provides two levels of filtering to improve signal response at low signal levels. This control is a three-posi-

tion (OFF, MIN, MAX) switch. When the SMOOTHING switch is depressed to light the MIN indicator, the first level of filtering is activated. With SMOOTHING-MIN selected, input signals below -30 dBm receive filtering. Input signals above -30 dBm are not filtered. When the SMOOTHING switch is depressed to light the MAX indicator, the second level of filtering is selected. With SMOOTHING-MAX selected, input signals below -30 dBm receive filtering — first-level filtering from -30 dBm to -40 dBm and second-level filtering below -40 dBm. Input signals above -30 dBm receive no filtering. Filtering greatly improves noise-reduction at low signal levels; however, filtering slows the response time of the logarithmic amplifier. Consequently, if SMOOTHING-MIN or -MAX is selected, the sweep time of the sweep generator, should be reduced to ensure faithful reproduction of input signals.

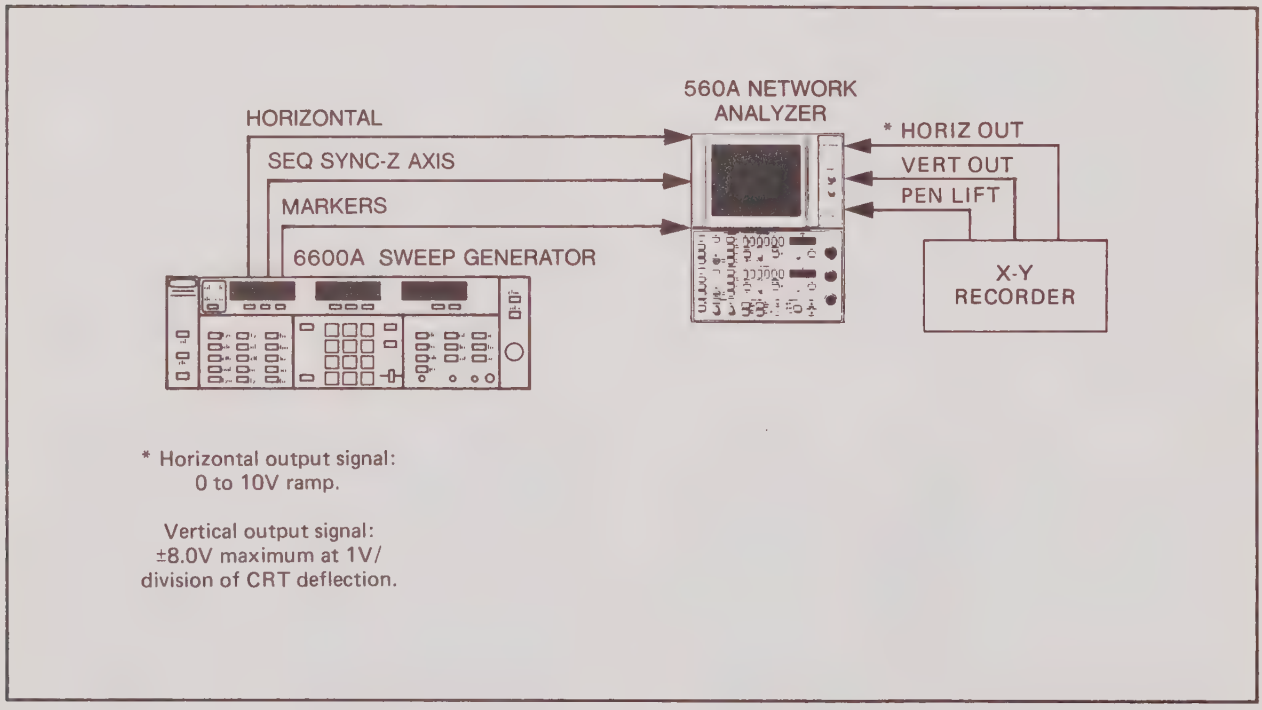


Figure 3-12. Equipment Setup for X-Y Recorder Setup

Table 3-4. X-Y Recorder Setup Procedure

1. Set up equipment and perform initial switch positioning:

6600A Sweep Generator

POWER: ON
Press RESET.

Network Analyzer

CHANNEL A: ON
INPUT: A
MEMORY: OFF
dB PER DIVISION: 10
REFERENCE dB/dBm: Depressed
(dBm indicator lit)
OFFSET ZERO: Not depressed
OFFSET dB: 00.0

CHANNEL B: OFF
INPUT: B
MEMORY: OFF
dB PER DIVISION: 10
REFERENCE dB/dBm: Depressed
OFFSET ZERO: Not depressed
THRESHOLD: OFF (fully CCW)
TILT: Center of range
DISPLAY MODE: REAL TIME
SMOOTHING: OFF
OUTPUT MODE (rear panel): RCDR
POWER: ON

Step	Procedure	Results
2	On 560A, lightly depress A-R or R pushbutton switch so that all three INPUT switches are released (not depressed).	Trace is present on CRT.
3	On 560A, adjust Channel A SET screwdriver potentiometer to center trace on CRT.	Trace is centered.
4	On 560A, check that HORIZ START and STOP screwdriver potentiometers are properly adjusted; refer to paragraph 2-3.3.	Refer to paragraph 2-3.3.
5	On 6600A, press MANUAL SWEEP button.	Beam dot appears on 560A CRT.
6	On 560A, position rear panel OUTPUT MODE switch to CRT.	N/A
7	On 6600A, rotate MANUAL SWEEP control fully counterclockwise.	Beam dot on 560A CRT moves to left graticule edge.
8	On recorder, adjust horizontal (X) Offset (or Position) control to position pen over left edge of plot graph. Press down on pen and make contact with paper.	Ink dot superimposed on left edge of plot graph.

Table 3-4. X-Y Recorder Setup Procedure (Continued)

Step	Procedure	Results
9	On 6600A, rotate MANUAL SWEEP control fully clockwise.	Beam dot on 560A CRT moves from left to right graticule edge.
10	On recorder, press down on pen and ensure that pen is coincident with right edge of plot graph. If pen not aligned with right edge, adjust horizontal Gain (or Sensitivity) control. NOTE If Gain (or Sensitivity) control is adjusted, it may be necessary to recheck adjustment of Offset (or Position) control.	Ink dot superimposed on right edge of plot graph.
11	On 6600A, rotate MANUAL SWEEP control until beam dot is centered on 560A display.	Beam dot centered on 560A CRT.
12	On recorder, adjust vertical (Y) Offset (or Position) control to position pen on reference line for type of measurement being plotted (i.e., top of graph if return loss being plotted or bottom of graph if transmission gain being plotted). Press down on pen and make contact with paper.	Ink dot positioned on reference line of plot graph.
13	If reference line on recorder is positioned at top of graph (return loss), adjust OFFSET control in -10 dBm increments, as indicated on OFFSET dB display, and observe recorder pen movement.	Recorder pen should deflect 1 division for each 10 dBm of OFFSET control movement.
14	If reference line on recorder is positioned at bottom of graph (transmission gain), adjust OFFSET control in +10 dBm increments, as indicated on OFFSET dB display, and observe recorder pen movement.	Recorder pen should deflect 1 division for each 10 dBm of OFFSET control movement.
15	If recorder pen movement not as described in steps 13 or 14, above, adjust recorder vertical Gain (or Sensitivity) control. NOTE If Gain (or Sensitivity) control is adjusted, it may be necessary to recheck adjustment of Offset (or Position control.	N/A

Table 3-4. X-Y Recorder Setup Procedure (Continued)

Step	Procedure	Results
16	On 560A, position rear panel OUTPUT MODE switch to RCDR.	N/A
17	On 6600A, press AUTO button.	N/A
18	On 560A, depress desired Channel A INPUT switch (A, A-R, R).	N/A
	END OF PROCEDURE.	

3-4. OPERATIONAL CHECKOUT

Operational checkout of the Model 560A Scalar Network Analyzer consists of evaluating the operation of front panel controls and verifying the operation of microwave input components (SWR Autotester and RF Detector). Operational checkout requires the use of a sweep generator to provide control voltages and a microwave test signal; refer to paragraph 2-3.2 for sweep generator requirements.

3-4.1 Preliminary Checks

The following steps must be completed before beginning the operational checkout in Table 3-5. These steps include configuring the 560A for proper line voltage, interconnecting the 560A with sweep generator, energizing sweep generator, and positioning the 560A front and rear panel controls.

a. Configure for Line Voltage. Configure the 560A for correct line voltage per paragraph 2-3.1.

b. Interconnect Sweep Generator. Interconnect the 560A to the sweep generator per paragraph 2-3.2.

c. Energize Sweep Generator. Turn on and position sweep generator controls for a 50 ms sweep. Set RF output attenuation control to provide maximum output.

d. Set Controls. Set the 560A front and rear panel controls as follows:

Front Panel

CHANNEL A
- CHANNEL A ON: Not depressed
- INPUT: R
- MEMORY: OFF
- dB PER DIVISION: 10
- REFERENCE dB/dBm: Not depressed
- OFFSET ZERO: Not depressed
- SET (screwdriver pot): Center of range

CHANNEL B
- CHANNEL B ON: Not depressed
- INPUT: R
- MEMORY: OFF
- dB PER DIVISION: 10
- REFERENCE dB/dBm: Not depressed
- OFFSET ZERO: Not depressed
- SET (screwdriver pot.): Center of range

THRESHOLD: OFF (fully CCW until control clicks)
TILT: Center of range
DISPLAY MODE: REAL TIME
POWER: Not depressed

Rear Panel

LOW LEVEL CAL: NORM
OUTPUT MODE: CRT

3-4.2 Operational Checkout and Troubleshooting Procedure

Operational checkout and troubleshooting instructions are presented in Table 3-5.

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers

Step	Control	Procedure	Normal Indication	If Indication Abnormal
1	POWER	Depress. NOTE With both channel ON switches off (not depressed), 560A defaults to Channel A operation.	a. ON indicator lights.	a. If ON indicator does not light but indicators in Steps 1b, c, and d do light, then ON indicator is faulty. If no indicators light, refer to Figure 7-2.
			b. SMOOTHING OFF indicator lights.	b. If MAX or MIN indicators light, A2 PCB Power-On Reset (PON) circuit is faulty. Refer to paragraphs 7-7.13 and 7-7.23.
			c. Channel A dB indicator lights.	c. A1 PCB faulty; refer to paragraph 7-7.1.
			d. Channel A OFFSET dB display lights.	d. A1 PCB faulty; refer to paragraph 7-7.1.
		Channel A Checkout		
2	CHANNEL A ON	Depress.	No change from Step 1.	N/A
3	REFERENCE dB/dBm	Depress.	dB indicator goes out and dBm indicator lights.	A1 PCB faulty. Refer to paragraph 7-7.1.
4	OFFSET	Rotate throughout range, then set control to -30.0	a. OFFSET dB display varies >±65.0 dB.	a. A1 PCB faulty. Refer to paragraph 7-7.1.
			b. Horizontal trace is on the display.	b. Refer to Figure 7-3.

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
5	OFFSET ZERO	Depress.	OFFSET dB indicates ±00.0; trace deflects downward near bottom of CRT or off-screen.	A1 PCB faulty; refer to paragraph 7-7.1.
6	OFFSET ZERO	Depress.	OFFSET dB display indicates -30.0 and trace returns to near center of CRT.	A1 PCB faulty; refer to paragraph 7-7.1.
7	OFFSET	Rotate counterclockwise (CCW) to obtain 00.0 readout on OFFSET dB display.	OFFSET dB indicates ±00.0; trace deflects downward near bottom of CRT or off-screen.	A1 PCB faulty; refer to paragraph 7-7.1.
8	REF POS LOCATE	Depress and hold.	Trace appears on or near center of CRT.	Refer to Figure 7-4.
9	SET potentiometer	Rotate throughout range.	Trace moves vertically on display.	Refer to Figure 7-5.
10	SET potentiometer	Adjust so that trace is centered on display.	Trace is centered on display.	N/A
11	REF POS LOCATE	Release.	Trace deflects downward near bottom of CRT or off-screen.	N/A
12	OFFSET	Rotate clockwise (CW) to obtain -30.0 on OFFSET dB display.	Trace returns to near center of CRT and OFFSET dB display indicates -30.0.	N/A
13	HORIZ START	Check that potentiometer is properly adjusted so that input horizontal sweep ramp starts at 0 volts (paragraph 2-3.3). Determine proper adjustment as follows:	N/A	N/A

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
13	(Cont'd)	a. Observe CRT and rotate START potentiometer CW until left hand trace end begins to move right; stop CW rotation.	N/A	a. If trace-end dot fails to intensify when START is rotated fully CCW or fails to deintensify when START is rotated fully CW, refer to Figure 7-6.
		b. Rotate START potentiometer CCW until trace-end stops moving left and dot begins to intensify; stop CCW rotation.	Trace movement to the left stops on or within 1 minor division from left edge of graticule.	b. If intensified trace-end dot fails to extend to graticule left edge, adjust CRT mainframe HORIZ POSITION potentiometer, refer to paragraph 3-4.3.
14	HORIZ STOP	Check that potentiometer is properly adjusted so that input horizontal sweep ramp stops at 10 volts. Proper adjustment is determined by observing CRT and rotating STOP potentiometer CW until trace movement to the right stops and trace-end dot begins to intensify.	Trace movement to the right stops on or within 1 minor division from right edge of graticule.	Refer to Figure 7-7.
15	None	Check that trace is level.	Trace is level.	Adjust CRT mainframe TRACE ROTATE potentiometer. Refer to paragraph 3-4.3 for adjustment procedure.
16	None	Connect 560-7 series RF Detector between front panel R connector and RF OUTPUT on sweep generator.	Trace deflects approximately 3 divisions upward from centerline.	RF detector, detector connector, or 560A input connector faulty.

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
17	OFFSET	Rotate control CCW to center trace on display.	Trace centered on display.	N/A
18	SLOPE (on sweep generator	Adjust control for a level trace.	Level trace centered on display.	Sweep generator faulty.
19	INPUT A-R	Depress.	a. Trace deflects either near bottom or off CRT. b. dBm indicator begins flashing.	a. N/A b. A2 PCB faulty. Refer to paragraph 7-7.3.
20	INPUT A	Depress.	Trace remains unchanged, but dBm indicator stops flashing.	N/A
21	None	Disconnect RF detector from R connector and connect to A connector.	Trace on or near center of CRT.	Refer to Figure 7-8.
22	SLOPE (on sweep generator)	Rotate fully CW.	Trace on CRT slopes downwards from left to right.	Sweep generator faulty.
23	dB PER DIVISION	Depress each switch in turn and observe that displayed trace changes in slope; leave .5 switch depressed.	Trace changes in slope.	A1 PCB faulty. Refer to paragraph 7-7.1.
24	SLOPE (on sweep generator)	While observing CRT, adjust control for a trace slope of 4 divisions.	Trace slopes 4 divisions downwards from left to right.	N/A
25	STORE TRACE	Depress and release. When red indicator located	Trace as specified in Step 24 appears on CRT.	a. If red LED fails to light, A1 PCB is faulty. Refer

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
25	(Cont'd)	above switch goes out, trace is stored. NOTE The length of time this LED remains lit depends upon sweep speed.		to paragraph 7-7.1. b. If red LED fails to go out, A2 PCB is faulty. Refer to paragraph 7-7.18.
26	None	On sweep generator, position RF output switch to OFF.	Trace disappears from CRT.	Troubleshoot sweep generator.
27	RECALL	Depress.	Trace as specified in Step 24 reappears on CRT and dBm indicator begins flashing.	a. If straight-line trace appears on CRT or if dBm indicator fails to flash, A1 PCB faulty. Refer to paragraph 7-7.1. b. If a trace does not appear on CRT, or if CRT displays random lines, A2 is faulty. Refer to paragraphs 7-7.4, 7-7.5 and 7-7.18.
28	MEMORY OFF	Depress.	Trace disappears from CRT and dBm indicator stops flashing.	N/A
29	None	On sweep generator, position RF output switch to ON.	Trace as specified in Step 24 reappears on CRT.	N/A
30	SUBTRACT	Depress.	Trace changes to straight-line trace and dBm indicator begins flashing.	A1 PCB faulty. Refer to paragraph 7-7.1.

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
31	STORE TRACE	Depress and Release.	Trace as specified in Step 24 reappears on CRT.	A1 PCB faulty. Refer to paragraph 7-7.1.
32	AVG	Depress.	Trace slopes downwards 2 divisions from left to right.	A1 PCB faulty. Refer to paragraph 7-7.1.
33	MEMORY OFF	Depress.	Trace as specified in Step 24 reappears on CRT.	N/A
34	SLOPE (on sweep generator)	While observing CRT, rotate control CCW until trace is level.	Trace is level.	N/A
35	REFERENCE dB/dBm	Depress	a. dBm indicator goes out; dB indicator lights. b. Trace may shift vertically or may disappear entirely.	A1 PCB faulty. Refer to paragraph 7-7.1.
36	ZERO dB SET	Push and turn to to move trace onto display. If trace already present on display, rotate control and verify that trace moves vertically. Increase to 10 dB PER DIVISION as necessary.	Trace moves vertically on CRT.	A1 PCB faulty. Refer to paragraph 7-7.1.
37	ZERO dB SET	Rotate control (push and turn) to center trace on CRT.	Trace centered on CRT.	A1 PCB faulty. Refer to paragraph 7-7.1.
		Channel B Checkout		
38	CHANNEL B ON	Depress.	a. Channel B dB indicator lights. b. Channel B OFFSET dB display lights.	A1 PCB faulty. Refer to paragraph 7-7.1.

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
39	CHANNEL A ON	Depress.	Channel A OFFSET dB display and dB indicator goes out.	N/A
40	REFERENCE dB/dBm	Depress.	dB indicator goes out and dBm indicator lights.	A1 PCB faulty. Refer to paragraph 7-7.1.
41	OFFSET	Rotate throughout range, then leave control set at -30.0.	a. OFFSET dB display varies >±65 dB. b. Horizontal trace is on the display.	a. A1 PCB faulty. Refer to paragraph 7-7.1. b. Refer to Figure 7-9.
42	OFFSET ZERO	Depress.	OFFSET dB display indicates ±00.0; trace deflects downward near bottom of CRT or off-screen.	A1 PCB faulty. Refer to paragraph 7-7.1.
43	OFFSET ZERO	Depress.	OFFSET dB display indicates -30.0 and trace moves back to center of CRT.	A1 PCB faulty. Refer to paragraph 7-7.1.
44	OFFSET	Rotate CCW to obtain +00.0 readout on OFFSET dB display.	OFFSET dB indicates ±00.0; trace deflects downwards near bottom of CRT or off-screen.	A1 PCB faulty. Refer to paragraph 7-7.1.
45	REF POS LOCATE	Depress and hold.	Trace moves to center of CRT.	Refer to Figure 7-10.
46	SET potentiometer	Rotate throughout range.	Trace moves vertically on CRT.	Refer to Figure 7-11.
47	SET potentiometer	Center trace on CRT.	Trace is centered on display.	N/A
48	REF POS LOCATE	Release.	Trace deflects downwards near bottom of CRT or off-screen.	N/A

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
49	OFFSET	Rotate CW to obtain -30.0 on OFFSET dB display.	Trace returns to near center of CRT and OFFSET dB display indicates -30.0.	N/A
50	None	Disconnect RF detector from A connector and connect to R connector.	Trace deflects approximately 3 divsions upwards from centerline.	N/A
51	OFFSET	Rotate control CCW to center trace on CRT.	Leveled trace centered on CRT.	N/A
52	INPUT B-R	Depress.	a. Trace deflects downwards near bottom of CRT or off-screen. b. dBm indicator begins flashing.	N/A
53	INPUT B	Depress.	Trace remains unchanged, but dBm indicator stops flashing.	N/A
54	None	Disconnect RF detector from R connector and connect to B connector.	Trace on or near center of CRT.	Refer to Figure 7-12.
55	SLOPE (on sweep generator)	Rotate fully CW.	Trace on CRT slopes downwards from left to right.	N/A
56	dB PER DIVISION	Depress each switch in turn and observe that displayed trace changes in slope; leave .5 switch depressed.	Trace changes in slope.	A1 PCB faulty. Refer to paragraph 7-7.1.
57	SLOPE (on sweep generator)	While observing CRT, adjust control for a trace slope of 4 divisions.	Trace slopes downwards 4 divisions from left to right.	N/A

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
58	STORE TRACE	Depress and release. When red indicator located directly above switch goes out, trace is stored.	Trace is as specified in Step 57.	a. If red LED fails to light, A1 PCB is faulty. Refer to paragraph 7-7.1. b. If red LED fails to go out, A2 PCB is faulty. Refer to paragraph 7-7.18.
59	None	On sweep generator, position RF output switch to OFF.	Trace disappears from CRT.	N/A
60	RECALL	Depress.	Trace as specified in Step 57 reappears on CRT and dBm indicator begins flashing.	a. If straight-line trace appears on CRT or if dBm indicator fails to flash, A1 PCB faulty. Refer to paragraph 7-7.1. b. If trace does not appear on CRT or if CRT displays random lines, A2 PCB faulty. Refer to paragraphs 7-7.4, 7-7.5 and 7-7.18.
61	MEMORY OFF	Depress.	Trace disappears from CRT and dBm indicator stops flashing.	N/A
62	None	On sweep generator, position RF output switch to ON.	Trace as specified in Step 57 reappears.	N/A
63	SUBTRACT	Depress.	Trace changes to straight-line trace and dBm indicator begins flashing.	A1 PCB faulty. Refer to paragraph 7-7.1.

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
64	STORE TRACE	Depress and Release.	Trace as specified in Step 57 reappears on CRT.	A1 PCB faulty. Refer to paragraph 7-7.1.
65	AVG	Depress.	Trace slopes downwards 2 divisions from left to right.	A1 PCB faulty. Refer to paragraph 7-7.1.
66	MEMORY OFF	Depress.	Trace as specified in Step 57 reappears on CRT.	N/A
67	SLOPE (on sweep generator)	While observing 560A CRT, rotate control CCW until trace is level.	Trace is level.	N/A
68	REFERENCE dB/dBm;	Depress.	a. dBm indicator goes out/ dB indicator lights. b. Trace may shift vertically or it may disappear entirely.	N/A
69	ZERO dB SET	Push and turn to move trace onto display. If trace already present on display, rotate control and verify that trace moves vertically. (Increase to 10 dB PER DIVISION as necessary.)	Trace moves vertically on CRT.	A1 PCB faulty. Refer to paragraph 7-7.1.
70	ZERO dB SET	Rotate control (push and turn) to center trace on CRT.	Trace centered on CRT.	A1 PCB faulty. Refer to paragraph 7-7.1.

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
		Markers, Display Mode, and Smoothing Checkout		
71	None	On sweep generator, position marker control(s) to provide video marker near center of band (on 6600A MARKER AMPLITUDE must be maximum).	N/A	N/A
72	THRESHOLD	a. If WILTRON 6600A series sweeper is used, rotate control CW until video marker appears.	a. Marker pulse positioned near center of trace.	a. Refer to Figure 7-13.
73	TILT	Refer to page 3-5, (9).	Marker tilts ±45°.	A1 PCB or wiring between A1 and A2 faulty.
74	THRESHOLD	Rotate CCW to OFF (detent)	Marker pulse disappears.	N/A
75	REFRESH	Depress.	Real time display replaced by refresh display.	Refer to Figure 7-15.
76	REFRESH HOLD	Depress.	Display freezes and REFRESH HOLD indicator lights.	a. If indicator does not light, A1 PCB faulty. b. If display does not freeze, A2 PCB or wiring between A1 and A2 faulty.

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
77	REFRESH HOLD	Depress.	Refresh display returns and REFRESH HOLD indicator goes out.	N/A
78	X-Y PLOT	Depress. NOTE The data in this step is being read out of memory. Consequently, controls may be changed or input disconnected without affecting the recording of X-Y plot data.	Indicator comes on, display disappears, and intensified dot begins a 30-second sweep from left to right across CRT. At conclusion of sweep, indicator goes out and display returns.	a. If indicator does not light, A1 PCB faulty. Refer to paragraph 7-7.1. b. If indicator lights but no sweep appears, A2 PCB faulty. Refer to paragraph 7-7.22.
79	X-Y PLOT	Depress. After approximately 1 second, depress switch again.	a. X-Y PLOT indicator comes on, display disappears, and intensified dot begins a 30-second sweep across CRT. b. Coincident with second time switch is depressed, X-Y PLOT indicator goes out and display returns.	A2 PCB faulty. Refer to paragraph 7-7.22.
80	CHANNEL A ON	Depress.	Channel A dBm indicator and OFFSET dB display comes on.	
81	None	Disconnect RF detector from B and connect to R.	N/A	N/A
82	Channel A INPUT R	Depress.	Trace appears near center of CRT.	N/A

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
92	(Cont'd)		heard and intensified dot begins Channel A sweep. Channel A is swept (plotted) and then Channel B is swept (plotted). After Channel B sweep (plot), a second click is heard and indicator goes out. c. Real time sweep returns.	
93	CHANNEL A ON	Depress.	a. Channel A dB indicator and OFFSET dB display go out. b. Channel A sweep disappears.	N/A
94	SMOOTHING	Depress control several times and observe that indicators switch between OFF, MIN, and MAX.	Indicators switch between OFF, MIN, and MAX.	Refer to Figure 7-16.
95	SWEEP TIME 6600A	On sweeper, set controls for a 10 ms sweep.	Horizontal sweep on 560A CRT speeds up, display changes from intensified dot to trace.	N/A
96	None	On 560A, observe UNCAL, REDUCE SWEEP SPEED indicator.	UNCAL indicator flashing.	Refer to Figure 7-17.
97	None	On sweeper, rotate sweep VERNIER control CCW until UNCAL indicator goes out.	UNCAL indicator off.	N/A

Table 3-5. Operational Checkout and Troubleshooting Using Front Panel Controls and Potentiometers (Continued)

Step	Control	Procedure	Normal Indication	If Indication Abnormal
		SWR Autotester Checkout		
98	OFFSET	Rotate to position trace on center line of graticule. Record value of OFFSET dB display.	Trace located on center line.	N/A
99	None	Disconnect RF Detector from sweep generator RF OUTPUT connector.	N/A	N/A
100	None	Connect INPUT port of SWR Autotester to sweep generator RF OUTPUT connector.	N/A	N/A
101	None	Connect Channel B RF Detector to TEST PORT of SWR Autotester; output of SWR Autotester may be left disconnected.	Trace appears on display.	N/A
102	OFFSET	Rotate to position trace on center line of graticule. Record value of OFFSET dB display.	Approximately 6.5 dB difference between OFFSET dB value obtained in Step 99 and OFFSET dB value obtained in this step.	SWR Autotester faulty. Refer to paragraph 7-5.1.

3-4.3 CRT Mainframe Horiz Position and Trace Rotate Adjustment Instructions

The HORIZ POSITION and TRACE ROTATE controls are mounted on the front panel. Their adjustment is specified in steps 13 and 15 of Table 3-5. Adjustment instructions are given below.

a. The HORIZ POSITION potentiometer moves the displayed trace horizontally on the CRT. Clockwise (CW) adjustment moves the trace to the right; counter-clockwise (CCW) adjustment moves the trace to the left.

b. The TRACE ROTATE potentiometer adjusts the slope of the displayed trace. The adjustment of the potentiometer moves the trace as shown by the arrows labeled A and B, below. CW adjustment is shown by arrow A, and CCW adjustment is shown by arrow B.

3-5 LOW LEVEL (≤45 dBm) TRIM ADJUSTMENTS

The low-level trim potentiometers are internally mounted and are accessible through holes in the right side panel (Figure 3-13). The potentiometers are used to cancel the effects of thermocouple junctions that exist between the RF detector (or SWR Autotester) and the input to the A or B log amplifier. In normal operation for most low-level measurements using standard 560 microwave components (RF detector of SWR Autotester), the adjustment of the CH A or CH B LOW LEVEL TRIM potentiometers is unnecessary; however, for measurements below approximately -45 dBm, adjustment of the applicable channel's LOW LEVEL TRIM potentiometer can provide increased low-level accuracy. Additionally, the LOW LEVEL TRIM potentiometers are used to ensure accurate low-level measurements when the 560-10BX(-1) cable is used. This cable adapts waveguide or other non-560 type RF detectors (or SWR Autotesters) for use with the 560A.

The test setup for the low-level trim adjustments is shown in Figure 3-14; a procedure for adjusting the CH A and CH B potentiometers is given in Table 3-6. The procedure in Table 3-6 provides the CRT deflection circuits with a calibrated voltage

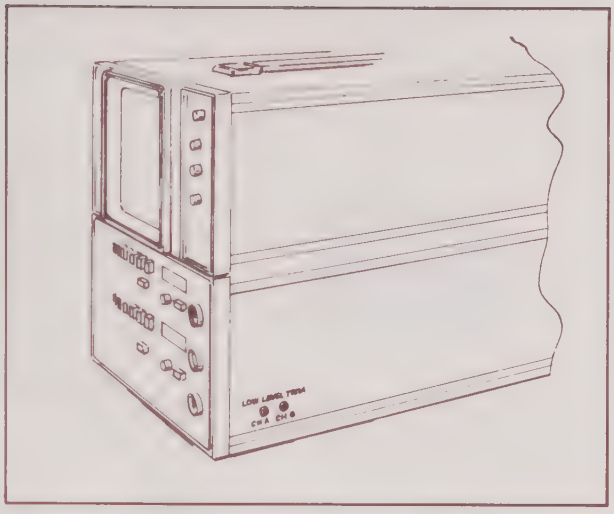


Figure 3-13. Location of Low-Level Trim Potentiometers

from the OFFSET potentiometer that represents the approximate noise floor of the A, B log amplifier. Since no input signal is provided to the A, B log amplifier, the waveform present on the CRT represents the noise level of the first amplifier stage. The CH A or CH B potentiometer is adjusted until the noise level of this amplifier stage is near the noise floor and only random negative clipping occurs. Allow the 560A to warm up for at least 30 minutes before performing the procedure in Table 3-6.

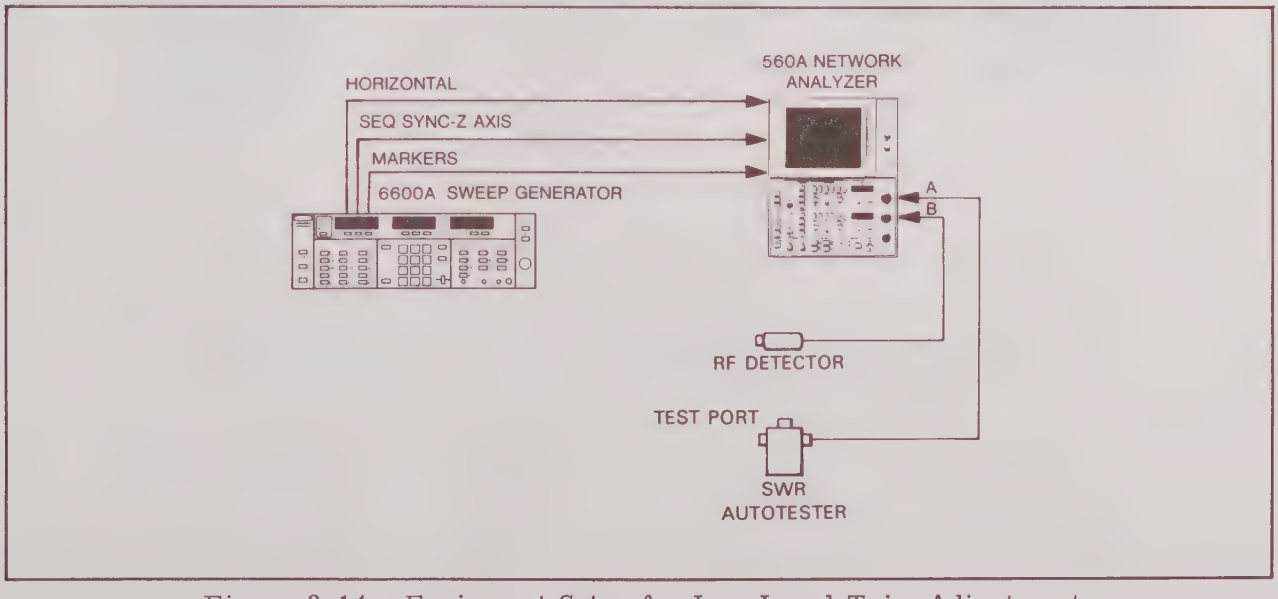


Figure 3-14. Equipment Setup for Low-Level Trim Adjustment

Table 3-6. Channel A and Channel B Low Level Trim Procedure

1. Set up equipment and perform initial switch positioning:

6600A Sweep Generator

POWER: ON
Press RESET.
Press SWEEP TIME and enter 100 ms.
Press F1-F2.

Network Analyzer

CHANNEL A: ON
INPUT: A
MEMORY: OFF
dB PER DIVISION: 1
REFERENCE dB/dBm: Depressed
(dBm indicator lit)
OFFSET ZERO: Not depressed

CHANNEL B: OFF
INPUT: B
MEMORY: OFF
dB PER DIVISION: 1
REFERENCE dB/dBm: Depressed
OFFSET ZERO: Not depressed
THRESHOLD: OFF (fully CCW)
TILT: Center of range
DISPLAY MODE: REFRESH
SMOOTHING: OFF
POWER: ON
LOW LEVEL CAL (rear panel): NORM

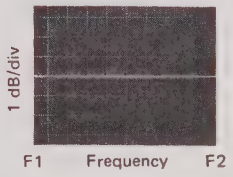
Step	Procedure	Result
2.	Depress and hold Channel A REF POS LOCATE pushbutton switch. Adjust SET potentiometer to position reference line on center graticule line.	
3.	Release REF POS LOCATE.	N/A
4.	Depress SMOOTHING pushbutton switch until MAX indicator lights.	MAX indicator lit.
5.	Adjust Channel A OFFSET control for -58.0 on OFFSET dB display.	OFFSET dB display indicates -58.0.

Table 3-6. Channel A and Channel B Low Level Trim Procedure (Continued)

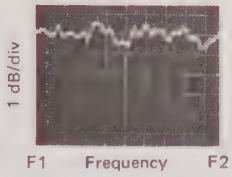
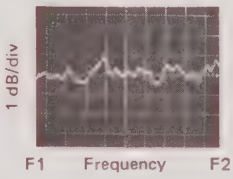
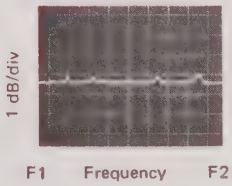
Step	Procedure	Results
6.	A trace similar to one of the three examples shown should appear on the display. If trace is not present, proceed to Step 6A. If trace is present, proceed to Step 7.	EXAMPLE 1  Noise trace with no clipping, but located too far above reference line. EXAMPLE 2  Noise trace with no clipping, located on reference line. EXAMPLE 3  Noise trace with clipping.
6A.	Increase dB PER DIVISION switch-bank until trace appears on screen. Adjust CH A potentiometer clockwise to position trace on centerline.. Return dB PER DIVISION switch-bank setting to 1. Proceed to Step 7.	N/A

Table 3-6. Channel A and Channel B Low Level Trim Procedure (Continued)

Step	Procedure	Results
7.	If trace is being clipped (Example 3 in Step 6), adjust CH A potentiometer counterclockwise until clipping just ceases. If trace is not being clipped (Examples 1 and 2 in Step 6), adjust CH A potentiometer clockwise until clipping just starts; back potentiometer off until clipping just ceases.	Trace containing noise with no clipping appears on or near -58 dB reference line (Example 2 in Step 6).
8.	Depress CHANNEL B ON pushbutton switch.	Channel B dBm indicator and OFFSET dB display light.
9.	Depress CHANNEL A ON pushbutton switch.	Channel A dBm indicator and OFFSET dB display go out.
10.	Repeat steps 2, 3, and 5 through 7 for Channel B.	

3-6 560-10BX OR -10BX-1 CABLE

The 560-10BX cable permits the 560A to be used with detectors other than the 560-7 and 560-71 series and with SWR Autotesters other than the 560-97, -98, and -6 series; specifically, the cable allows the 560A to be used with all types of waveguide detectors and with other SWR Autotesters, e.g. the Series -97, -98, and -63. The 560-10BX-1 cable allows the 560A to be used with a high-impedance diode detector. Before making measurements using this cable, it is necessary to adjust the applicable CH A or CH B LOW LEVEL TRIM side panel potentiometer. To perform this adjustment, connect the 560-10BX or -10BX-1 cable between the 560A A or B connector and the RF detector; leave the RF detector unconnected from the source and perform the low-level trim procedure in Table 3-6.

NOTE

When making measurements using the 560-10BX or -10BX-1 cable, there are two factors that should be considered. Because the 560 microwave components and 560A network analyzer are interdependent, the accuracy of absolute power (dBm) and low-level power (<-40 dBm) measurements made with the 560-10BX or -10BX-1 cable cannot be specified. Consequently, all measurements should be made with the 560A REFERENCE dB/dBm switch in the dB position, and transmission or return loss measurements below approximately -40 dBm should not be attempted.

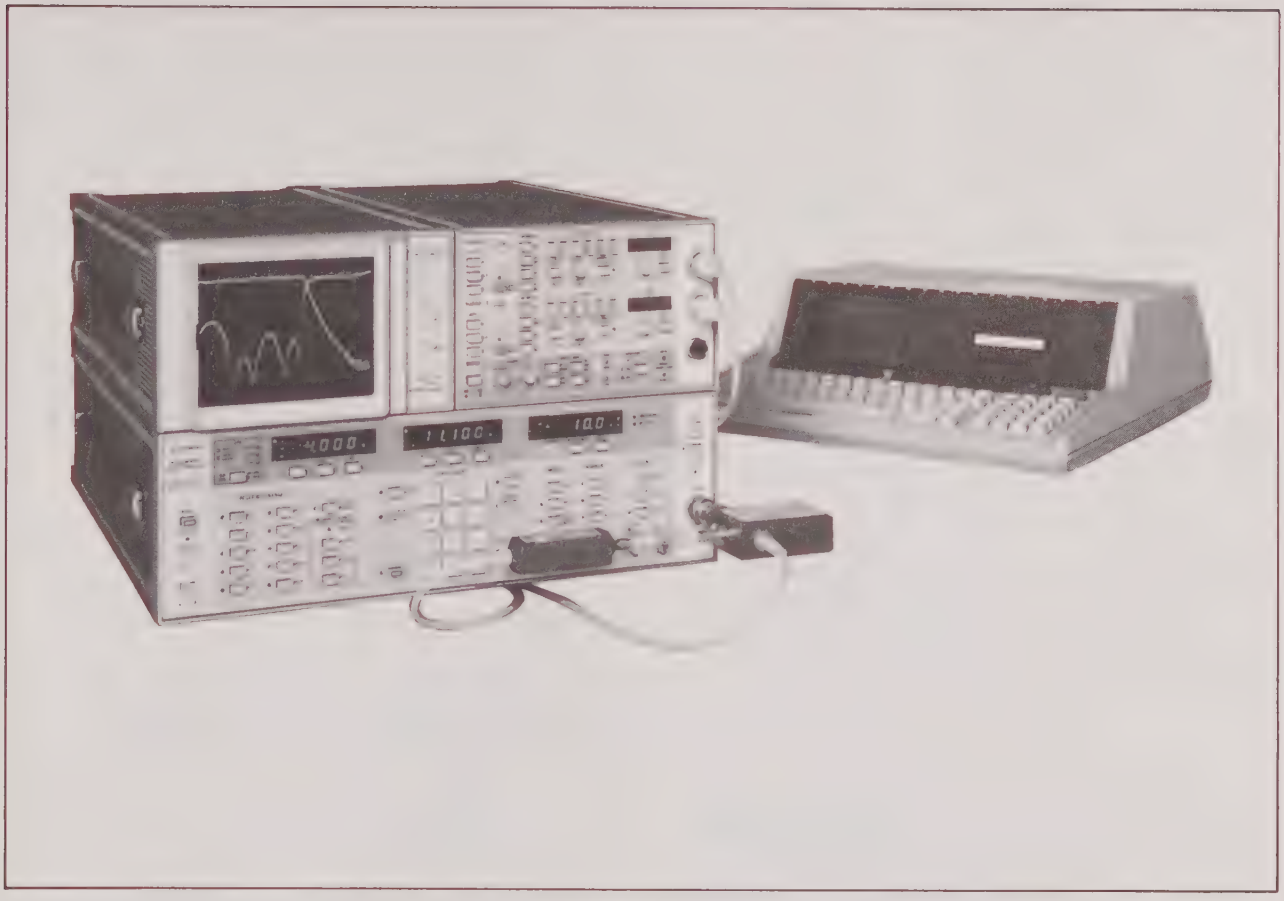


Figure 3-15. Typical GPIB Equipment Setup

3-7 GPIB OPERATION (OPTION 3)

A typical GPIB equipment setup consists of a WILTRON Model 560A/Option 3 Scalar Network Analyzer, a Model 6647A/Option 3 Programmable Sweep Generator, and a Model 85 Controller (Figure 3-15). In a measurement setup of this type, the 560A is capable of providing automated microwave transmission and return loss measurements. GPIB operation for the 560A is described in the following paragraphs.

3-7.1 General Information and Description of Model 560A GPIB Command Codes

The Model 560A is used on the interface bus as both a listener and a talker. When addressed to listen, the 560A can be commanded to collect measurement data and to make that data available to the bus. When addressed to talk, the data which has been collected is sent over the bus to all listeners. Also, in a semi-automatic bus operation, the 560A can be programmed to furnish data to an analog, non-GPIB X-Y plotter.

Interconnection to the GPIB is shown in Figure 3-16. Except for the output connection labeled DISPLAY (used during AD, BD modes only -- see subparagraph a below), the GPIB Interface Circuit Board is connected to the outputs of the channel-amplifiers and the subtract circuit. With connection made at these points, except for POWER, none of the Model 560A front panel controls (MEMORY, dB PER DIVISION, DISPLAY MODE, etc.) have any effect on bus opera-

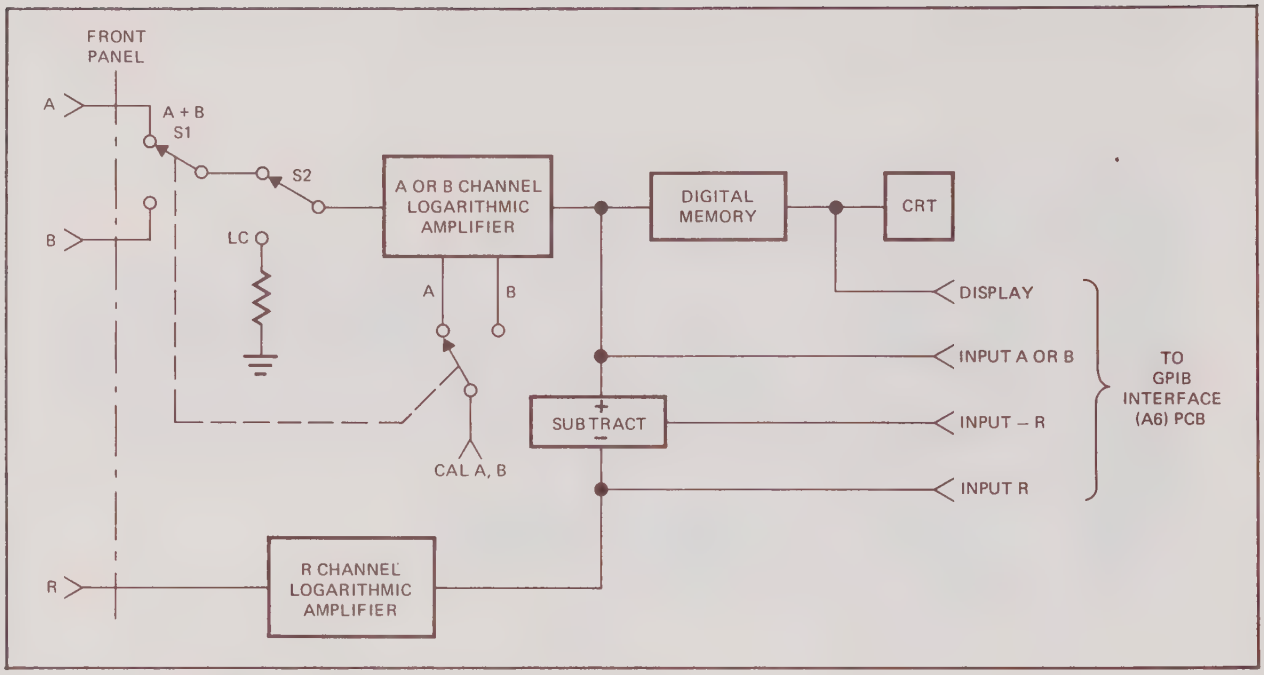


Figure 3-16. Simplified Block Diagram Showing GPIB Interconnection

tion. Measurement data is detected by the applicable microwave input device (RF detector of SWR Autotester), amplified, and applied directly to analog-to-digital converters located on the 560A GPIB Interface Circuit Board.

Control over the Model 560A bus operations is provided through the use of twenty 2-character command codes. These command codes are categorized into four functional groups, plus two miscellaneous commands. The four command groups are data, calibrate, smoothing, and mode. The two miscellaneous commands are XY (initiate X-Y plot) and RL (return to local). Command codes are described below.

a. Data Commands. Data commands are used to direct the 560A to collect and condition (digitize) data for transmission over the bus. Data commands consist of input commands, input minus reference commands, display commands, and a special noise level (NL) command that is used to obtain a readout of the selected amplifier's internal noise level (noise floor). Descriptions of these commands follow:

1. Input commands AI, BI, and RI provide for collection of input data from A Channel, B Channel, and R Channel, respectively. These codes command the 560A to (1) collect analog data from the respective A, B, or R Channel log amplifier, (2) convert the analog data collected into a 7-bit ASCII format, and (3) hold the ASCII binary data until addressed to talk. To see how this multilevel task is accomplished, refer to Figure 3-16 while reading the following description.

   When either an AI or BI command is received, S1 connects the appropriate front panel channel connector (A, B) to the input of the A or B Channel log amplifier; at the same time, the input line INPUT A or B is connected to the GPIB Interface Board A/D Converter input. When RI is received, the input line INPUT R is connected to the GPIB Interface

Board A/D Converter input (amplifier input is always connected to front panel connector). The analog data from the applicable log amplifier is then routed to the GPIB Interface Circuit Board, where it is converted to ASCII data and held for later transmission over the bus. Transmission of the data does not occur until the 560A is addressed to talk.

2. The input-minus-reference commands, AR and BR, provide for collection of A-R and B-R data, respectively. Circuit operations are similar to those described for the input commands. The main difference between operation in these modes and operation in the input modes is the point from which the circuit output is taken. As shown in Figure 3-16, the circuit output is taken from the Subtract circuit; this circuit contains the difference signal when the selected A or B Channel output signal is subtracted by the R Channel output signal.

3. Display commands AD and BD provide for the collection of CRT vertical deflection data from Channel A and Channel B, respectively. As the CRT horizontal frequency data sweeps across the screen, the point at which an AD or BD command is received determines the frequency at which vertical data is supplied to the bus. This vertical data is supplied to the bus in a 160-unit format, with 80 units displayed on-screen and 80 units off-screen in an area known as overrange deflection. An oscillograph relating the CRT screen to this 160-unit digital readout format, plus a narrative describing how to interpret this format, are presented in Figure 3-17. For the display commands to be used, however, the following 560A front panel controls must be positioned as indicated below:

AD command - CHANNEL A ON, depressed

CHANNEL B ON, not depressed

REAL TIME, depressed.

BD command - CHANNEL A ON, not depressed

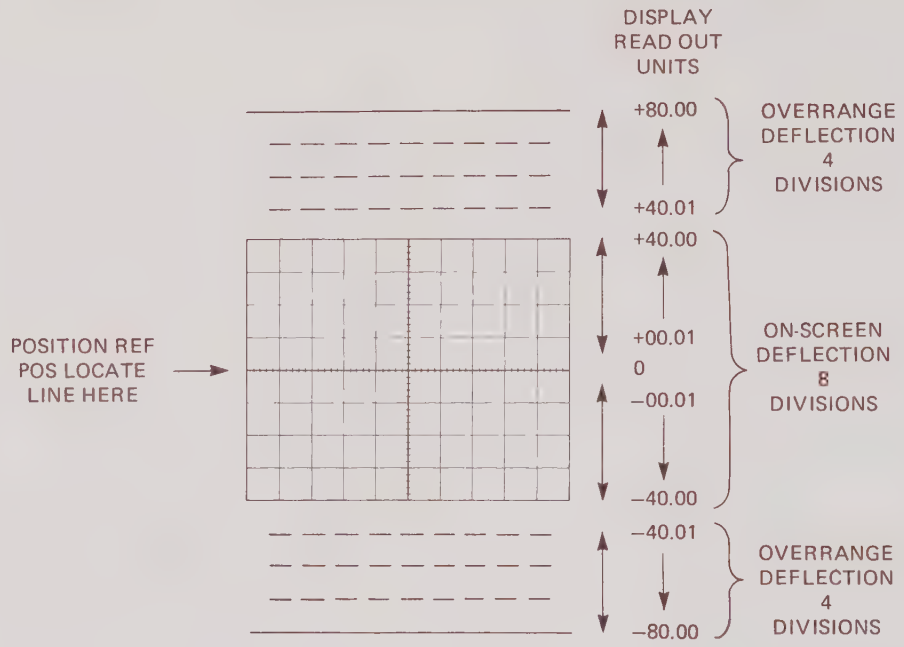
CHANNEL B ON, depressed

REAL TIME, depressed

4. Noise level command NL provides for measurement, in dBm, of the A, B Channel log amplifier's internal noise level (noise floor). During measurements, this command can be used to determine the 560A's actual sensitivity. Although sensitivity is specified at -50 dBm, the 560A is often usable to -55 dBm or less.

b. Calibrate Commands. Calibrate commands are used to correct for thermal drift within the A, B Channel log amplifier. Under local (non-GPIB) control, thermal drift is compensated for during sweep generator retrace. Under GPIB control, however, thermal compensation has to be programmed. Programming is accomplished through the use of calibrate commands. Calibrate commands consist of local calibrate (LC), external calibrate (EC), and channel select (CA, CB) commands. To provide optimum amplifier accuracy, calibrate command LC or EC should be programmed for bus transmission each time the 560A is turned on and again prior to each series of measurements. Before sending a calibrate command, however, the desired channel (A or B) must be selected. Channel selection is accomplished either by sending a channel select command such as CA or CB, or by sending a data command such as AI, BI, RI, AR, BR, AD or BD. The calibrate commands are described below.

1. Local calibrate command LC provides



The CRT display range includes screen and eight divisions of overrange deflection. As shown above, this display range is organized into a 160-unit format. The 80.00 units preceded by the positive (+) sign are allocated to the top half of the display range, and the 80.00 units preceded with the minus (—) sign are allocated to the bottom half of the display range. Since these units are fixed with reference to the CRT centerline graticule, the 560A vertical deflection system should also be referenced to the centerline. This can be accomplished by positioning the REF POS LOCATE reference line on the centering graticule (see oscillograph above).

With the 560A vertical display data referenced to the centerline, the digitized readout that results from a display command can be converted into the input signal's absolute value, in dBm. To effect this conversion, however, the values of the dB PER DIVISION switch bank and the OFFSET dB display must be known. Also, the REFERENCE dB/dBm switch must be in the dBm position (pushbutton switch depressed.) The formula for accomplishing data conversion is shown below.

$$\left(\frac{\text{Readout Digit}}{10} \times \text{dB/DIV}\right) + \text{OFFSET} = \text{dBm}$$

Where Readout Digit refers to the four-digit computer readout, including algebraic sign and decimal point.

dB/DIV refers to the value of the dB PER DIVISION switch bank.

OFFSET refers to the value of the OFFSET dB LED display.

Example: Assume computer Readout Digit equals +20.10; dB PER DIVISION switch bank equals .5 (.5 pushbutton switch depressed), and OFFSET dB display equals +10.2.

$$\left(\frac{+20.10}{10} \times 0.5\right) + +10.2 = +11.2\ \text{dBm}$$

Figure 3-17. Digitized Display Resulting from Display Command (AD or BD), and Example Showing Conversion of Readout Digits to True Measurement Value

thermal compensation for the A, B Channel log amplifier with no signal present and with the amplifier input grounded. To see the circuit operation, refer to Figure 3-16. When the LC command is received, switch S2 momentarily grounds the A or B Channel log amplifier input; the CAL A, B signal causes thermal compensation to be affected.

2. External calibrate command EC provides thermal compensation for the A, B Channel log amplifier when the amplifier input is connected to its microwave input device (RF detector or SWR Autotester). This command provides better thermal compensation than LC does; however, sweep generator RF must be off (<-60 dBm) for this command to be effective. Circuit operation for EC is the same as described for LC, except that switch S2 is not affected and remains connected, as shown in Figure 3-16.

3. Channel select commands CA and CB provide channel-switching only. In the absence of a data command, these two commands select the channel to which the calibrate signal will be applied. As shown in Figure 3-16, channel input switch S1 is "ganged" with the CAL A, B switch. When a CA or CB command is received, it causes these two switches to switch to their A or B positions, respectively. The CAL A, B switch is used to apply the calibrate signal to the appropriate amplifier; S1 is used to connect the appropriate channel connector to the amplifier unit.

c. Smoothing Commands. Smoothing commands provide for A, B Channel log amplifier smoothing. The three smoothing commands SØ, S1, and S2 correspond to the OFF, MIN, and MAX positions of the front panel SMOOTHING switch. Amplifier smoothing operations caused by these commands are identical to those caused by the SMOOTHING switch. These operations are described in paragraph 3-3.6.

Although the smoothing process is the same for both local and bus operation, there is an inherent log amplifier characteristic that affects smoothing during bus operation. This characteristic determines the amount of time required for the log amplifier to process input signals with rapidly-changing power levels, such as those seen when measuring the transmission or return loss of an electronic filter. (A filter can cause a power change of 50 or 60 dB when the frequency sweep crosses the bandpass/reject crossover point.) The worst-case (power change from +16 to -55 dBm) time required for log amplification is 12 ms for normal smoothing (SØ), 40 ms for minimum smoothing (S1), and 200 ms for maximum smoothing (S2).

For local (non-GPIB) operation, these times are not significant. For GPIB operation, however, these times are very significant because overall GPIB operational speed is affected. Remember, because of the asynchronous three-wire handshake process, the speed of GPIB operations is determined by the speed with which the slowest instrument can process data. Consequently, the delay in the 560A between the time a measurement starts and the time data is available for bus transmission affects overall GPIB speed.

Three methods of reducing this delay time have been devised. The first method, using hardware to determine which level of smoothing has been selected, is described later in this paragraph. The other two methods, interrupt mode and fast mode, are described in subparagraph d.

The method of using hardware to determine which level of smoothing has been selected is represented in the flowchart in Figure 3-18. This flowcharted routine is initiated by receipt of one of the data commands (AI, BI, RI, AR,

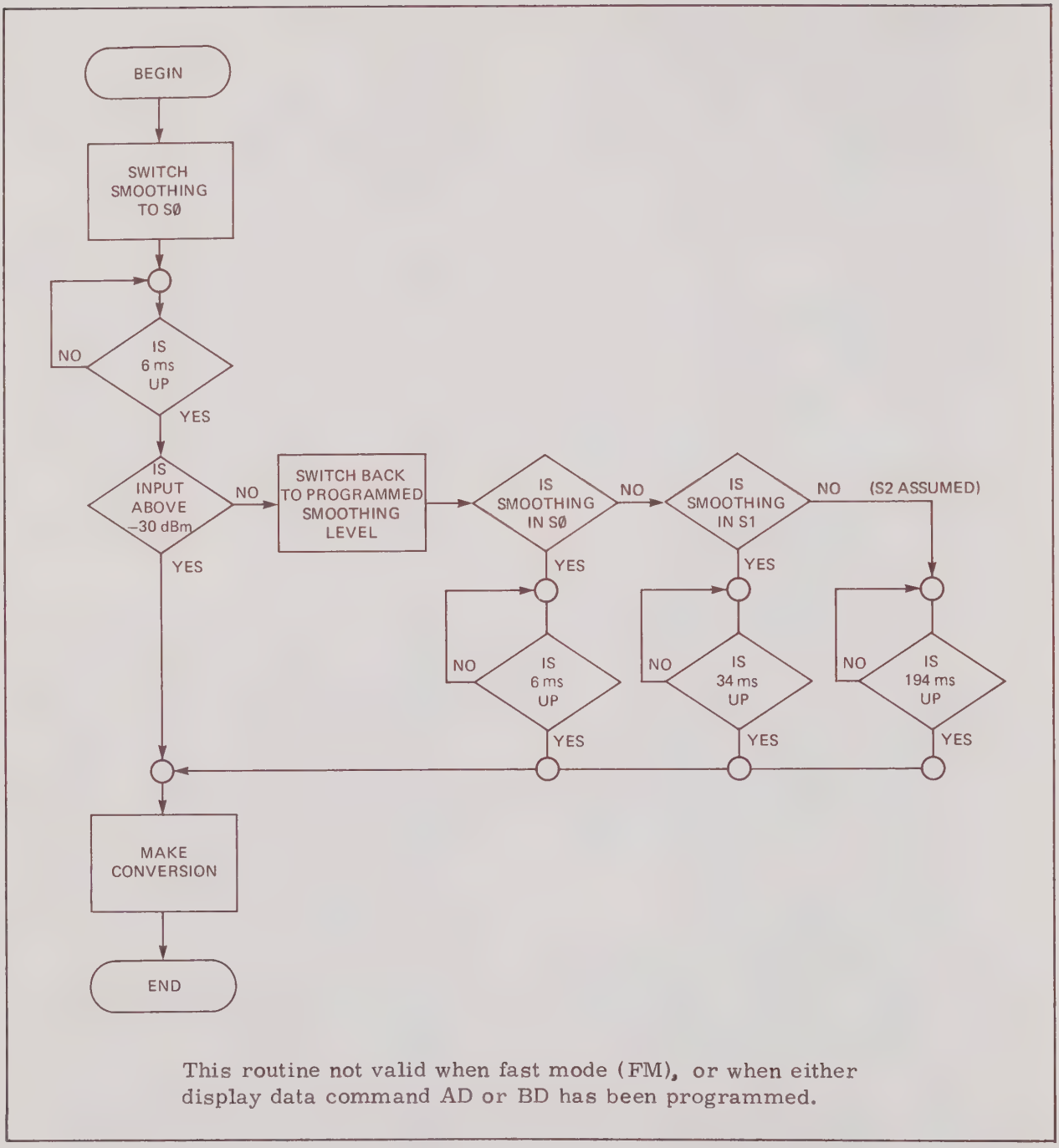


Figure 3-18. Flowchart Showing Smoothing Command Operation

BR, AD, BD, or NL). The routine starts off by switching smoothing to SØ and waiting 6 ms for the input data to settle. After this 6 ms delay, the routine determines whether the input signal is above or below -30 dBm. If above -30 dBm (i.e., +16 to -30), no further settling time is required and the input analog signal is converted to ASCII data bytes and made available for bus transmission. If, however, the input signal is determined to be below -30 dBm, more settling time is required before data conversion. The amount of additional settling time required depends on the level of smoothing programmed. If SØ is programmed, an additional 6 ms is required. If S1 is programmed, an additional 34 ms is required. If S2 is programmed, an additional 194 ms is required. The result of this overall routine is: for input power levels above -30 dBm, overall settling time is 6 ms regardless of which smoothing level is programmed; for input power levels below -30 dBm, overall settling time is 12 ms for SØ, 40 ms for S1, and 200 ms for S2. The GPIB operator can see the results of this routine's logical decision processes by observing the front panel SMOOTHING OFF, MIN, and MAX indicator LED's. These LED's change as the routine runs its course.

d. Mode Commands. Mode commands provide alternate methods of data conversion and data handling. These commands consist of hold mode (HM), interrupt mode (IM), and fast mode (FM). The HM, IM, and FM modes provide, respectively, normal data conversion with its up to 200 ms amplifier settling time requirement, normal conversion but with more efficient data handling using the SRQ management bus control line, and fast (immediate) data conversion. These three modes are described below.

1. Hold mode command HM provides for data conversion in the normal (up to 200 ms delay) mode. Upon receipt of a data command (AI, BI, RI, AR, BR, AD, or BD), the 560A initiates the flowcharted process shown in Figure 3-18. If the 560A is addressed to talk before the flowcharted process has run its course, GPIB handshake is inhibited until data conversion is complete. This is the easiest and least complex mode for which to program. Also, this is the default mode of operation. Each time power is applied, the 560A comes on line in this mode.

2. Interrupt mode command IM also uses the flowcharted process of Figure 3-18 for data conversion. However, in this mode, instead of delaying bus operation by holding up the handshake when addressed to talk, the Service Request (SRQ) control line is used. This line is set TRUE (low) to indicate an instrument needs service. When the controller senses that SRQ is TRUE, it sets ATN TRUE and sends a serial poll enable message to all instruments. When the 560A receives this message, it responds when next addressed to talk with an appropriately-coded Status Byte (STB). The status byte and request service bit are shown in Figure 3-19.

3. Fast mode command FM provides for data conversion without waiting for

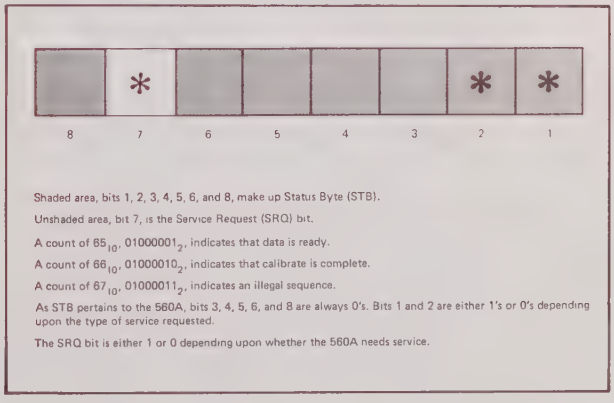

*
*
*
8
7
6
5
4
3
2
1
Shaded area, bits 1, 2, 3, 4, 5, 6, and 8, make up Status Byte (STB).
Unshaded area, bit 7, is the Service Request (SRQ) bit.
A count of 65_{10}, 01000001_2, indicates that data is ready.
A count of 66_{10}, 01000010_2, indicates that calibrate is complete.
A count of 67_{10}, 01000011_2, indicates an illegal sequence.
As STB pertains to the 560A, bits 3, 4, 5, 6, and 8 are always 0's. Bits 1 and 2 are either 1's or 0's depending upon the type of service requested.
The SRQ bit is either 1 or 0 depending upon whether the 560A needs service.

Figure 3-19. Request Service Bit and Status Byte

the normal, up to 200 ms, log amplifier delay (settling time). In this mode, the 560A completes data conversion immediately upon receipt of a data command. This mode provides for very rapid data transactions and it can be used to advantage in "averaging" algorithms. This mode should be used with care, however. Since it does not allow for amplifier settling, measurement data obtained using the fast mode could contain errors if used incorrectly.

e. Miscellaneous Commands. Miscellaneous commands XY and RL are used to control auxiliary GPIB functions. These two commands are described below.

1. The XY command is used to initiate an X-Y plot when a non-GPIB X-Y plotter is connected to rear panel connectors. The operation that this command controls is semi-automatic, in that manipulation of front panel controls is necessary to obtain a proper CRT display. When this command is sent over the bus, it serves the same function as physically depressing the front panel X-Y PLOT pushbutton switch. Operation of the X-Y pushbutton switch is described in paragraph 3-3.5. (An X-Y plot can also be initiated from the front panel while under GPIB control.)

2. The RL command is used to return the 560A to local (front panel) control.

3-7.2 Summary of GPIB Command Codes

To provide quick reference to GPIB command codes, a summary description of each code is provided in Table 3-7. Also, each code contains reference to the paragraph in text where the command is fully described.

3-7.3 Data Output Format

When addressed to talk, the 560A transmits ASCII coded data to the bus in the following format: +DD.DD CR(LF). In this format, the letter "D" stands for digit; the letters CR(LF) are abbreviations for carriage return and line feed, respectively. The LF abbreviation is set off in parentheses because the ASCII character for line feed may not be transmitted; this character can be inhibited by the rear panel CR-CR/LF switch. When this switch is in the CR position, the line feed character is inhibited. Conversely, when the switch is in the CR/LF position, the line feed character is sent over the bus. This format produces a controller readout similar to the following example: +18.12. An explanation of the +DD.DD CR(LF) format is shown below.

- Sign (+/-) character
- Most significant measurement digit
- Next most significant measurement digit
- Decimal point
- Next least significant measurement digit
- Least significant measurement digit
- Least significant measurement digit
- Carriage return character (CR)
- Line feed character (LF)

3-7.4 Sample Program in HPL Computer Language for HP 9825A Programmable Calculator

A sample program in HPL that exercises most of the 560A GPIB functions is presented in Figure 3-20. This program is intended for use with a GPIB system that uses an HP 9825A Programmable Calculator as system controller.

3-7.5 Sample Program in BASIC Computer Language for Commodore PET 2001 Controller

A sample program in BASIC that exercises most of the 560A GPIB functions is presented in Figure 3-21. This program is intended for use with a GPIB system that uses a Commodore PET 2001 as system controller.

3-7.6 Sample Program in BASIC Computer Language for HP 85 Controller

A sample program in BASIC that exercises most of the 560A GPIB functions is presented in Figure 3-22. This program is intended for use with a GPIB system that uses an HP 85 as system controller.

Table 3-7. Summary of GPIB Command Codes

Command Code	Name	Function
AI	A Channel Input	Connects A Channel to bus; returns data in dBm. See paragraph 3-7.1, a, 1 for description.
BI	B Channel Input	Connects B Channel to bus; returns data in dBm. See paragraph 3-7.1, a, 1.
RI	R Channel Input	Connects R Channel to bus; returns data in dBm. See paragraph 3-7.1, a, 1.
AR	A Channel minus R Channel	Connects A-R to bus; return data proportional to the dB difference between A Channel and R Channel. See paragraph 3-7.1, a, 2.
BR	B Channel minus R Channel	Connects B-R to bus; returns data proportional to the dB difference between B Channel and R Channel. See paragraph 3-7.1, a, 2.
AD	A Channel Display	Connects A Channel CRT display to bus. Returns data in a $\pm$80.00-unit format. See paragraph 3-7.1, a, 3.
BD	B Channel Display	Connects B Channel CRT display to bus. Returns data in a $\pm$80.00-unit format. See paragraph 3-7.1, a, 3.
NL	Noise Level	Returns data, in dBm, of A, B Channel log amplifier noise floor. See paragraph 3-7, 1, a, 4.
LC	Local Calibrate	Connects input of A, B Channel log amplifier to ground and compensates thermal drift. Desired channel must first be selected using either AI, BI, BR, CA, or CB. See paragraph 3-7.1, b, 1.
EC	External Calibrate	Compensates A, B Channel log amplifier drift with microwave input components connected to amplifier input. Sweep generator RF must be off (<-60 dBm). Desired channel must first be selected (see above). See paragraph 3-7.1, b, 2.

Table 3-7. Summary of GPIB Command Codes (Continued)

Command Code	Name	Function
CA	A Channel Select	Connects A Channel to bus. See paragraph 3-7.1, b, 3.
CB	B Channel Select	Connects B Channel to bus. See paragraph 3-7.1, b, 3.
SØ	Smoothing Off	Provides for minimal smoothing. See paragraph 3-7.1, c.
S1	Smoothing Minimum	Provides for first level (MIN) smoothing when input signal is below -30 dBm. See paragraph 3-7.1, c.
S2	Smoothing Maximum	Provides for second level (MAX) smoothing when input signal is below -40 dBm. See paragraph 3-7.1, c.
HM	Hold Mode	Provides for amplifier settling times of up to 200 ms before allowing data conversion and GPIB handshake. See paragraph 3-7.1, d, 1.
IM	Interrupt Mode	Provides for more efficient data handling using GPIB SRQ function. Data conversion is handled normally, but handshake is completed immediately upon receipt of data command. See paragraph 3-7.1, d, 2.
FM	Fast Mode	Enables immediate data conversion and GPIB handshake. Extremely fast method for data transaction; however, because amplifier settling time is not provided, measurement errors may be introduced. See paragraph 3-7.1, d, 3.
XY	Plot	Initiates X-Y plot when non-GPIB plotter is connected to rear panel jacks. See paragraph 3-7.1, e, 1.
RL	Return to Local	Returns 560A to local (front panel) control. See paragraph 3-7.1, e, 2.

```
0: ent "ENTER 560 ADDRESS",A;700+A)A
1: dev "560",A;dim A$[32]
2: wrt "560","CALC";prt "CA LC"
3: wrt "560","CBLC";prt "CB LC"
4: wrt "560","CANL";red "560",A$;prt "CA NL= ",A$
5: wrt "560","CBNL";red "560",A$;prt "CB NL= ",A$
6: wrt "560","AI";red "560",A$;prt "A INPUT= ",A$
7: wrt "560","BI";red "560",A$;prt "B INPUT= ",A$
8: wrt "560","RI";red "560",A$;prt "R INPUT= ",A$
9: wrt "560","AR";red "560",A$;prt "A-R= ",A$
10: wrt "560","BR";red "560",A$;prt "B-R= ",A$
11: wrt "560","AD";red "560",A$;prt "A DISP= ",A$
12: wrt "560","BD";red "560",A$;prt "B DISP= ",A$
```

Figure 3-20. Sample Program in HPL for HP 9825A Controller Exercising 560A GPIB Functions

```
200 OPEN6,6
210 PRINT"CA LC"
220 PRINT#6,"CALC"
230 PRINT"CB LC"
240 PRINT#6,"CBLC"
250 PRINT#6,"CANL"
260 INPUT#6,B$
270 PRINT"CA NL = ";B$
280 PRINT#6,"CBNL"
290 INPUT#6,B$
300 PRINT"CB NL = ";B$
310 PRINT#6,"AI"
320 INPUT#6,B$
330 PRINT"A INPUT = ";B$
340 PRINT#6,"BI"
350 INPUT#6,B$
360 PRINT"B INPUT = ";B$
370 PRINT#6,"RI"
380 INPUT#6,B$
390 PRINT"R INPUT = ";B$
400 PRINT#6,"AR"
410 INPUT#6,B$
420 PRINT"A-R = ";B$
430 PRINT#6,"BR"
440 INPUT#6,B$
450 PRINT"B-R = ";B$
460 PRINT#6,"AD"
470 INPUT#6,B$
480 PRINT"A DISP =";B$
490 PRINT#6,"BD"
500 INPUT#6,B$
510 PRINT"B DISP = ";B$
520 PRINT#6,"S1";FOR J=1TO200;NEXTJ
530 PRINT#6,"S2";FORJ=1TO200;NEXTJ
540 PRINT#6,"S0";FORJ=1TO200;NEXTJ;GOTO520
```

Figure 3-21. Sample Program in BASIC for Commodore PET 2001 Controller Exercising 560A GPIB Functions

```
 10 ! 560TST
 20 PRINT USING 30
 30 IMAGE 5/,"WILTRON MODEL 560
    SCALAR NETWORKANALYZER GPIB
    FUNCTION EXERCISER",5/
 40 OUTPUT 706 ;"CALC"
 50 PRINT USING 60
 60 IMAGE 2/,"CHANNEL A CAL COMP
    LETE",2/
 70 OUTPUT 706 ;"CBLC"
 80 PRINT USING 90
 90 IMAGE "CHANNEL B CAL COMPLET
    E",2/
100 OUTPUT 706 ;"S2CANL"
110 ENTER 706 ; N1
120 PRINT USING 130 ; N1
130 IMAGE "CH. A NOISE LEVEL= ",
    S2D.D," dBM",2/
140 OUTPUT 706 ;"S2CBNL"
150 ENTER 706 ; N2
160 PRINT USING 170 ; N2
170 IMAGE "CH. B NOISE LEVEL= ",
    S2D.D," dBM",2/
180 OUTPUT 706 ;"S0"
190 OUTPUT 706 ;"HMAI"
200 ENTER 706 ; A
210 OUTPUT 706 ;"HMBI"
220 ENTER 706 ; B
230 OUTPUT 706 ;"HMRI"
240 ENTER 706 ; R
250 PRINT USING 260
260 IMAGE "A INPUT",5X,"B INPUT"
    ,5X,"R INPUT",/,2X,"dBM",9X,
    "dBM",9X,"dBM",/
270 PRINT USING 280 ; A,B,R
280 IMAGE X,S2D.D,7X,S2D.D,7X,S2
    D.D,2/
290 OUTPUT 706 ;"HMAR"
300 ENTER 706 ; A1
310 OUTPUT 706 ;"HMBR"
320 ENTER 706 ; B1
330 PRINT USING 340
340 IMAGE 9X,"A-R,",6X,"B-R,",/,
    10X,"dB",8X,"dB",/
350 PRINT USING 360 ; A1,B1
360 IMAGE 8X,S2D.D,5X,S2D.D,2/
370 CLEAR
380 DISP USING 390
390 IMAGE 2/,"PLACE 560 IN REAL
    TIME MODE",2/,"PRESS CONTINU
    E WHEN READY"
400 BEEP 100,60
410 PAUSE
420 CLEAR
430 OUTPUT 706 ;"CAAD"
440 ENTER 706 ; A2
450 OUTPUT 706 ;"CBBD"
460 ENTER 706 ; B2
470 PRINT USING 480
480 IMAGE 9X,"A DISP",5X,"B DISP
    ",/
490 PRINT USING 500 ; A2,B2
500 IMAGE 9X,S2Z.2D,5X,S2Z.2D,4/
510 OUTPUT 706 ;"RL"
520 PRINT USING 530
530 IMAGE "560 GPIB EXERCISE COM
    PLETE",2/,"PLACE 560 IN REFR
    ESH MODE",5/
540 END
```

Figure 3-22. Sample Program in BASIC for HP 85 Controller Exercising 560A GPIB Functions

3-8. ALTERNATING-SWEEP OPERATION

Alternating-sweep capability allows the 560A to process and then display two swept-frequency ranges with only one RF detector connected to the Channel A input. A sweep generator with alternating-sweep capability, such as the WILTRON 6600A Series Programmable Sweep Generator, must be connected to the rear panel AUX I/O connector for the 560A to display simultaneously one swept-frequency range on Channel A and the other swept-frequency range on Channel B. In the alternating-sweep mode, the front panel Channel A and Channel B display controls independently adjust each display trace.

SECTION IV
PERFORMANCE VERIFICATION

4-1 INTRODUCTION

This section provides performance verification philosophy and procedures for the Model 560A Scalar Network Analyzer. Also included is a listing of recommended test equipment.

4-2 RECOMMENDED TEST EQUIPMENT

Performance verification for the 560A can be accomplished using a minimum of test equipment. Table 4-1 provides a listing. If recommended test equipment items are not available, however, equipment with equivalent characteristics may be substituted.

4-3 PERFORMANCE VERIFICATION

The philosophy pertaining to 560A performance verification and the detailed instructions for accomplishing this verification are provided in the following paragraphs.

4-3.1 Performance Verification Philosophy

The 560A performance verification tests verify that the 560A Front Panel (A1), Digital (A2), Power Supply (A4), Interface Control (A8), and optional GPIB Interface (A6) PCB circuits are performing properly, and that the Log Amplifier (A3) PCB circuits are within specified limits for absolute power measurements. These performance tests are verified from the front panel; no internal circuits or controls other than the A3 PCB TEST-NORMAL switch are disturbed. Each performance test contains instructions that, in most cases, direct the reader to Section V for the applicable adjustment procedure, should the test fail. In cases where no adjustments are applicable, the reader is told which PCB is faulty. If all of the tests in paragraph 4-3.2 are within their specified tolerances, the 560A requires no calibration and none should be attempted.

4-3.2 Performance Verification Procedure

The procedure for verifying 560A performance is given below. This entire procedure is intended to be accomplished from start to finish; no break-in points are provided. The performance verification tests require the use of a sweep generator to provide the proper operational signals, and markers.

The radio frequency at which performance verification testing is conducted is 50 MHz. In the front panel and digital PCB tests, this frequency is used for convenience. In the log amplifier and optional GPIB interface PCB tests, this frequency is used for two reasons: the 8481A power sensor is calibrated at 50 MHz, and the 355D Step Attenuator is more accurate at this frequency. (50 MHz is low enough in frequency that the 355D specifications for dc may be used.)

a. Equipment Setup and Initial Switch Positioning

1. Connect test equipment and position sweep generator controls as shown in Figure 4-1.

2. Position A3 PCB TEST-NORMAL switch to TEST. Access to this switch is permitted through a hole in the bottom panel of the network analyzer section. Reposition 560A upright.

Table 4-1. Recommended Test Equipment

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED MANUFACTURER
SWEEP GENERATOR	Horizontal output, blanking, and marker signals compatible with the 560A. Refer to Table 1-1. Frequency: 50 MHz*. Output Power: +10 dBm.	WILTRON Model 6647A Programmable Sweep Generator 8620
DIGITAL VOLTMETER	4-1/2 digit readout.	Hewlett-Packard 3465A
POWER METER	50 MHz calibrated output.	Hewlett-Packard 435A
POWER SENSOR	Ability to handle 0 dBm.	Hewlett-Packard 8481A
POWER SUPPLY	+20V at 180 mA.	Hewlett-Packard 6215A
STEP ATTENUATOR	60 dB range.	Hewlett-Packard 355D
POWER AMPLIFIER	Gain: 10 dB; Output Power: 31 dBm	Anzac Model AM109
ATTENUATOR, 6 dB ATTENUATOR, 10 dB	SWR: 1.04 at 50 MHz. Accuracy: ±.05 dB	Weinschel 50-6 Weinschel 50-10
ADAPTER	BNC jack to Type N plug.	Pamona Part No. 3288
ADAPTER	Type N jack to BNC plug.	Pamona Part No. 3535
CABLE, 12"	BNC to BNC.	Pamona P/N 2249-C-12
Additional Equipment Required for GPIB PC Board Calibration:		
OSCILLOSCOPE	20mV/division vertical sensitivity.	Tektronix 5103N/D10 with 5A15N and 5B10N
GPIB CONTROLLER	IEEE 488 (IEC 625-1) Interface.	Model 85 with: HP 82903A 16k Memory Module HP 82936A ROM Drawer HP 00085-15002 Plotter/ Printer ROM HP 00085-15003 I/O ROM HP 00085-15004 Matrix ROM HP 82937A GPIB Interface

*50 MHz is used because (1) the 8481A Power Sensor is calibrated at this frequency and (2) the 355D Step Attenuator is more accurate at this frequency. (50 MHz is low enough in frequency that the 355D specifications for dc may be used.)

Table 4-1. Recommended Test Equipment

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED MANUFACTURER
	Directivity Measurements Above 2 GHz	
AUTOMATED SCALAR NETWORK ANALYZER	Sweep Generator Leveled Output ±1.0 Frequency Range: 2 to 18 GHz	WILTRON 5637 with 560-10BX cable
	Scalar Network Analyzer Vertical Sensitivity: 0.5 dB per division Variable Offset Control	
AIR LINE	SWR: 1.002 (GPC 7 Connector) SWR: 1.006 (Type N Connector) SWR: 1.006 (WSMA Connector)	WILTRON 18 Series 19 Series
20 dB Offset	20 ±1.0 dB (GPC 7 Connector) 20 ±1.5 dB (WSMA Connector)	WILTRON 29 Series
	Directivity Measurement Below 2 GHz	
SWEEP GENERATOR	Leveled Output ±1.0 dB Frequency Range: 10 MHz to 2 GHz	WILTRON 6609A
OSCILLOSCOPE	Vertical Sensitivity: 10 μV per division	Tektronix 5110 with 5A22N Differential Amplifier
DETECTOR	SWR: 1.25	WILTRON 74 Series
STEP ATTENUATOR	0 to 50 dB in 1 dB steps	Weinschel AC-117A-69-43
PRECISION TERMINATION	50 ±0.5 Ohms GPC 7 Test Port Connector Type N Test Port Connector WSMA Female Test Port Connector WSMA Male Test Port Connector 75 ±0.5 Ohms Type N Test Port Connector BNC Test Port Connector	 28A50-1 26N50 26S50 26SF50 26N75 26B75
	Pin Depth Measurement	
CONNECTOR GAUGE	GPC 7 Connector Range: 0.001 to 0.250 in. Type N Connector Dial Graduations: 0.0001 in. WSMA Connector Dial Graduations: 0.0001 - 0.25 in.	Maury Microwaves Corp. (MMC) A-024 MMC A-007A WILTRON 01-160 WSMA Gauging Set

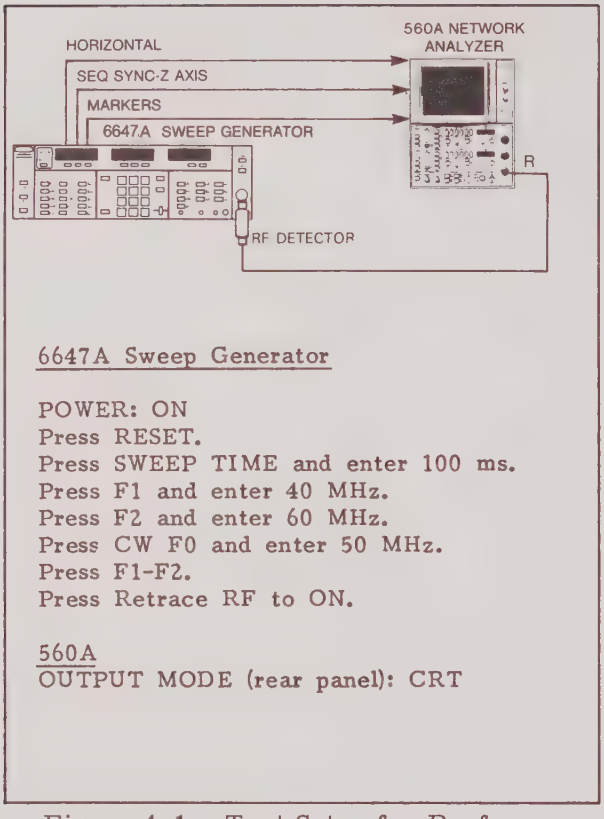


Figure 4-1. Test Setup for Performance Verification

CAUTION

On 560As where access to the TEST-NORMAL switch is via the hole in the bottom panel, use a short-shafted screwdriver to gently nudge the switch toward the center of the PCB. Do not press down on switch shaft with screwdriver blade. Applying pressure to switch shaft can damage switch.

NOTE

In the horizontal clamp test (subparagraph b, below), instructions will be given to adjust the CRT mainframe HORIZ POSITION potentiometer. The earth's magnetic fields may affect the horizontal positioning of the CRT trace; consequently, the potentiometer should be adjusted with the 560A oriented in either the same position in which it will be used or the same position in which further testing will be conducted.

3. Position 560A controls as follows:

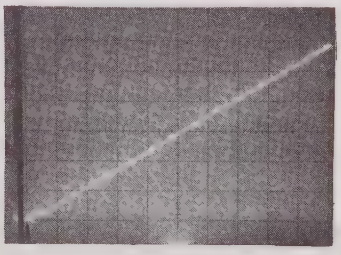
   CHANNEL A ON: On
   - INPUT: R
   - MEMORY: Off
   - dB PER DIVISION: 17 (10, 5, & 2 depressed)
   - REFERENCE dB/dBm: dBm
   - OFFSET ZERO: Not depressed
   - OFFSET: +50.0

   CHANNEL B ON: Off
   - INPUT: R
   - MEMORY: Off
   - dB PER DIVISION: 17 (10, 5, & 2 depressed)
   - REFERENCE dB/dBm: dBm
   - OFFSET ZERO: Not depressed

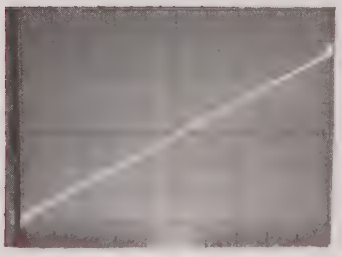
   MARKER THRESHOLD: Off
   REAL TIME: On
   REFRESH HOLD: Off
   SMOOTHING: Off
   POWER: On

b. Horizontal Clamp and CRT Mainframe HORIZ POSITION Adjustments

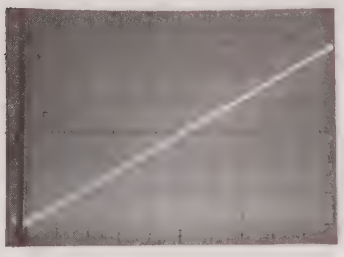
1. Adjust OFFSET to position trace so that both ends can be observed; see waveform below.



2. Adjust front panel HORIZ START screwdriver potentiometer until left end of trace begins to intensify and clamping starts. Clamping is indicated when the trace stops rising diagonally and either "shoots up" (right end) or "drops off" (left end) vertically. See waveform below.



3. Adjust HORIZ STOP potentiometer until right end of trace starts clamping. An example of a properly adjusted waveform is shown below.



4. Press MANUAL SWEEP button (6647A); adjust MANUAL SWEEP control to low end of frequency band.

5. Connect DVM between 560A HORIZONTAL OUTPUT connector (rear panel) center conductor and chassis. Meter should indicate 0V ±0.2V (OUTPUT MODE switch in CRT position).

6. Adjust MANUAL SWEEP control (6647A) to high end of frequency band. DVM should indicate +10.0 ±0.2 Vdc. If meter does not indicate correct voltage, refer to HORIZ STOP troubleshooting chart, Figure 7-7.

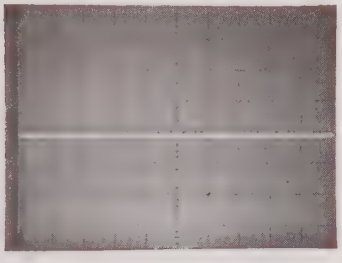
7. Press AUTO button (6647A).

8. Depress INPUT A pushbutton lightly so that all three Channel A INPUT switches are released.

9. Rotate OFFSET control clockwise until trace is positioned on center graticule line.

10. Adjust CRT mainframe HORIZ POSITION to position left end of trace on left graticule edge.

11. Adjust CRT mainframe X-Gain potentiometer (Figure 5-12) to position right end of trace on right graticule edge. The HORIZ POSITION and X-Gain potentiometers are interactive; repeat steps 10 and 11 until trace is positioned as shown below.



c. Refresh Horizontal Gain Test

1. Depress Channel A INPUT R.

2. Rotate OFFSET control counterclockwise for +50.0, as indicated on OFFSET dB display.

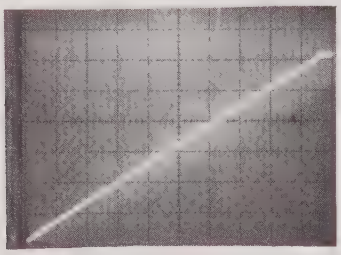
3. Depress CHANNEL B ON.

4. Adjust Channel B OFFSET for +40.0, as indicated on OFFSET dB display.

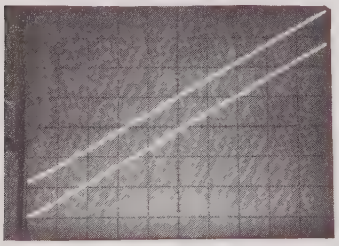
5. Depress REFRESH.

6. Adjust both OFFSET controls to position traces so that the start (left end) of Channel A refresh ramp (diagonal trace) and the finish (right end) of the Channel B refresh ramp can be observed. Channel A ramp should start on the left graticule edge, and the Channel B ramp should end on the right graticule edge. Traces should not be flattened out at the right end (waveform on the next page). If traces

are not AS DESCRIBED, REFER TO PARAGRAPH 5-3.3.



7. Readjust both OFFSET controls as required to observe the finish of both ramps. Both ramps should end at right graticule edge - see below. If traces do not end at right graticule edge, refer to paragraph 5-3.3.



8. Depress CHANNEL B ON pushbutton (turn Channel B off).

9. Channel A ramp should finish at right graticule edge. If trace does not finish at right graticule edge, refer to paragraph 5-3.3.

10. Depress X - Y PLOT pushbutton and observe intensified dot as it moves across CRT. If dot fails to reach right graticule edge, refer to paragraph 5-3.3.

d. Channel A and Channel B OFFSET ZERO tests

1. Depress Channel A and Channel B .2 dB PER DIVISION pushbuttons.

2. Depress REAL TIME.

3. Rotate OFFSET control clockwise for -00.0, as indicated on OFFSET dB display.

4. Depress INPUT A pushbutton lightly so that all three Channel A INPUT switches are released.

5. Depress REF POS LOCATE momentarily and insure that trace deflects to center graticule line.

6. Depress OFFSET ZERO; verify that trace deflects to center graticule line. If trace does not deflect as described, refer to paragraph 5-3.4.

7. Depress REF POS LOCATE momentarily and verify that trace does not deflect. If trace deflects, refer to paragraph 5-3.4.

8. Depress (release) OFFSET ZERO.

9. Depress Channel A INPUT R.

10. Depress X - Y PLOT pushbutton and observe intensified dot as it moves across CRT. If dot fails to reach right graticule edge, refer to paragraph 5-3.3

11. Repeat steps 3 thru 8 for Channel B.

e. CRT Mainframe Vertical Calibration

1. Rotate OFFSET control counterclockwise for +30.0, as indicated on OFFSET dB display (CHANNEL B INPUT switches must be out; see step d4 above).

2. Depress 5 dB PER DIVISION pushbutton.

3. Depress and hold REF POS LOCATE and adjust SET potentiometer to position trace on next-to-top graticule line.

4. Release REF POS LOCATE. Trace should deflect to next-to-bottom graticule line. If trace does not deflect as described, refer to paragraph 5-3.5.

5. Rotate OFFSET control clockwise for -30.0, as indicated on OFFSET dB display.

6. Depress and hold REF POS LOCATE and adjust SET potentiometer to position trace on next-to-bottom graticule line.

7. Release REF POS LOCATE. Trace should deflect to next-to-top graticule line. If trace deflection is not as described, A2 PCB is faulty.

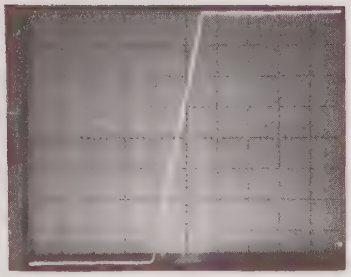
8. Depress and hold REF POS LOCATE and adjust SET potentiometer to position trace to center graticule line.

9. Release REF POS LOCATE.

10. Depress Channel B INPUT R.

f. Storage Memory Digital-to-Analog Converter Calibration

PARAGRAPH DELETED



g. Vertical Analog-to-Digital Converter Calibration

1. Depress 10 dB PER DIVISION pushbutton.

2. Depress REFRESH.

3. Depress MEMORY OFF.

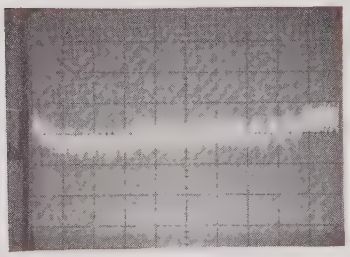
4. Depress STORE TRACE momentarily.

5. Depress SUBTRACT.

6. Depress .2 dB PER DIVISION pushbutton.

7. Observe CRT. A trace similar to

that shown below should be present near center-screen. The perturbations on the trace should not exceed 1-1/2 major divisions on either side of the center graticule line. If the trace is not as described, refer to paragraph 5-3.7.



8. Depress MEMORY OFF.

9. Depress CHANNEL A ON pushbutton.

10. Depress Channel A and Channel B 10 dB PER DIVISION pushbuttons.

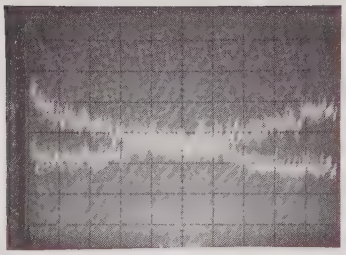
11. Rotate Channel A OFFSET control counterclockwise until Channel A trace is superimposed on Channel B trace.

12. Depress Channel A and Channel B STORE TRACE pushbuttons.

13. Depress Channel A and Channel B SUBTRACT pushbuttons.

14. Depress Channel A and Channel B .2 dB PER DIVISION pushbuttons.

15. Observe CRT. A criss-cross waveform pattern similar to that shown below should be present. The ends of the Channel A and Channel B traces should be contained within the 6 major divisions that extend ±3 divisions on either side of the center graticule line. If the traces are not as described, refer to paragraph 5-3.7.



h. Channel A and Channel B Memory and Subtract Balance

1. Depress Channel A and Channel B MEMORY OFF pushbuttons.

2. Depress CHANNEL A ON pushbutton (turn Channel A off).

3. Depress REAL TIME.

4. Depress INPUT B pushbutton lightly so that all three Channel B INPUT switches are released.

5. Rotate OFFSET control clockwise for -00.0, as indicated on OFFSET dB display.

6. Depress OFFSET ZERO. Trace should deflect to center graticule line.

7. Depress STORE TRACE momentarily.

8. Depress RECALL. Verify that trace does not deflect from center graticule line. If trace deflects, refer to paragraph 5-3.8.

9. Depress SUBTRACT. Verify that trace does not deflect from center graticule line. If trace deflects, refer to paragraph 5-3.8.

10. Depress (release) OFFSET ZERO.

11. Depress MEMORY OFF.

12. Depress Channel B INPUT R.

13. Depress CHANNEL A ON and CHANNEL B ON pushbuttons. (Turn Channel A on and Channel B off.)

14. Repeat steps 4 thru 11 for Channel A.

i. Refresh Memory Digital-to-Analog Converter and Dot-Connector Calibration

1. Depress Channel A 5 dB PER DIVISION.

2. Depress and hold REF POS LOCATE and adjust SET potentiometer to position trace on next-to-bottom graticule line.

3. Release REF POS LOCATE.

4. Rotate OFFSET control clockwise to position trace on next-to-top graticule line (≅ -30.0 as indicated on OFFSET dB display).

5. Depress REFRESH.

6. Depress OFFSET ZERO. Trace should deflect to next-to-bottom graticule line. If trace deflection is not as described, refer to paragraph 5-3.9. Depress OFFSET ZERO.

7. Depress and hold REF POS LOCATE and adjust SET potentiometer to position trace on next-to-top graticule line.

8. Release REF POS LOCATE.

9. Rotate OFFSET control counterclockwise to position trace on next-to-bottom graticule line (≅ +30.0 as indicated on OFFSET dB display).

10. Depress OFFSET ZERO. Trace should deflect to next-to-top graticule line. If trace deflection is not as described, A2 PCB is faulty. Depress OFFSET ZERO.

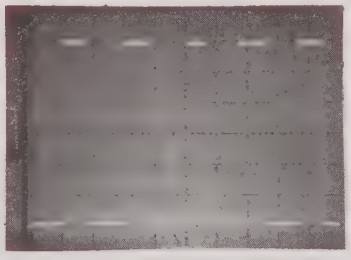
11. Depress REAL TIME.

12. Set SWEEP TIME controls for a 10 s sweep.

13. Observe CRT and when intensified dot reaches the right of the screen, depress REFRESH.

14. Depress OFFSET ZERO; when refresh sweep starts, alternately release and depress OFFSET ZERO to obtain approximately 10 to 12 rectangular pulses on the CRT. At the conclusion of the refresh sweep, immediately depress REFRESH HOLD to save the display.

15. Observe CRT and verify that pulses are rectangular with no overshoot or ringing. See waveform below. If overshoot or ringing is present, refer to paragraph 5-3.9.



16. Depress X-Y PLOT.

17. Observe CRT. Intensified dot should trace the rectangular pulse pattern; there should be no overshoot or ringing. If overshoot or ringing is present, refer to paragraph 5-3.9.

18. Depress (release) REFRESH HOLD.

19. Set SWEEP TIME controls for a 100 ms sweep.

20. Depress REF POS LOCATE and adjust SET potentiometer to position trace on center graticule line.

21. Position A3 PCB TEST-NORMAL switch to NORMAL.

22. Reinstall bottom (if necessary).

23. Remove RF detector from between sweeper and 560A.

POWER ACCURACY TESTS

Power Accuracy Verification is divided into two tests. The first test verifies the most common measurement range, +10 to -55 dBm, and is contained in steps j through q. This test requires only two additional items of test equipment: (1) a power meter/power sensor and (2) a step attenuator.

The second test verifies power accuracy at +16 dBm and is provided in steps r and s. This test requires an RF power amplifier, a dc power supply, and two attenuators in addition to the power meter/power sensor.

Unless the 560A is going to be used at +16 dBm, verification at this power level is not necessary - skip steps r and s and proceed to step t.

j. Power Meter/Power Sensor Calibration at 50 MHz

1. Position CAL FACTOR control on power meter to the correct power factor (see chart on power sensor).

2. Position the RANGE control to 1mW.

3. Connect power sensor to POWER REF connector. Adjust CAL ADJ screwdriver potentiometer to position meter pointer on CAL mark.

4. Disconnect power sensor from POWER REF connector.

k. Sweep Generator/Step Attenuator Output Power Calibration

1. Set up the test equipment as shown in Figure 4-2, and connect the 8481A Power Sensor to the output of the step attenuator.

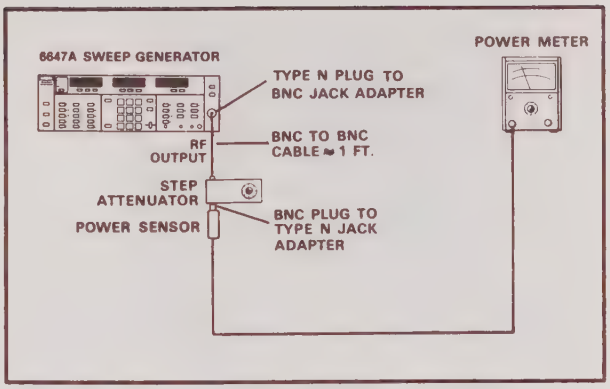

6647A SWEEP GENERATOR
POWER METER
TYPE N PLUG TO BNC JACK ADAPTER
BNC TO BNC CABLE ≈ 1 FT.
RF OUTPUT
STEP ATTENUATOR
POWER SENSOR
BNC PLUG TO TYPE N JACK ADAPTER

Figure 4-2. Test Setup for Sweep Generator/Step Attenuator Output Power Calibration

2. On the 6647A:

a. Press CW FØ.
b. Press LEVEL and set for +5 dBm.

3. On the 335D, position the attenuator dial to 10.

4. On the 6647A, press LEVEL and operate the INCREASE-DECREASE lever to obtain a -5 dBm reading on the power meter.

5. Record the 6647A's indicated output power level from the LEVEL LED display.

6. On the 6647A,

a. Set the power level for a +10 dBm reading on the LEVEL LED display.

b. Operate the INCREASE-DECREASE lever to obtain a 0 dBm reading on the power meter.

c. Record the 6647A's indicated output power level from the LEVEL LED display.

d. Press F1-F2.

m. Channel A Low Level Calibration

1. Connect RF detector to front panel connector A. (Leave detector unconnected from RF source.)

NOTE

Ensure that bottom cover is installed.

2. Depress SMOOTHING to MAX.

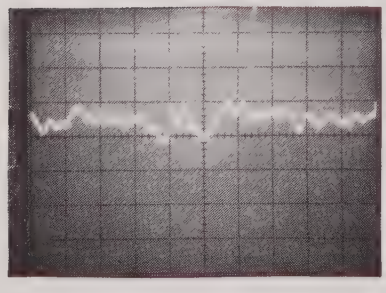
3. Depress INPUT A.

4. Rotate OFFSET control clockwise to -58.0, as indicated on display.

5. Depress 1 dB PER DIVISION pushbutton.

6. On right side panel, adjust CH A (LOW LEVEL TRIM) control as follows:

(a) If trace is below center graticule line, rotate potentiometer counterclockwise until trace is slightly above center line and exhibits only random negative clipping. See waveform below.



(b) If trace is either above center graticule line or off-screen, rotate potentiometer clockwise until trace is positioned as described in (a) above.

n. Channel A Power Accuracy Test

1. Rotate OFFSET control counterclockwise to +10.0, as indicated on display.

2. Connect RF detector to output connector of 355D.

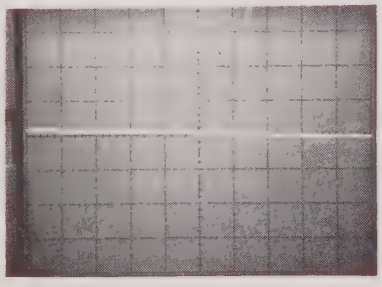
3. Depress .2 dB PER DIVISION pushbutton.

4. Construct a chart similar to that shown below in Table 4-2.

5. Operate the chart of Table 4-2 as follows:

(a) Position 355D to first Attenuator Dial Setting.

(b) Adjust OFFSET control to position center of trace (50 MHz) coincident with center of graticule crosshairs on CRT; see waveform below.



set at stop mark

(c) Record OFFSET dB display value in OFFSET dB Reading column.

(d) Repeat steps (a) through (c) for remaining Attenuator Dial Settings up through 60.

(e) On the 6647A, press LEVEL and set the output power for the value recorded in step k.5 above.

(f) On the 560A, repeat steps (b) and (c) above.

(g) If any of the power accuracy readings are out of tolerance, refer to paragraph 4-4 for instructions on how to interpret the chart in Table 4-2.

(h) On the 6647A, press LEVEL and set the output power for the value recorded in step k.6(c) above.

o. Channel B Low Level Calibration

1. Depress CHANNEL A ON and CHANNEL B ON pushbuttons (turn Channel A off and Channel B on).

2. In subparagraph m, repeat step 1 and steps 3 through 6 for Channel B.

p. Channel B Power Accuracy Test

Repeat subparagraph n, steps 1 through 6 for Channel B.

q. Channel R Power Accuracy Test

1. Disconnect RF detector from B and move to R connector.

2. Depress Channel B INPUT R pushbutton.

3. Rotate OFFSET control counterclockwise for +10.0, as indicated on OFFSET dB display.

NOTE

The output signal from the R channel log amplifier is processed by the A1/A2 PCB Channel B circuits and displayed on Channel B trace.

4. Repeat subparagraph n, steps 1 through 5 for Channel R except: for Channel R complete the chart in Table 4-2 only through Attenuator Dial Setting 40. The R channel has a power measurement range of +16 to -30 dBM.

Table 4-2. Power Accuracy Chart

Attenuator Dial Setting	Input Power Level (dBm)	OFFSET dB Reading	Limits (dBm)
0	+10		+10.6 to + 9.5
10	0		+ 0.7 to - 0.5
20	-10		- 9.4 to -10.6
30	-20		-19.3 to -20.6
40	-30		-29.2 to -30.7
50	-40		-39.2 to -40.8
60	-50		-49.1 to -50.9*
60	-55		-53.8 to -56.3

*If power acuracy reading is not within limits, recheck Channel A Low Level Calibration (subparagraph m above).

Don't Do

r. +16 dBm Power Accuracy Test Setup Output Power Calibration

1. Set FREQUENCY SELECTOR to CW FO (6647A).

2. Set RF output at 6 dBm.

3. Connect equipment as shown in Figure 4-3.

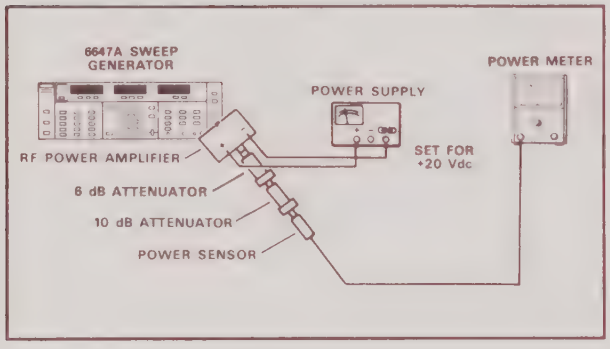


Figure 4-3. Equipment Setup, +16 dBm Verification

4. Disconnect power sensor from 10 dB attenuator.

5. Remove both attenuators from test setup and connect RF detector to output of power amplifier.

6. Set FREQUENCY SELECTOR to F1 TO F2 (6647A).

Don't D

s. +16 dBm Power Accuracy Test

1. Rotate OFFSET control counterclockwise to +16.0, as indicated on OFFSET dB display.

2. Adjust OFFSET control to position center of trace (50 MHz) on center of graticule crosshairs on CRT.

3. Record the OFFSET dB display value. This reading, which is the R channel power accuracy at +16 dBm, should fall between +16.8 and +15.7 dBm.

4. Move RF detector to front panel connector B.

5. Repeat steps 2 and 3 above for Channel B (the same accuracy limits apply).

6. Depress CHANNEL A ON and CHANNEL B ON (turn on Channel A and turn off Channel B).

7. Move RF detector to front panel connector A.

8. Repeat steps 2 and 3 above for Channel A (the same accuracy limits apply).

t. Smoothing Verification Tests

1. Position RF ON switch to off (6647A).

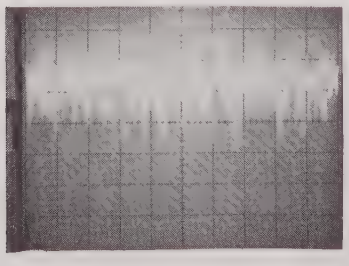
2. Depress 2 dB PER DIVISION.

3. Disconnect RF detector from R connector and move to B connector.

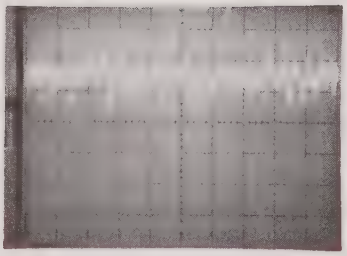
4. Depress INPUT B.

5. Adjust OFFSET control for -58.0, as indicated on OFFSET dB display.

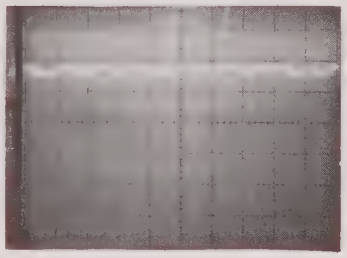
6. Depress SMOOTHING to OFF, MIN, and MAX and observe trace at each position. Trace should exhibit a change in noise level (see waveforms A, B, and C below). If no change in noise is observed, the A3 PCB is faulty.



A - SMOOTHING OFF



B - SMOOTHING MIN



C - SMOOTHING MAX

u. Marker Verification Tests

1. Position RF ON switch to ON (6647A).

2. Rotate OFFSET control counterclockwise for ±00.0 on OFFSET dB display.

3. Position attenuation dial on 355D to 10.

4. Depress the 5 dB PER DIVISION pushbutton.

5. Rotate MARKER AMPLITUDE control fully clockwise (6647A).

6. Rotate MARKER THRESHOLD control (560A) clockwise out of detent until marker pulse appears on trace. If no marker appears on trace, refer to Marker Malfunction Troubleshooting Chart, Figure 7-13.

7. Rotate TILT control throughout its range. Marker should tilt ±45 de-

grees. If marker does not tilt, A1 PCB is faulty.

DON'T DO

4-3.3 Performance Verification Procedure (Option 3--GPIB)

The procedure for verifying 560A GPIB Interface (A6) PCB performance is given below. This procedure assumes the 560A performance to be within specified limits; consequently, the procedures in paragraph 4-3.2 should be completed first. The A6 PCB test setup and initial control positioning requirements for the sweep generator are shown in Figure 4-4. To verify the performance of of the A6 PCB, proceed as follows:

a. Power Meter/Power Sensor Calibration at 50 MHz (Refer to Performance Verification Procedure, paragraph 4-3.2j.)

b. Sweep Generator/Step Attenuator Output Power Calibration (Refer to Performance Verification Procedure, paragraph 4-3.2k.)

c. Initial Positioning of 560A Controls

CHANNEL A ON: On
INPUT: A
MEMORY: Off
dB PER DIVISION: 1
REFERENCE dB/dBm: dBm
OFFSET: −58.0
OFFSET ZERO: Not depressed
CHANNEL B ON: Off
INPUT: B
MEMORY: Off
dB PER DIVISION: 1
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
MARKER THRESHOLD: Off
REFRESH: On
REFRESH HOLD: Off
SMOOTHING: MAX
POWER: On

d. Channel A Low-Level Calibration

1. Connect RF detector to front panel A connector. (Leave detector unconnected from RF source.)

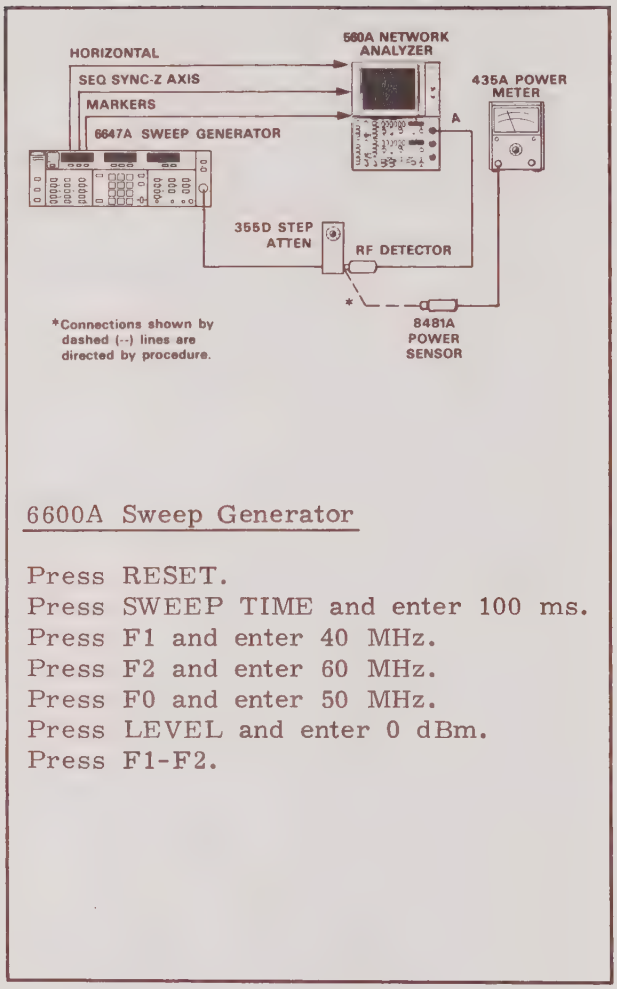


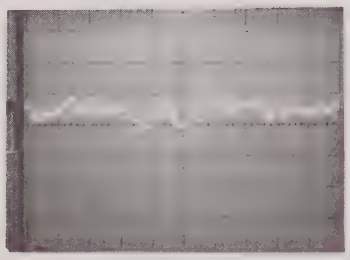
Figure 4-4. Equipment Setup for A6 PCB Performance Verification

2. Depress and hold REF POS LOCATE and adjust SET potentiometer to position trace on center graticule line.

3. Release REF POS LOCATE.

4. Adjust CH A side panel control as follows:

(a) If trace is below center graticule line, rotate potentiometer counterclockwise until trace is slightly above center graticule line and exhibits only random negative clipping. See waveform below.



(b) If trace is either above the center graticule line or off-screen, rotate potentiometer clockwise until trace is positioned as described in step (a), above.

e. GPIB Controller Readout/560A OFFSET dB Display Tracking Tests

1. Connect detector to the sweeper's RF OUTPUT connector. Press ΔF and set to 0 MHz. Press SHIFT and CW RAMP.

2. Adjust attenuator dial on 355D to 0.

3. Program controller (1) for maximum smoothing, and (2) to take data continuously from Channel A. Se flowchart in Figure 4-5. A computer program (written in HPL for the HP 9825A Programmable Calculator) that implements this flowchart is provided in Figure 4-6; Figure 4-7 provides a program written in BASIC for the WILTRON 85 Controller.

4. Rotate OFFSET control on 560A counterclockwise to position the trace on the center graticule line. The OFFSET dB display should indicate between +10.6 and +09.5 ±1 digit; the readout on the controller should indicate the same value as that shown on the OFFSET dB display ±0.1 dB. Example: OFFSET dB Display indicated +10.1; controller should indicate between +10.00 and +10.20. If reading is not correct, refer to paragraph 5-5 for calibration procedure.

5. Repeat step 4 for 355D attenuator dial settings of 10 thru 60. At each attenuator dial setting, OFFSET dB display readout should be within the limits specified in Table 4-2. To compensate for noise at the lower power levels (i.e., -40 and -50 dBm), it may be necessary to average approximately 100 readings to meet the specified tolerance. If readout is not as specified, refer to paragraph 5-5 for calibration procedure.

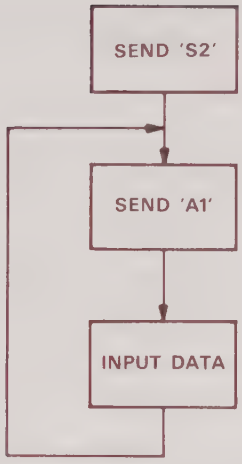


Figure 4-5. Flowchart for Programming SMOOTHING MAX (S2) and Continuous Data Readout on Channel A

```
0: wrt 706,"S2"
1: wrt 706,"A1"
2: red 706,X
3: dsp X
4: wait 50
5: gto 0
```

Figure 4-6. GPIB Program in HPL for HP 9825A Controller

```
10 OUTPUT 706 ;"A1S2"
20 ENTER 706 ; X@ DISP X
30 WAIT 100 @ GOTO 10
40 END
```

Figure 4-7. GPIB Program in BASIC for WILTRON 85 Controller

f. -30 dBm Comparator Trip Point Test

1. Adjust attenuator dial on 355D to 10 (0 dBm). Observe controller display and make a mental note of the rate at which readout digits change (readout rate).

2. Rotate attenuator dial counterclockwise to 40 (-30 dBm). The controller readout rate should slow. If readout rate does not slow, refer to paragraph 5-5 for calibration procedure.

3. Increase RF output of sweeper until controller readout rate increases. The increase in the readout rate should occur around -29.5 dBm (-29.50 on controller readout). If test is not as specified, proceed to paragraph 5-5 for calibration procedure.

g. +/- Sign Change Trip Point Test

1. Rotate attenuator dial on 355D clockwise to 10.

2. Disconnect RF detector from 355D; connect power sensor in its place.

3. Set RF output for a 0 dBm reading on power meter.

4. Disconnect power sensor from 355D and reconnect RF detector.

5. Decrease and then increase the RF output of the sweeper. The sign of the readout digits, as shown on the controller display, should change as the RF power level is varied approximately 0.05 dB either side of 0 dBm. If test result is not as specified, refer to paragraph 5-5 for calibration procedure.

h. Smoothing Sequencer Test

1. Rotate attenuator dial on 355D counterclockwise to 50 (-40 dBm).

2. Observe SMOOTHING indicators on 560A front panel. The MAX indicator should appear to be lit continuously, and the OFF indicator should be flashing. If test results are not as specified, A6 PCB is faulty.

i. Settling Time Determination Tests Using HP 9825A Programmable Calculator

1. Referring to flowchart in Figure 4-8 or program in Figure 4-9, program

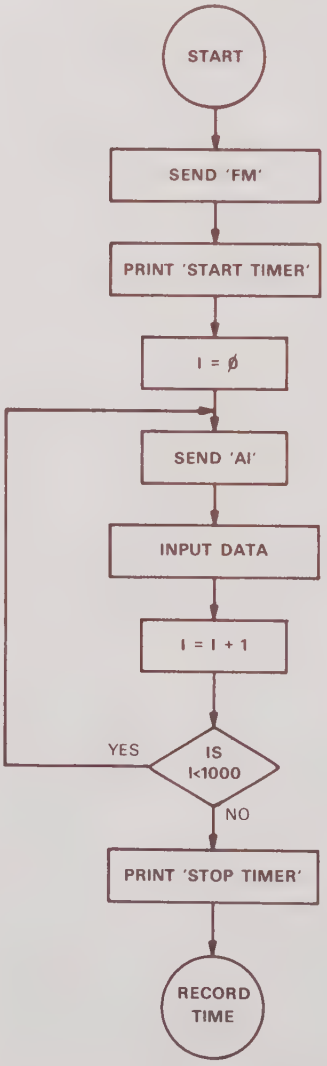


Figure 4-8. Flowchart for Programming 560A to Return 1000 Readings of Channel A Data

the controller to (1) send a fast mode (FM) command and (2) take 1000 readings of Channel A data. Use a stopwatch to measure the time between "START TIMER" and "STOP TIMER" in the controller program. Record this time, for it will be used as a reference time for SØ, S1 and S2 measurements. (This time is the inherent time delay of the controller/560A GPIB system.)

2. Program controller to (1) send hold mode (HM) command, (2) send smoothing off (SØ) command, and (3) take 1000 readings of Channel A data. (In flowchart of Figure 4-7, change "FM" to "HMSØ" and rerun program.) Use a stopwatch to measure the time between "START TIMER" and "STOP TIMER" in controller program. Subtract the time measured in step 1 from the time measured in this step. The difference between these two times should be 12 ±2 seconds. If the time is not 12 ±2 seconds, the A6 PCB is faulty; there is no adjustment for this time delay.

3. Program controller for smoothing 1 (substitute "S1" for "SØ" in flowchart) and repeat step 2. The time should be 40 ±6 seconds. As in step 2 above, if this time is incorrect the A6 PCB is faulty.

4. Program controller for smoothing 2 (substitute "S2" for "S1" in flowchart) and repeat step 2. The time should be 200 ±30 seconds. As in step 2 above, if this time is incorrect the A6 PCB is faulty.

j. Settling Time Determination Tests Using WILTRON 85 Controller

1. Enter and run the program shown in Figure 4-10. The first time, the printout will show the time for FMS0 (fast mode, smoothing off). It is nominally 60 seconds.

```
0: wrt 706,"FM"
1: prt "Start
 timing    with
 the first  beep
 .";spc
2: prt "Stop
 timing withthe
 second beep.";
 spc 3
3: 0→I
4: wait 50;beep
5: wrt 706,"AI"
6: red 706,X
7: I+1→I
8: if I<1000;
 gto 5
9: beep;prt "Sto
 p timing.";spc
 3
10: wrt 706,"RL"
11: stp
```

Figure 4-9. GPIB Program in HPL for Taking 1000 Readings of Measurement Data

```
 10 PRINT "RUN TIME APPROX. 5 MI
    NUTES"
 20 CLEAR
 30 READ O$@ IF O$="X" THEN 150
 40 DISP "TESTING ";O$
 50 OUTPUT 706 ;O$
 60 SETTIME 0,0
 70 FOR I=0 TO 1000
 80 OUTPUT 706 ;"AI"
 90 ENTER 706 ; Z
100 NEXT I
110 T=TIME @ IF O$="FMS0" THEN S
    =T ELSE T=T-S
120 PRINT "TIME FOR ";O$;T;"SEC"
130 GOTO 20
140 DATA "FMS0","HMS0","HMS1","H
    MS2","X"
150 OUTPUT 706 ;"RL"
160 PRINT "END OF RUN"
170 END


RUN TIME APPROX. 5 MINUTES
TIME FOR FMS0 56.359 SEC
TIME FOR HMS0 11.771 SEC
TIME FOR HMS1 39.582 SEC
TIME FOR HMS2 219.203 SEC
END OF RUN
```

Figure 10. GPIB Program in BASIC for Taking 1000 Readings of Measurement Data

2. The second time, the printout will show the time for HMS0 (hold mode, smoothing off). It should be 12 ±2 seconds. If the time is out-of-tolerance, the A6 PCB is faulty. There is no adjustment for this time delay.

3. The third time, the printout will show the time for HMS1 (hold mode, smoothing minimum). It should be 40 ±6 seconds. As in step 2 above, if this time is incorrect, the A6 PCB is faulty.

4. The fourth time, the printout will show the time for the HMS2 (hold mode, smoothing maximum). It should be 200 ±30 seconds. As in step 2 above, if this time is incorrect, the A6 PCB is faulty.

4-4 POWER ACCURACY MEASUREMENT CHART

This paragraph describes the power accuracy measurement chart that appears in paragraph 4-3.2 n. of the Performance Verification Procedure. This description is divided into two areas: (1) a description and listing of the possible error sources inherent in the power measurement system of paragraph 4-3.2, and (2) recommended courses of action, should one or more power accuracy readings be out of tolerance.

4-4.1 Error Sources Inherent in Performance Verification Procedure Power Measurement System

The power measurement system (i.e., power meter, sweep generator, step attenuator, and RF detector) in paragraph 4-3.2 contains several inherent possible error sources. A listing of these error sources is given below; the degree to which these error sources contribute to measurement uncertainty is given in Table 4-3.

a. Detector/Source Match Interaction Error. The impedance mismatch between the RF source and the RF detector contributes a possible error known as source match. For the Model 6647A Programmable Sweep Generator and the 560-7 series detectors, this error is: At +10 dBm (355D Attenuator Dial at 0), the source match of the sweeper and the mismatch of the RF detector interact to produce an overall error of 0.28 dB. At 0 dBm and below (355D Attenuator Dial between 10 and 60), the source match of the 355D and the RF detector interact to produce an error of 0.14 dB.

b. Harmonic Frequency Error. In the linear range of the RF detector, i.e., +16 dBm to approximately -15 dBm, harmonics of the sweep generator fundamental frequency contribute possible errors in measurements.

c. Step Attenuator Error. The HP 355D Step Attenuator has a specified accuracy of ±0.3 dB from dc to approximately 50 MHz. This possible error in accuracy is present at all attenuator dial settings, including zero.

d. Model 560-7 or 560-71 Series RF Detectors Frequency Sensitivity Error. This possible error source varies with frequency and is graphically shown in Table 1-3.

e. A and B Log Amplifier Accuracy Error. This possible error source varies with input power; it is graphically shown in Table 1-1.

4-4.2 Recommended Courses of Action for Power Accuracy Out-of-Tolerance Conditions

The Channel A and B accuracy potentiometers (R154 and R181), along with those for Channel R (R230 and R294), are critical adjustments. These potentiometers should not be adjusted until all of the other possible-error-producing sources have been checked, or, in the case of the 560 detectors, until the possible-error sources have been isolated from the 560A input. Therefore, the following should be performed before the accuracy adjustments are attempted.

Table 4-3. Possible Errors Inherent in Power Measurement System of Paragraph 4-3.2

Input Power (dBm)	Possible Error (dB) at 50 MHz					RMS Error*
	Det./Source Match Interaction	Harmonic Frequency at 30 dBc	Attenuator Accuracy	Detector Frequency Sensitivity	Log Amp Accuracy	
+16	±0.31	+0.6 -0.4	±0.04	+0.3 -0.2	±0.4	+0.8 -0.7
+10	±0.28	+0.3 -0.2	±0.3	+0.3 -0.2	±0.2	+0.6 -0.5
0	±0.14	+0.3 -0.2	±0.3	+0.3 -0.2	±0.3	+0.7 -0.5
-10	±0.14	+0.15 -0.1	±0.3	+0.3 -0.2	±0.4	±0.6
-20	±0.14	+0.15 -0.1	±0.3	+0.3 -0.2	±0.5	+0.7 -0.6
-30	±0.14	+0.15 -0.1	±0.3	+0.3 -0.2	±0.6	+0.8 -0.7
-40	±0.14	+0.15 -0.1	±0.3	+0.3 -0.2	±0.7	±0.8
-50	±0.14	+0.15 -0.1	±0.3	+0.3 -0.2	±0.8	±0.9

*The rms error is found by squaring the individual errors, summing them, and taking their square root. The rms error for +10 dBm would be as follows:

$$\sqrt{(0.28)^2 + (0.3)^2 + (0.3)^2 + (0.3)^2 + (0.2)^2} = 0.62, \text{ or } 0.6.$$

a. If any of the power accuracy readings for Channel A (or B) are out of tolerance, perform the Channel B (or A) low-level calibration and power accuracy tests in paragraph 4-3.2. After performing the Channel B (or A) tests:

   1. If Channel A (or B) is out of tolerance but Channel B (or A) is not, perform the Channel A (or B) checks and adjustments in paragraph 5-4.1. After performing these checks and adjustments, recheck Channel A (or B) power accuracy.

   2. If both channels' power accuracy readings are out of tolerance:

      (a) Try a different RF detector.

      (b) Try a different 355D Step Attenuator.

      (c) Perform the power accuracy test in paragraph 4-5.

b. If only the -50 dBm power accuracy readings (60 on step attenuator dial) are out of tolerance, recheck the appropriate channel's low-level calibration (paragraph 4-3.2 m and/or o).

c. If the R input power accuracy readings are out of tolerance, perform the Channel R checks and adjustments of paragraph 5-4.1. After performing these checks and adjustments, recheck Channel R power accuracy.

4-5 POWER ACCURACY TEST USING DC VOLTAGE STANDARD

This test uses highly-accurate (0.0005%) dc voltages to simulate input RF power for 560A power accuracy verification. The test in this paragraph may be used to isolate the RF detector as a possible-error-producing source in log amplifier power accuracy tests. To connect the dc voltages to the log amplifier input requires a special connector test jig. Instructions, along with a parts list, for building this connector test jig are given in Figure 4-11. The EDC Model 501 DC Power Supply (Table 4-1) may be used to supply the dc voltages. To perform this test, proceed as follows:

a. Connect equipment, with the exception of the RF detector, as shown in Figure 4-1 (page 4-3).

b. Position 560A controls as follows:

CHANNEL A ON: On
INPUT: A
MEMORY: Off
dB PER DIVISION: .2
REFERENCE dB/dBm: dBm
OFFSET: See Table 4-4
OFFSET ZERO: Not depressed
CHANNEL B ON: Off
INPUT: B
MEMORY: Off
dB PER DIVISION: .2
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
MARKER THRESHOLD: Off
REFRESH: On
REFRESH HOLD: Off
SMOOTHING: MAX

c. On 560A, press REF POS LOCATE and adjust the SET potentiometer to position trace on center graticule line.

d. Connect the special connector test jig (Figure 4-11) to the front panel "A" connector.

e. Connect the black lead of the test jig to the negative (-) terminal on the floating-ground power supply.

f. Connect the red lead of the test jig to the positive (+) terminal on the floating-ground power supply.

g. Connect the shield lead of the test jig to the ground terminal on the floating-ground power supply.

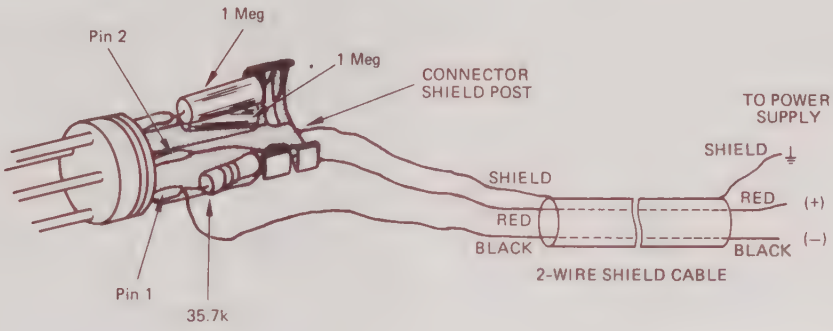
h. On the power supply, adjust the controls to provide voltage number 1 in Table 4-4.

i. On 560A, adjust OFFSET to position trace on center graticule line. The OFFSET dB display should read the dBm value that corresponds to voltage number 1 in Table 4-4.

j. Repeat steps h and i for the remaining voltages in Table 4-4.

Table 4-4. Equivalency Chart, DC Voltage to dBm

DC Voltage	OFFSET dB Reading
1. -1.462V	+16, ±0.2
2. -0.6208V	+9, ±0.2
3. -0.2449V	+2, ±0.2
4. -86.94 mV	-5, ±0.2
5. -26.13 mV	-12, ±0.2
6. -6.268 mV	-19, ±0.2
7. -1.313 mV	-26, ±0.2



Fabricate special connector test jig as follows:

1. Solder one end of the 35.7 kΩ resistor to pin 1. Solder the other end of the 35.7 kΩ resistor to the shield post and to pin 2.

2. On the 2-wire shielded cable, solder the black lead to pin 1. Solder both the red and shield leads to the connector shieldpost.

3. Solder 1 MΩ resistor to pin 3. Solder the other resistor lead to shieldpost.

4. Solder 1 MΩ resistor to pin 4. Solder the other resistor lead to shieldpost.

Special Connector Parts List

Part Description	Part Number	Vendor
Connector, Plug	09CL4M	Switchcraft, Inc.
Shielded Wire, 2-conducted, 22 ga.	2464	Belden
Resistor, Metal Film, 1 MΩ, 1/8W, 0.1% (2 each)	EMF55T9-1 Meg-0.1% ——— RNC55J1DO4BS	Dale Elect. ——— Mil. Spec.
Resistor, Metal Film, 35.7 kΩ, 1/8W, 1/8W, 0.1%	EMF55FT9-35.7k-0.1%	Dale Elect.

Figure 4-11. Fabrication Instructions for Special Connector Used With DC Voltage Standard

4-6 DIRECTIVITY MEASUREMENTS

Directivity measurements are frequency-limited. Above 2 GHz, a technique employing an air line is used to make a precise measurement of directivity.* Below 2 GHz, where the air line is not effective, an oscilloscope is used to compare the directivity of the bridge or SWR Autotester against a calibrated reference in a "Go/No-Go" method. Table 4-6 provides the procedure for measuring directivity using an air line. Table 4-8 provides the procedure for the Go/No-Go method.

Measuring the directivity of the 560-98S50 and -98SF50 SWR Autotesters above 2 GHz requires using a 19SF50 or 19S50 Air Line, respectively. The WSMA connectors on the SWR Autotesters and air lines have been designed for mating with SMA connectors. When two WSMA connectors are mated, they require a washer for pin-depth compensation of the center conductors. The only exceptions are the WSMA open/short and the sweep generator RF OUTPUT connector, which have been optimized for use with WSMA. An envelope containing six or more of these washers has been packaged with each air line. Table 4-5 provides instructions for installing these washers. Before starting the procedure in Table 4-5, perform the following steps:

a. Press the POWER pushbutton on the 560A and 6637A. Set the 560A controls as shown in Figure 4-12.

b. On the 6637A:

   1. Press RESET.

   2. Press F1-F2.

   3. Press F1 and set for 2 GHz.

c. On the 560A:

   1. Press REF POS LOCATE and adjust the SET potentiometer to position the reference trace on the center graticule line; release REF POS LOCATE.

   2. Adjust OFFSET for a 00.0 reading on the OFFSET dB display.

   3. Adjust ZERO dB SET to position the trace on the center graticule line.

   4. Press dB PER DIVISION 1.

   5. Proceed to Table 4-5.

4-7 PIN DEPTH MEASUREMENTS

The following procedure provides instructions for measuring the pin depth of GPC 7 and type N male and female connectors. Instructions for measuring pin depth on WSMA connectors are given in the instruction sheet for the Model 01-160 Gauging Set.

Pin depth is a critical specification on the connectors of detectors and SWR Autotesters. It should be checked periodically to ensure that these connectors meet the specified tolerances listed in Table 4-9.

a. GPC 7 Connectors

   1. Calibrate the gauge for zero, as follows:

      (a) Press the gauge against the calibrated gauge block.

      (b) Loosen the knurled knob and turn the serrated ring until the "0" on the dial aligns with the pointer. Tighten the knob.

   2. Press the measurement plane of the gauge against the center conductor on the connector to be measured.

   3. Read the pin depth setting.

   4. If the setting is out of tolerance, the bridge or SWR Autotester should be returned to WILTRON for repair.

b. Type N-Male Connectors

   1. Install the adapter stamped "N" M over the gauge plunger mechanism.

*Error Averaging is the Technique used. This technique is described in WILTRON Technical Review #8, "An Easy-to-Use Method for Measuring Small SWRs to Better Than Computer-Aided Accuracy Levels."

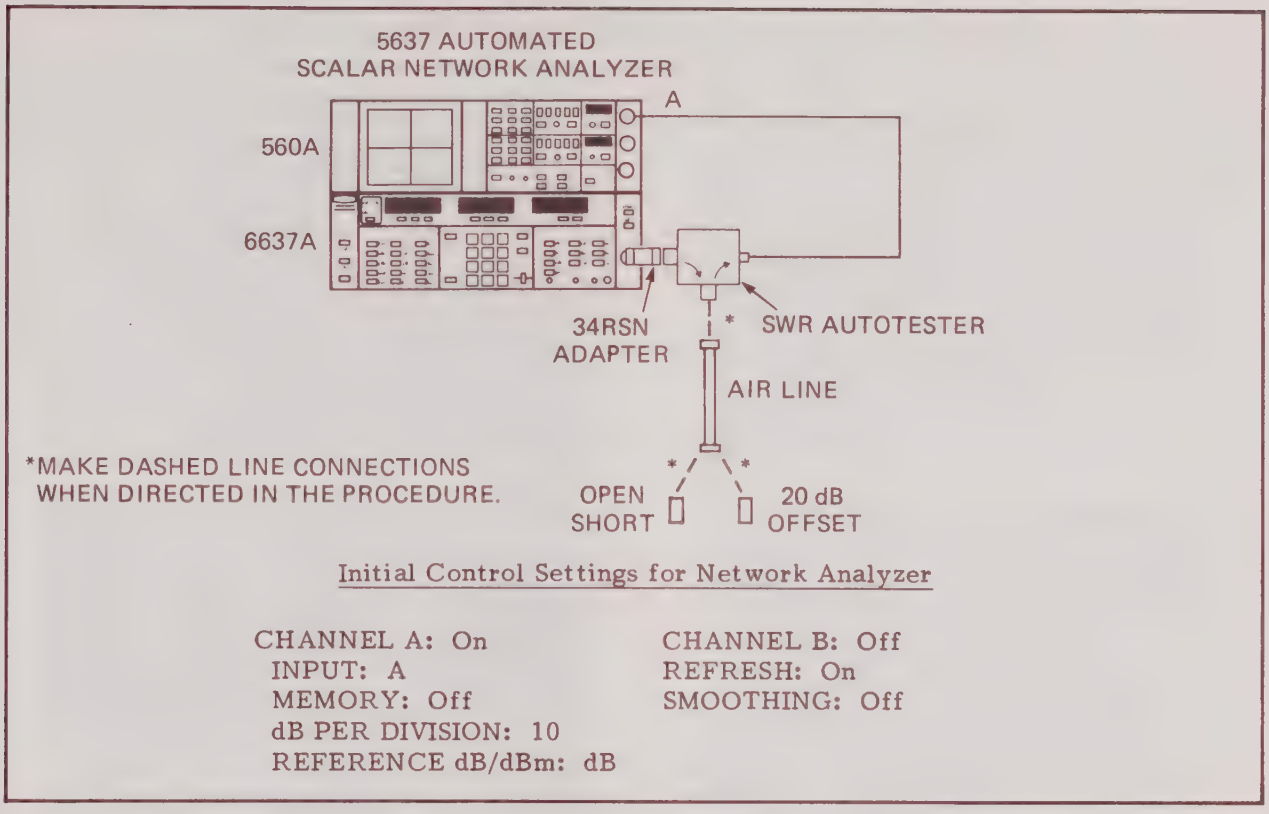


Figure 4-12. Test Setup for Measuring Directivity Above 2 GHz

2. Calibrate the guage for zero, as follows:

   (a) Insert the measuring plunger into the sleeve in the "M" half of the calibration device.

   (b) Loosen the knurled knob and turn the serrated ring until the "0" aligns with the pointer.

3. Install the measuring plunger over the center pin on the connector to be measured.

4. Read the pin depth setting.

5. If the setting is out of tolerance, the bridge or SWR Autotester should be returned to WILTRON for repair.

c. Type N-Female Connectors

1. Install the adapter stamped "N_F" over the guage plunger mechanism.

2. Calibrate the guage for zero, as follows:

   (a) Insert the protrusion on the "F" half of the calibration device into the sleeve on the guage adapter.

   (b) Loosen the knurled knob and turn the serrated ring until the "0" aligns with the pointer.

3. Install the measuring plunger over the center pin on the connector to be measured.

4. Read the pin depth setting.

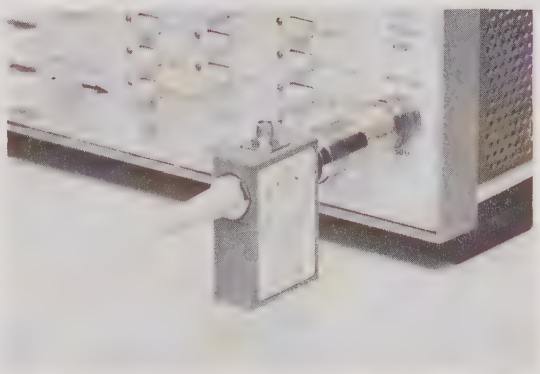
5. If the setting is out of tolerance, the bridge or SWR Autotester should be returned to WILTRON for repair.

Table 4-5. Washer Installation and Component Mating Procedure

1. Separate a washer, and trim away the tabs.

560-98SF SWR AUTOTESTER WITH 19S50 AIR LINE

2. Connect the SWR Autotester to the sweep generator (test port up).



OR

560-98S50 SWR AUTOTESTER WITH 19SF50 AIR LINE

Connect the SWR Autotester to the sweep generator (test port down).

3. Connect the open end of the open/short to the beaded end of the air line.

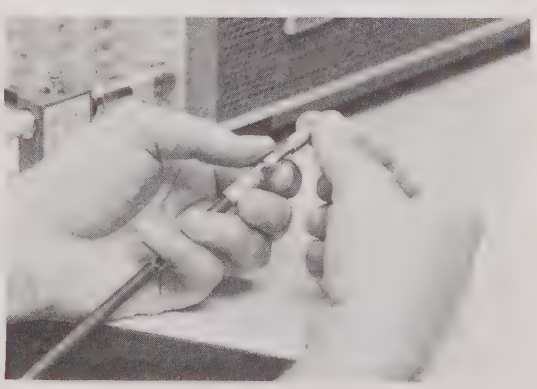


Table 4-5. Washer Installation and Component Mating Procedure (Continued)

560-98 SWR AUTOTESTER WITH 19S50 AIR LINE

4. Insert the washer into the opening of the SWR Autotester test port connector.

OR

560-98 SWR AUTOTESTER WITH 19SF50 AIR LINE

Insert the washer into the beadless end of the air line.

5. • Tilt the air line horizontally.
   • Align the center conductor with the center of the connector opening.

6. • Loosen the RF INPUT connection and rotate the SWR Autotester as shown.
   • Align the test port with the air line.
   • Carefully mate the two connectors.

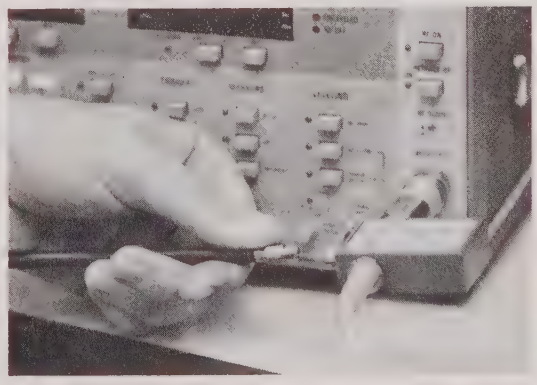
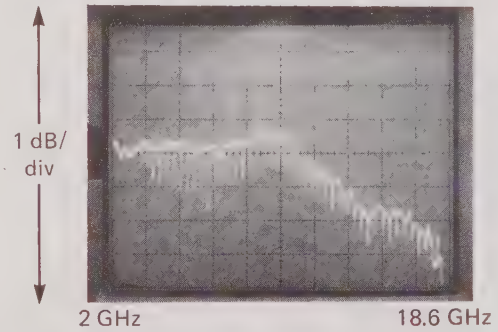


Table 4-5. Washer Installation and Component Mating Procedure (Continued)

NOTE

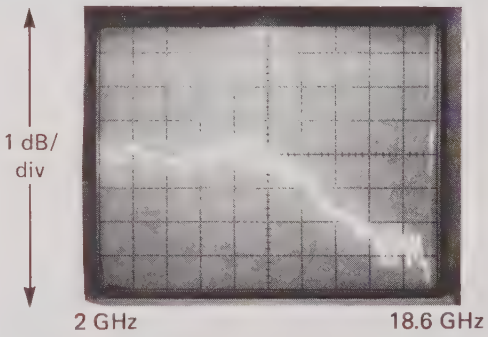
Orienting the air line horizontally usually makes effecting a good connection easier (determining when the center conductor is centered is easier). Horizontal orientation is not the only way, however. A good connection may also be effected when the air line is oriented vertically.

7. While observing the network analyzer display, begin by slowly tightening the connector coupling. While tightening,
   - if Waveform A appears, STOP. The sharp spikes in the waveform indicate improper contact with the center conductor has been made. Uncouple the connectors, examine the washer for damage, and repeat steps 5 thru 7.
   - if Waveform B appears, a good connection has been made. Continue tightening the coupling, but DO NOT OVER-TORQUE. Finger-tight is sufficient.



WAVEFORM A

Bad center-pin mating between air line and SWR Autotester



WAVEFORM B

Good center-pin mating between air line and SWR Autotester

8. Rotate the SWR Autotester clockwise, until the air line is vertical; tighten the RF INPUT connection.
9. Separate another washer (step 1) and install it in the Model 29S50-20 or 29SF50-20 20 dB offset.
10. Proceed with the directivity measurements in Table 4-6, beginning with step 7.

Table 4-6. Procedure for Measuring Directivity Above 2 GHz

1. Connect the test equipment as shown in Figure 4-12.

2. Press POWER on both instruments and set the 560A controls to their initial settings.

3. On the 6637A,

   a. Press RESET.

   b. Press F1-F2.

   c. Press F1 and set for 2 GHz.

   d. Press F2 and set for 18 GHz.

4. On the 560A,

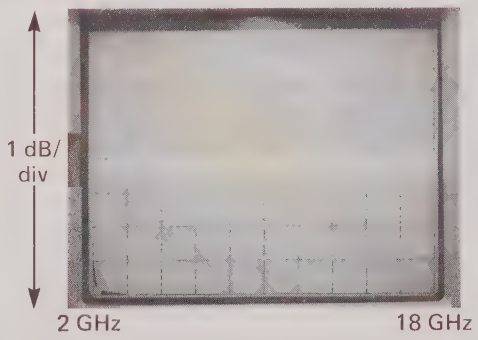
   a. Press REF POS LOCATE and adjust the SET potentiometer to position the reference trace on the center graticule line; release REF POS LOCATE.

   b. Adjust OFFSET for a 00.0 reading on the OFFSET dB display.

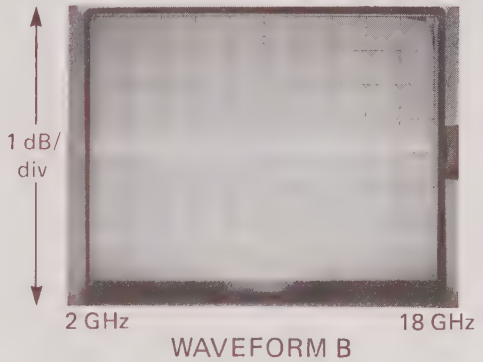
   c. Adjust ZERO dB SET to position the trace on the center graticule line.

5. Connect the Open to the beaded end of the air line.

6. Connect the beadless end of the air line to the test port, as shown in Figure 4-10. If, after tightening the air line connector, the 560A trace has spikes like those shown in Waveform A, below, the center conductor is not making a good connection. Disconnect the air line, remate the center conductor, and retighten the connector. Waveform B, below, indicates a good connection.



WAVEFORM A

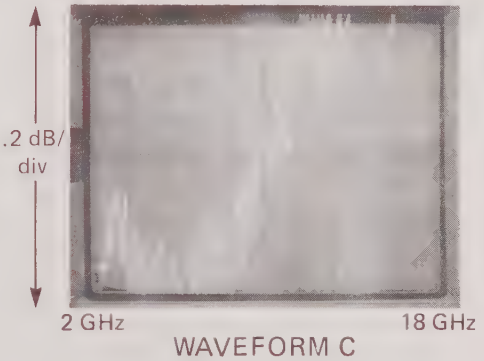


WAVEFORM B

7. On the 560A,

   a. Press dB PER DIVISON .2.

   b. Press STORE TRACE. The display should resemble Waveform C, below.



WAVEFORM C

8. Remove the Open and install the Short.

9. On the 560A, sequentially press MEMORY AVG, STORE TRACE, and SUBTRACT. The trace should resemble Waveform D, below.

WAVEFORM D

Table 4-6. Procedure for Measuring Directivity Above 2 GHz (Continued)

10. Remove the Short and install the 20 dB Offset.

NOTE

For the 19S50 and 19SF50 Air Lines: After the open and short have been averaged and the 20 dB offset has been attached, slightly loosening and retightening the connections between the test port and air line may improve center-conductor mating, thereby resulting in a lower-amplitude peak-to-peak ripple pattern (higher directivity).

11. On the 560A,

a. Press dB PER DIVISION 1.

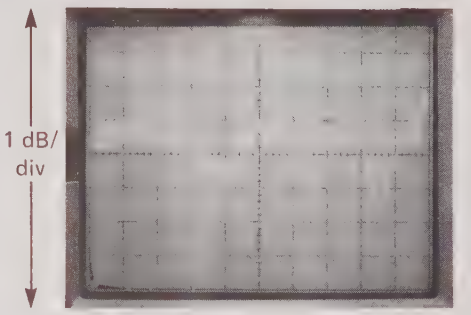
b. Adjust OFFSET to position the trace near center screen. The OFFSET dB display should read approximately, -20.0.

c. Select the ripple with the greatest peak-to-peak value and position its average point (see NOTE) on the center graticule line.

NOTE

The average point is approximately halfway between the peak and trough values for ripples 3 dB or less. For ripples greater than 3 dB, refer to Table 4-7 to find the average value.

d. The display should resemble Waveform E, below.



WAVEFORM E

e. Note the OFFSET dB display. This is the value of the 20 dB Offset.

f. Measure the peak-to-peak value of the selected ripple.

12. Refer to the RF Measurement Chart in Table 4-7 for the following steps:

a. In the "REF ±x, Peak to Peak Ripple, dB," column, find the value nearest to the peak-to-peak signal value measured in step 9f.

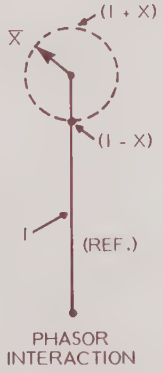
b. Read the coordinate value from the "x dB Below Reference" column.

c. Add the dB value from step b., above, to the OFFSET dB value measured in step 9e. This sum is the SWR Autotester's or bridge's worst-case directivity. It should equal or exceed the specification in Table 1-2.

Table 4-7. Microwave Measurement Chart

Conversion tables for Return Loss, Reflection Coefficient, and SWR
with tabular values for interactions of a small phasor x with a large phasor (unity reference)
expressed in dB related to reference.

			RELATIVE TO UNITY REFERENCE			
SWR	REFLECTION COEFFICIENT	RETURN LOSS dB	X dB BELOW REFERENCE	REF + X dB	REF - X dB	REF ± X PEAK TO PEAK RIPPLE dB
17.3910	.8913	1	1	5.5350	-19.2715	24.8065
8.7242	.7943	2	2	5.0780	-13.7365	18.8145
5.8480	.7079	3	3	4.6495	-10.6907	15.3402
4.4194	.6310	4	4	4.2489	-8.6585	12.9073
3.5698	.5623	5	5	3.8755	-7.1773	11.0528
3.0095	.5012	6	6	3.5287	-6.0412	9.5699
2.6146	.4467	7	7	3.2075	-5.1405	8.3480
2.3229	.3981	8	8	2.9108	-4.4096	7.3204
2.0999	.3548	9	9	2.6376	-3.8063	6.4439
1.9250	.3162	10	10	2.3866	-3.3018	5.6884
1.7849	.2818	11	11	2.1567	-2.8756	5.0322
1.6709	.2512	12	12	1.9465	-2.5126	4.4590
1.5769	.2239	13	13	1.7547	-2.2013	3.9561
1.4935	.1995	14	14	1.5802	-1.9331	3.5133
1.4326	.1778	15	15	1.4216	-1.7007	3.1224
1.3767	.1585	16	16	1.2778	-1.4988	2.7766
1.3290	.1413	17	17	1.1476	-1.3227	2.4703
1.2880	.1259	18	18	1.0299	-1.1687	2.1986
1.2528	.1122	19	19	.9237	-1.0337	1.9574
1.2222	.1000	20	20	.8279	-.9151	1.7430
1.1957	.0891	21	21	.7416	-.8108	1.5524
1.1726	.0794	22	22	.6639	-.7189	1.3828
1.1524	.0708	23	23	.5941	-.6378	1.2319
1.1347	.0631	24	24	.5314	-.5661	1.0975
1.1192	.0562	25	25	.4752	-.5027	.9779
1.1055	.0501	26	26	.4248	-.4466	.8714
1.0935	.0447	27	27	.3796	-.3969	.7765
1.0829	.0398	28	28	.3391	-.3529	.6919
1.0736	.0355	29	29	.3028	-.3138	.6166
1.0653	.0316	30	30	.2704	-.2791	.5495
1.0580	.0282	31	31	.2414	-.2483	.4897
1.0515	.0251	32	32	.2155	-.2210	.4365
1.0458	.0224	33	33	.1923	-.1967	.3890
1.0407	.0200	34	34	.1716	-.1751	.3467
1.0362	.0178	35	35	.1531	-.1558	.3090
1.0322	.0158	36	36	.1366	-.1388	.2753
1.0287	.0141	37	37	.1218	-.1236	.2454
1.0255	.0126	38	38	.1087	-.1100	.2187
1.0227	.0112	39	39	.0969	-.0980	.1949
1.0202	.0100	40	40	.0864	-.0873	.1737
1.0180	.0089	41	41	.0771	-.0778	.1548
1.0160	.0079	42	42	.0687	-.0693	.1380
1.0143	.0071	43	43	.0613	-.0617	.1230
1.0127	.0063	44	44	.0546	-.0550	.1096
1.0113	.0056	45	45	.0487	-.0490	.0977
1.0101	.0050	46	46	.0434	-.0436	.0871
1.0090	.0045	47	47	.0387	-.0389	.0776
1.0080	.0040	48	48	.0345	-.0346	.0692
1.0071	.0035	49	49	.0308	-.0309	.0616
1.0063	.0032	50	50	.0274	-.0275	.0549
1.0057	.0028	51	51	.0244	-.0245	.0490
1.0050	.0025	52	52	.0218	-.0218	.0436
1.0045	.0022	53	53	.0194	-.0195	.0389
1.0040	.0020	54	54	.0173	-.0173	.0347
1.0036	.0018	55	55	.0154	-.0155	.0309
1.0032	.0016	56	56	.0138	-.0138	.0275
1.0028	.0014	57	57	.0123	-.0123	.0245
1.0025	.0013	58	58	.0109	-.0109	.0219
1.0022	.0011	59	59	.0097	-.0098	.0195
1.0020	.0010	60	60	.0087	-.0087	.0174



PHASOR INTERACTION

Table 4-8. Direct, Go/No-Go Method of Measuring Directivity

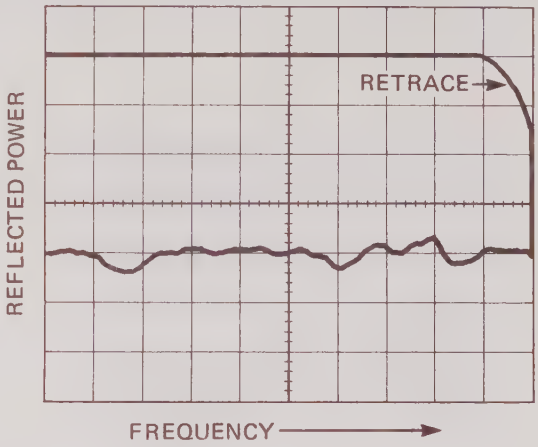
1. Set up the equipment as shown in Figure 4-13. Position the oscilloscope and step attenuator controls as shown. Do not connect the termination to the test port.

2. On the 6609A, press RESET. (Frequency sweep: .01 to 2 GHz.)

3. On the step attenuator, position the control to a dB setting equal to the SWR Autotester directivity, as specified in Table 1-2.

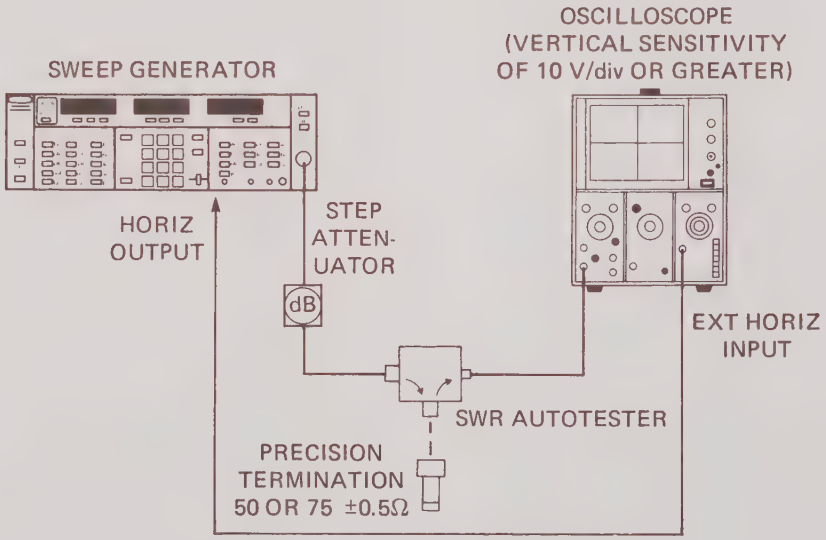
4. On the oscilloscope, adjust the vertical controls to position the frequency plot (see below) on a convenient reference line.

5. Connect the termination to the test port of the SWR Autotester.



6. On the step attenuator, set the control to 0 dB.

7. Observe the oscilloscope display. If the measured directivity signal is above the reference line, the directivity exceeds that specified in Table 1-2.



Initial Settings for Oscilloscope and Attenuator Controls

Oscilloscope
- Vertical Input: DC
- Vertical Input Polarity: Positive (+)
- Vertical Sensitivity: 10 μV/division
- Horizontal Input: External (sweep off)
- Power: On

Step Attenuator
- 0 dB

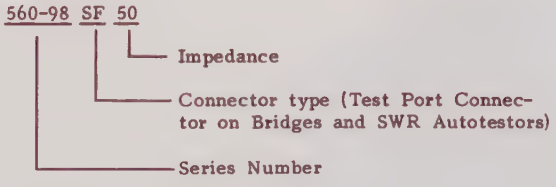
Figure 4-13. Equipment Setup for Direct, Go/No-Go Test

Table 4-9. Pin depth Tolerance for 560 Detectors and SWR Autotesters

SERIES	PORT/CONNECTOR TYPE	PIN DEPTH (Mils)	MMC GAUGE READING[1]
560-98 SWR Autotesters	TEST-A	+0.000 -0.003	same as Pin Depth
	TEST-N	207 -0.000 +0.002	210 -0.003 +0.001
	TEST-NF	207 +0.000 -0.002	same as Pin Depth
	TEST-S[2]	-0.0025 -0.0035	
	TEST-SF[2]	-0.0003 -0.0007	
	INPUT-RS	-0.0003 -0.0007	
	TEST-K	+0.000 -0.002	
	INPUT-KF	+0.000 -0.003	
560-7 RF Detectors	INPUT-N	207 -0.000 +0.006	210 -0.003 +0.003
	INPUT-A	+0.000 -0.003	same as Pin Depth
	INPUT-S	-0.001 +0.004	
	INPUT-K	+0.000 -0.003	

LEGEND AND NOTES

Typical Model Numbers:



Connector-Type Abbreviations

N = Type N male
NF = Type N female
A = GPC7
S = WSMA male
SF = WSMA female
K = K male
KF = K female

[1]MMC is Maury Microwave Corp.
[2]SMA connectors that mate with WSMA connectors should have the same pin depth tolerance.

SECTION V
CALIBRATION

5-1 INTRODUCTION

This section provides calibration instructions for the Front Panel (A1), Digital (A2), Log Amplifier (A3), and optional GPIB Interface (A6) PCBs. The instructions in this section should not be performed unless the performance verification instructions in Section IV indicate that an out-of-tolerance condition exists.

5-2 GAINING ACCESS TO THE 560A PRINTED CIRCUIT BOARDS

The 560A Scalar Network Analyzer is produced in two configurations, horizontal and vertical (Option 2), and is composed of two main assemblies, network analyzer and CRT mainframe. The network analyzer and CRT mainframe PCBs in either 560A configuration are readily accessible. How to gain access to these PCBs is described below:

Horizontal Configuration

To gain access to the network analyzer PCBs, remove the two straight brackets and the two left-corner brackets from the rear of the 560A (Figure 5-1), and slide the bottom cover to the rear; to gain access to the CRT mainframe PCBs, remove the two right-corner brackets in addition to the two straight brackets, and slide the top cover to the rear.

Vertical Configuration

To gain access to the network analyzer PCBs, remove the two straight brackets and the two bottom-corner brackets from the rear of the 560A (Figure 5-2), and slide the bottom cover to the rear; to gain access to the CRT mainframe PCBs, remove the two top-corner brackets in addition to the two straight brackets, and slide the top

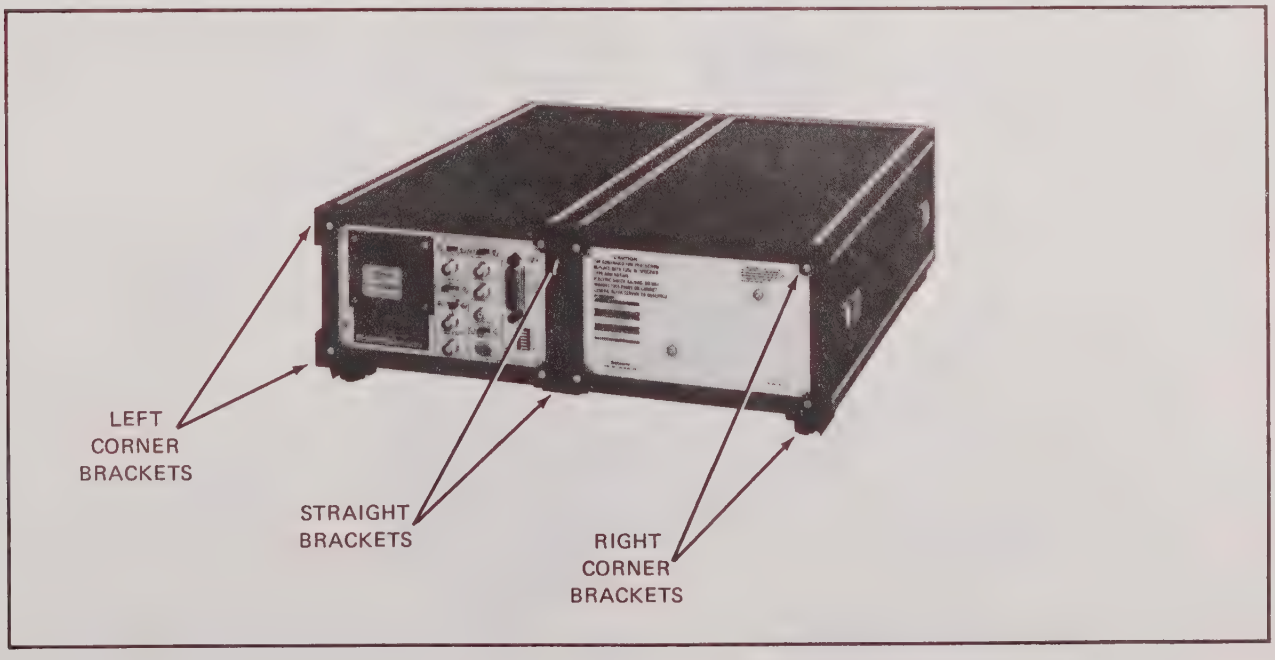


Figure 5-1. Rear Panel Brackets, 560A Horizontal Chassis

cover to the rear. Figure 5-3 shows a vertical chassis with the network analyzer PCBs exposed.

5-3 FRONT PANEL (A1) AND DIGITAL (A2) PCB ADJUSTMENTS

The adjustments required to calibrate the front panel and digital PCB circuits are described in the following paragraphs. The calibration of these two PCBs requires a digital voltmeter and a sweep generator. The sweep generator interconnections and initial control positioning for the WILTRON 6647A Programmable Sweep Generator are

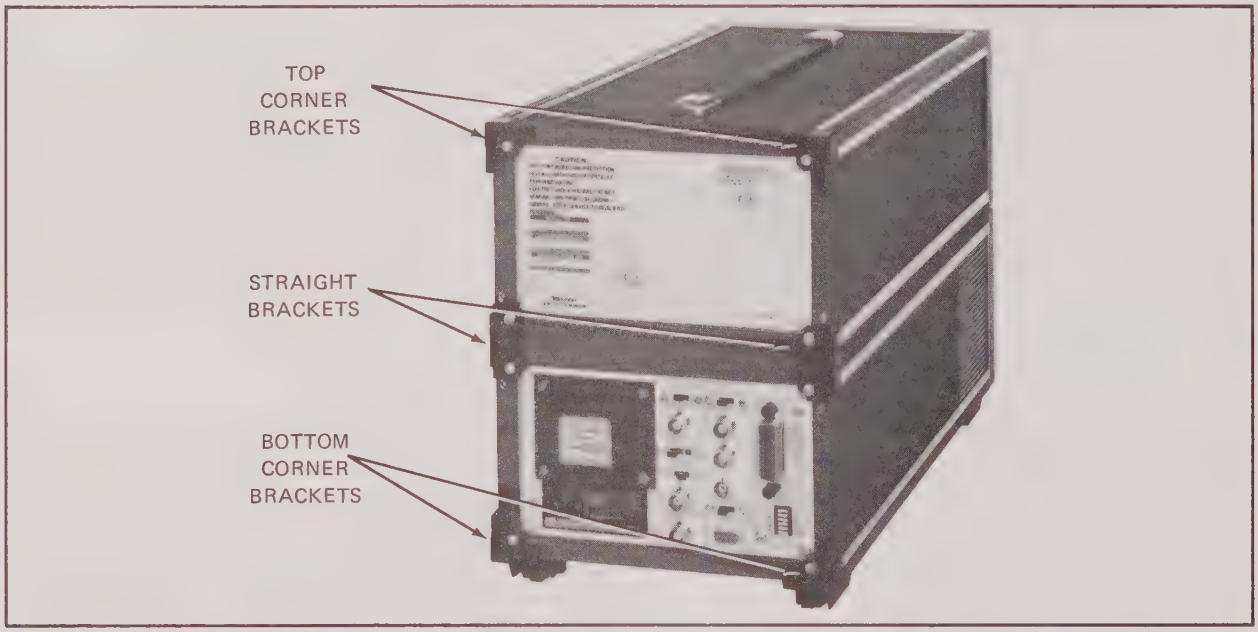


Figure 5-2. Rear Panel Brackets, 560A Vertical Chassis

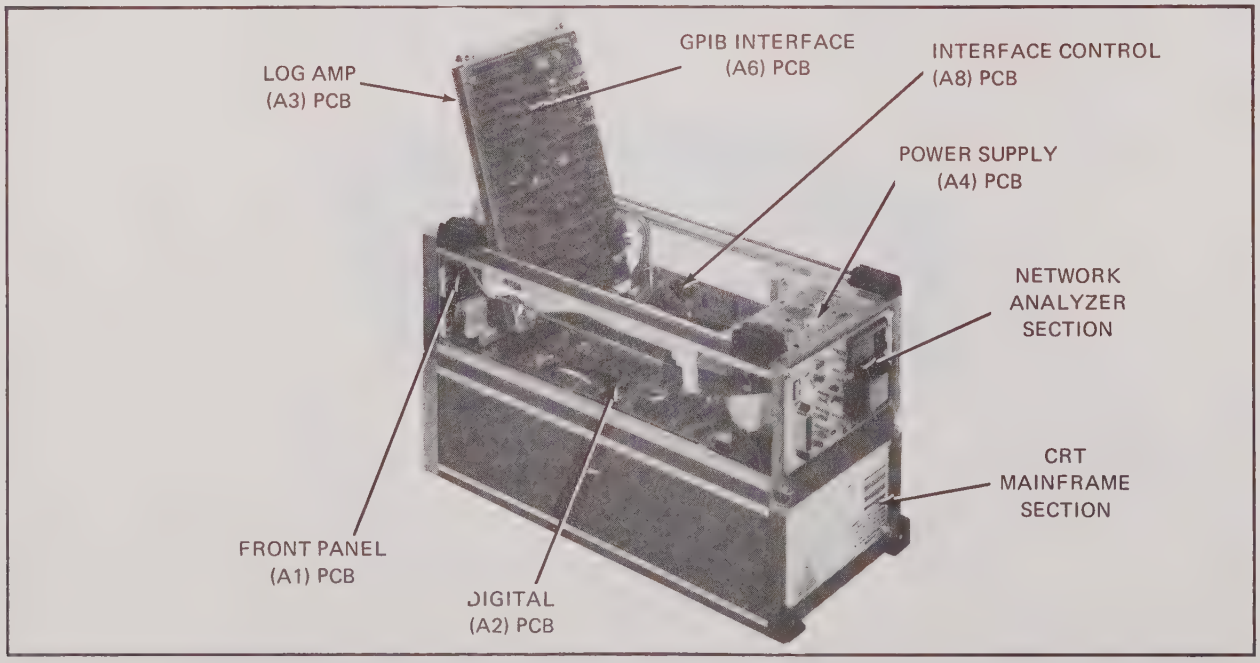
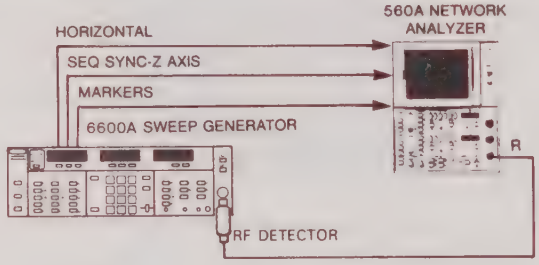


Figure 5-3. Vertical Chassis With Network Analyzer Exposed

shown in Figure 5-4.

NOTE

Reference to top and bottom of the CRT in the following procedures is viewed with the 560A upside down (Figure 5-3).



MARKER: VIDEO
AMPLITUDE: Fully CCW
TRIGGER: AUTO
SWEEP TIME: 100 ms
FREQUENCY SELECTOR: F1-F2
RETRACE RF: ON
F1: Lower frequency of interest
F2: Higher frequency of interest
LEVELING: INTERNAL
POWER: ON
RF: ON
LEVEL: Maximum Leveled Power
560A
OUTPUT MODE (rear panel): CRT

Figure 5-4. Digital PCB Calibration Equipment Setup Using WILTRON 6600A Series Programmable Sweep Generator

5-3.1 Power Supply Checks and OFFSET dB Display Reference Voltage Check and Adjustment

This paragraph provides instructions for checking the +15V, -15V, and +5V power supply output voltages, plus the +1.000Vdc input reference voltage for the Channel A and Channel B OFFSET dB digital voltmeter displays. Instructions for adjusting the OFFSET dB reference voltage are also included. The power supply voltage checks contain no corresponding adjustment instructions; there are no adjustments for these voltages. If any of the three power supply voltages are out of tolerance, the power supply (A4) PCB is faulty. To perform voltage checks, proceed to subparagraph a, below. If the +1.000 volt OFFSET dB display reference voltage is out of tolerance, perform the voltage adjustment outlined in subparagraph b, below.

a. Voltage Checks

1. Connect 560A to sweep generator and position sweep generator controls as shown in Figure 5-4.

2. Gain access to the network analyzer digital and front panel PCBs; refer to paragraph 5-2.

3. Depress POWER pushbutton.

4. Connect DVM test leads to A2TP1 (common) (see Figure 5-14 for location) and A2TP2. Verify that meter indicates +15.0 ±0.6 Vdc.

5. Connect DVM test leads between A2TP1 (common) and A2TP3. Verify that meter indicates -15.0 ±0.6 Vdc.

6. Connect DVM test leads between A2TP1 (common) and A2TP4. Verify that meter indicates +5.0 ±0.2 Vdc.

7. Connect DVM test leads between A1TP1 (see Figure 5-13 for location) and A1TP2 (common). Verify that meter indicates +1.000V ±1.0 mVdc.

CAUTION

To adjust A1R73 in b below, use a tubular adjustment tool with a recessed screwdriver tip (General Cement (GC) part number 8276, or equivalent). A1R73 is difficult to reach; the use of a normal screwdriver may result in the screwdriver's slipping from the potentiometer screw slot and damaging the A1 PCB.

b. OFFSET dB Reference Voltage Adjustment. With DVM connected between A1TP1 and A1TP2, adjust potentiometer A1R73 for +1.000 Vdc.

5-3.2 Horizontal Clamp and CRT Mainframe HORIZ POSITION and X-Gain Adjustments

This paragraph provides instructions for aligning the CRT mainframe horizontal deflection with the network analyzer normalized 0-10 V input horizontal sweep ramp. To perform these adjustments, proceed as follows:

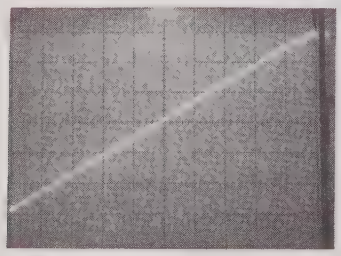
a. Perform voltage checks per paragraph 5-3.1.

b. Position 560A controls as follows (controls not identified may be in any position):

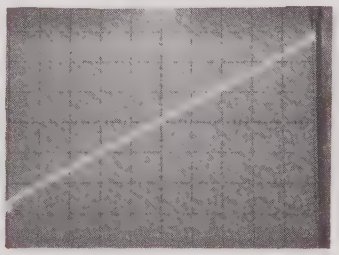
CHANNEL A ON: On
INPUT: R
MEMORY: Off
dB PER DIVISION: 17 (10, 5, & 2 depressed)
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
OFFSET: +50.0
MARKER THRESHOLD: Off
REAL TIME: On
SMOOTHING: Off

c. Position A3 PCB TEST-NORMAL switch to TEST.

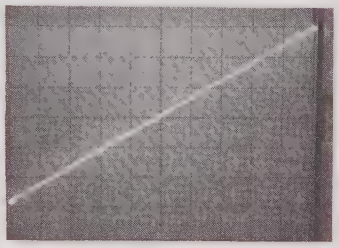
d. Adjust OFFSET to position trace so that both ends can be observed; see waveform below.



e. Adjust front panel HORIZ START screwdriver potentiometer until right end of trace, as observed on CRT, begins to intensify and clamping starts. Clamping is indicated when the trace stops rising diagonally and either "shoots up" (right end) or "drops off" (left end) vertically. See waveform below.



f. Adjust HORIZ STOP potentiometer until left end of trace starts clamping. An example of a properly adjusted waveform is shown below.



g. Select manual sweep on sweep generator to Manual and adjust its control fully CCW (to low end of band). Connect DVM between HORIZONTAL OUTPUT, on rear panel of 560A, and chassis. Meter should indicate zero ±0.2 volts (OUTPUT MODE switch in CRT position).

h. Adjust manual sweep control fully CW (to high end of band). DVM should indicate +10.0 ±0.2Vdc. If meter does not indicate correct voltage, refer to HORIZ STOP troubleshooting chart, Figure 7-7.

i. Select AUTO mode on sweep generator.

NOTE

If no other calibration adjustments are to be performed, complete steps

j and k, and proceed to step n (skip step m). However, if additional calibration adjustments are required, disregard steps j and k and proceed to step m.

j. Position A3 PCB TEST-NORMAL switch to NORMAL.

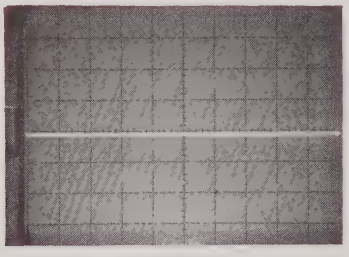
k. Refasten A3 PCB to chassis and position 560A upright.

m. (See NOTE above.) Depress INPUT A lightly so that all three Channel A INPUT switches are released.

n. Adjust OFFSET control until trace is positioned on center graticule line.

o. Adjust CRT mainframe HORIZ POSITION control to position left end of trace on left graticule edge.

p. Adjust CRT mainframe X-Gain potentiometer to position right end of trace on right graticule edge (Figure 5-12). The HORIZ POSITION control and X-Gain potentiometer are interactive; repeat steps o and p until trace is positioned as shown below.



5-3.3 Refresh Horizontal Gain Adjustment (Including X-Y Plot)

This paragraph provides instructions for adjusting the start of the refresh horizontal sweep ramp (R10) and the gains of the refresh sweep ramp in dual-channel sweep (R77), in single-channel sweep (R79) and in single-channel X-Y plot (R81). To perform these adjustments, proceed as follows:

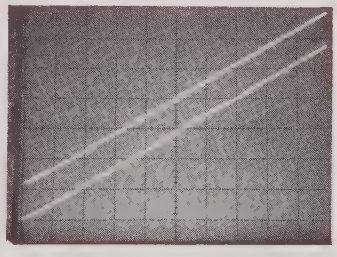
a. Perform voltage checks per paragraph 5-3.1.

b. Perform horizontal clamp and CRT mainframe adjustments per paragraph 5-3.2.

c. Position 560A controls as follows (controls in bold type indicate changes from the previous step):

CHANNEL A ON: On
INPUT: R
MEMORY: Off
dB PER DIVISION: 17 (10, 5, & 2 depressed)
REFERENCE dB/dBm: dBm
OFFSET dB: +50.0
OFFSET ZERO: Not depressed
CHANNEL B ON: On
INPUT: R
MEMORY: Off
dB PER DIVISION: 17 (10, 5, & 2 depressed)
REFERENCE dB/dBm: dBm
OFFSET dB: +40.0
OFFSET ZERO: Not depressed
MARKER THRESHOLD: Off
REFRESH: On
REFRESH HOLD: Off
SMOOTHING: Off
A3 PCB TEST-NORMAL: TEST

d. Adjust both channel OFFSET controls to position traces so that the start (right end) of Channel A refresh ramp (diagonal trace) and the finish (left end) of the Channel B refresh ramp can be observed. See waveform below.



e. Rotate A2R10 (see Figure 5-14 for location) clockwise until trace flattens on the left side; stop rotation.

f. Rotate A2R10 counterclockwise until the trace returns to normal (step d waveform). Continue counterclockwise adjustment for approximately 1/4 turn.

g. Depress CHANNEL B ON pushbutton (turn Channel B off).

h. Depress X-Y PLOT pushbutton and observe intensified dot as it moves across CRT. If dot fails to reach left graticule edge, adjust potentiometer A2R81 clockwise; if dot travels beyond left graticule edge, adjust A2R81 counterclockwise. Repeat, as necessary, until dot reaches left graticule edge before disappearing from CRT.

i. Depress CHANNEL B ON pushbutton.

j. Adjust A2R77 so that both refresh ramp endpoints coincide with left graticule edge.

k. Depress CHANNEL B ON pushbutton (turn Channel B off).

m. Adjust A2R79 so that left end of Channel A refresh ramp coincides with left graticule edge.

n. Readjust A2R10 (steps e and f), if necessary.

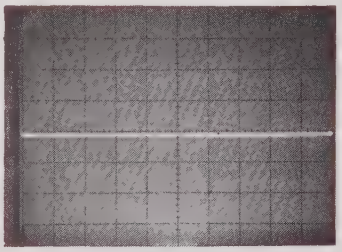
NOTE

If no other calibration adjustments are to be performed, proceed to step o. If additional calibration adjustments are required, however, disregard steps o thru q and proceed to next calibration adjustment paragraph.

o. Refasten A3 PCB to chassis and position 560A upright.

p. Adjust CRT mainframe HORIZ POSITION to position left end of trace on left graticule edge.

q. Adjust CRT mainframe X-Gain potentiometer to position right end of trace on right graticule edge (Figure 5-12). The HORIZ POSITION and X-Gain potentiometers are interactive; repeat steps p and q until trace is positioned as shown below.



5-3.4 Channel A and Channel B OFFSET ZERO Adjustments

This paragraph provides instructions for adjusting the Channel A and Channel B OFFSET ZERO traces so that their position is coincident with their respective channel's REF POS LOCATE trace position. To perform these adjustments proceed as follows:

a. Perform voltage checks per paragraph 5-3.1.

b. Position 560A controls as follows (controls in bold type indicate changes from the previous step):

CHANNEL A ON: **On**
INPUT: R
MEMORY: Off
dB PER DIVISION: .2

REFERENCE dB/dBm: dBm
CHANNEL B ON: Off
INPUT: R
MEMORY: Off
dB PER DIVISION: .2
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
MARKER THRESHOLD: Off
REAL TIME: On
SMOOTHING: Off

c. Depress INPUT A pushbutton lightly so that all three Channel A INPUT switches are released.

d. Depress and hold REF POS LOCATE pushbutton and adjust SET screwdriver potentiometer to position trace on center graticule line.

e. Release REF POS LOCATE.

f. Depress OFFSET ZERO; adjust A2R195 (see Figure 5-14 for location) to position trace on center graticule line.

g. Depress REF POS LOCATE momentarily and insure that trace does not deflect. (Note: Increase sweep generator sweep speed for a steady, non-flickering trace.)

h. Depress (release) OFFSET ZERO.

i. Depress Channel A INPUT R.

j. Depress both CHANNEL A ON and CHANNEL B ON pushbuttons (turn Channel A off and Channel B on).

k. Depress INPUT B pushbutton lightly so that all three Channel B INPUT switches are released.

m. Depress and hold REF POS LOCATE and adjust SET potentiometer to position trace on center graticule line.

n. Release REF POS LOCATE.

o. Depress OFFSET ZERO; adjust potentiometer A2R197 to position trace on center graticule line.

p. Depress REF POS LOCATE momentarily and insure that trace does not deflect. (Note: Increase sweep speed for steady, non-flickering trace.)

q. Depress (release) OFFSET ZERO.

r. Depress Channel B INPUT R.

NOTE

If no other calibration adjustments are to be performed, proceed to step s. If additional calibration adjustments are required, however, disregard step s and proceed to next calibration adjustment paragraph.

s. Refasten A3 PCB to chassis and position 560A upright.

5-3.5 CRT Mainframe Vertical Calibration

This paragraph provides instructions for adjusting the CRT mainframe vertical deflection circuits to be compatible with the 560A vertical signal. To perform these adjustments, proceed as follows:

a. Perform voltage checks per paragraph 5-3.1.

b. Perform Channel A and Channel B OFFSET ZERO adjustments per paragraph 5-3.4

c. Position 560A controls as follows (controls not indicated may be in any position. Controls in bold type indicate changes from the previous step):

CHANNEL A ON: On
INPUT: R
MEMORY: Off
dB PER DIVISION: 5

REFERENCE dB/dBm: dBm
OFFSET: 30.0
OFFSET ZERO: Not depressed
CHANNEL B ON: Off
MARKER THRESHOLD: Off
REAL TIME: On
SMOOTHING: Off
OUTPUT MODE (rear panel): CRT

d. Depress INPUT A pushbutton lightly so that all three Channel A INPUT pushbuttons are released.

e. Depress and hold REF POS LOCATE.

f. Observe CRT and adjust SET screwdriver potentiometer to position trace on next-to-bottom graticule line.

g. Release REF POS LOCATE.

h. Observe CRT and adjust CRT mainframe Y-Gain potentiometer (see Figure 5-12 for location) to position trace on next-to-top graticule line. The CRT mainframe Y-Gain and 560A Reference Position SET potentiometers interact to control vertical deflection; repeat steps e thru h until trace is positioned as described.

i. Connect DVM between rear panel VERTICAL OUTPUT connector center conductor and chassis.

j. Depress and hold REF POS LOCATE.

k. Adjust SET potentiometer for 0.000 ±0.025Vdc, as indicated on DVM.

m. Adjust CRT mainframe Y-Position potentiometer to position trace on center graticule line.

n. Observe CRT and rotate SET potentiometer throughout its entire range. Trace should move smoothly from off-screen top to off-screen bottom. If trace does not deflect as described, refer to Figure 7-5 and troubleshoot the Reference Position SET circuit.

o. Release REF POS LOCATE.

NOTE

If no other calibration adjustments are to be performed, proceed to step p. If additional calibrations are required, however, disregard steps p and q and proceed to next calibration paragraph.

p. Depress INPUT R.

q. Refasten A3 PCB to chassis and position 560A upright.

5-3.6 Storage Memory Digital-to-Analog Converter Calibration

This paragraph provides instructions for calibrating the storage memory digital-to-analog (D/A) converter's gain and offset potentiometers, A2R31 and A2R34, respectively. To perform these adjustments, proceed as follows:

a. Perform voltage checks per paragraph 5-3.1.

b. Perform horizontal clamp and CRT mainframe horizontal deflection adjustments per paragraph 5-3.2.

c. Perform refresh horizontal gain adjustments per paragraph 5-3.3.

d. Perform Channel A and Channel B OFFSET ZERO adjustments per paragraph 5-3.4.

e. Perform CRT mainframe vertical calibration per paragraph 5-3.5.

f. Position 560A controls as follows (controls not indicated may be in any position; controls in bold type indicate changes from previous step):

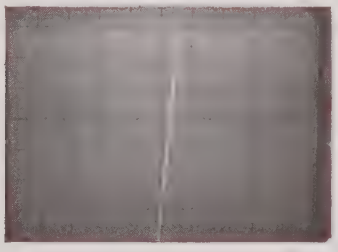
CHANNEL A ON: On
INPUT: R
MEMORY: Off
dB PER DIVISION: 1

REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
OFFSET: +50.0
MARKER THRESHOLD: Off
REAL TIME: On
SMOOTHING: Off
A3 PCB TEST-NORMAL: TEST

g. Depress and hold REF POS LOCATE and adjust SET screwdriver potentiometer to position trace on center graticule line.

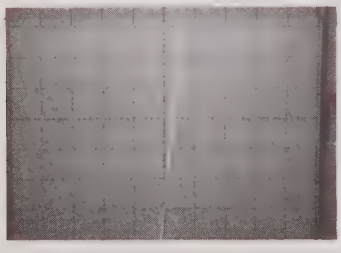
h. Release REF POS LOCATE.

i. Observe CRT. A diagonal trace with a steep slope should be present; see waveform below.



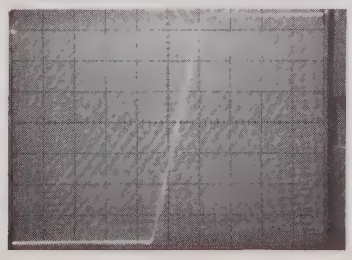
j. Depress STORE TRACE momentarily.

k. Depress RECALL. A digitized trace similar to that observed in step i should be present on CRT. See waveform below.

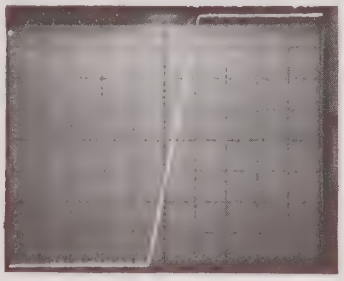


m. Depress 2 dB PER DIVISION pushbutton.

n. Observe CRT; a digitized trace that resembles a backwards Z (see waveform below) should be present.



o. Adjust A2R31 and A2R34 (see Figure 5-14 for locations) so that horizontal elements of the Z-shaped trace are slightly above and below the top and bottom solid graticule lines; see waveform below. (Note: A2R31 adjusts the overall height of the Z, and A2R34 adjusts its vertical offset.)



NOTE

If no other calibration adjustments are to be performed, proceed to step p. If additional calibration adjustments are required, however, disregard steps p thru u and proceed to next calibration adjustment paragraph.

p. Depress MEMORY OFF.

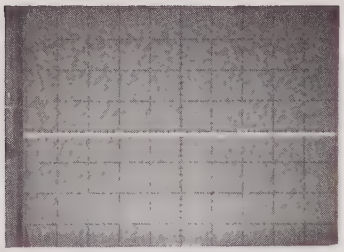
q. Position A3 PCB TEST-NORMAL switch to NORMAL.

r. Refasten A3 PCB to chassis and position 560A upright.

s. Adjust OFFSET control until trace is positioned on center graticule line.

t. Adjust CRT mainframe HORIZ POSITION control to position left end of trace on left graticule edge.

u. Adjust CRT mainframe X-Gain potentiometer to position right end of trace on right graticule edge. The HORIZ POSITION control and X-Gain potentiometer are interactive; repeat steps t and u until trace is positioned as shown below.



5-3.7 Vertical Analog-to-Digital Converter Calibration

This paragraph provides instructions for calibrating the vertical analog-to-digital (A/D) converter's gain and offset potentiometers, A2R19 and A2R24 respectively. To perform these adjustments, proceed as follows:

a. Perform voltage checks per paragraph 5-3.1.

b. Perform horizontal clamp and CRT mainframe horizontal deflection adjustments per paragraph 5-3.2.

c. Perform refresh horizontal gain adjustments per paragraph 5-3.3.

d. Perform Channel A and Channel B OFFSET ZERO adjustments per paragraph 5-3.4.

e. Perform CRT mainframe vertical calibration per paragraph 5-3.5.

f. Perform storage memory digital-to-analog converter calibration per paragraph 5-3.6.

g. Position 560A controls as follows (controls in bold type indicate changes from previous step):

CHANNEL A ON: On
INPUT: R
REFERENCE dB/dBm: dBm
OFFSET: +50.0
OFFSET ZERO: Not depressed
CHANNEL B ON: Off
INPUT: R
dB PER DIVISION: 10
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
MARKER THRESHOLD: Off
REFRESH: On
REFRESH HOLD: Off
SMOOTHING: Off
A3 PCB TEST-NORMAL: TEST

h. Depress and hold REF POS LOCATE and adjust SET screwdriver potentiometer to position trace on center graticule line.

i. Release REF POS LOCATE.

NOTE

Steps j thru o, below, provide a means of observing the output of the vertical A/D converter. The analog input signal is digitized, memorized, recalled and subtracted from a signal of equal value. The subtracted signal is then amplified at .2 dB per division and displayed on the CRT. When the vertical A/D converter gain and offset potentiometers are properly adjusted, the subtracted signal is a straight line ±0.6 dB.

j. Depress MEMORY OFF.

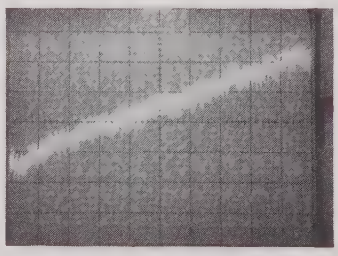
k. Depress 10 dB PER DIVISION pushbutton.

m. Depress STORE TRACE momentarily.

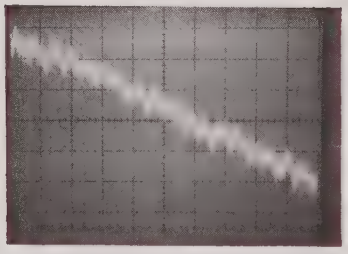
n. Depress SUBTRACT.

o. Depress .2 dB PER DIVISION pushbutton.

p. Observe CRT. A sloping trace similar to either A or B below should appear.



A



B

NOTE

Trace may be off screen. Increase dB PER DIVISION switch settings to either 1, 2, or 5 to bring trace back on screen.

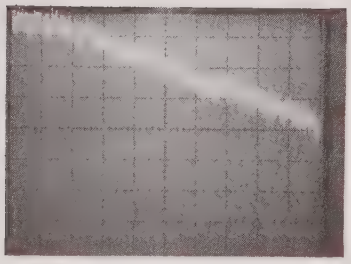
NOTE

In steps q thru y, below, adjustments made to A2R24 (offset) and A2R19 (gain) will have only minimal effects on the trace presently being displayed. Reason: The displayed trace is created, in part, by the storage memory and these two potentiometers affect the signal before it is memorized. The potentiometer's effect will be seen when the A/D converter output is next recalled from memory and displayed, which occurs each time steps j thru o are performed.

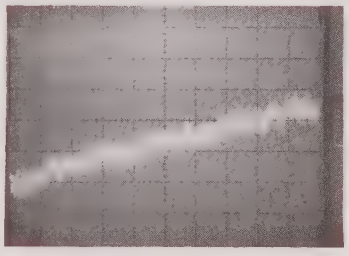
q. If trace observed on CRT is below center graticule line, rotate A2R24 (see Figure 5-14 for location) slightly clockwise. If trace is above center graticule line, rotate A2R24 slightly counterclockwise.

r. Repeat steps j thru o, above.

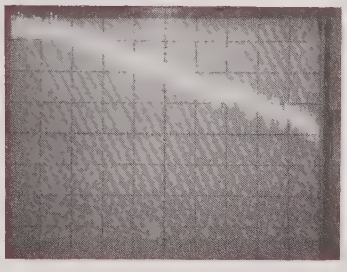
s. Observe CRT with .2 dB PER DIVISION pushbutton depressed. If right trace end is not superimposed on right side of center graticule line, repeat steps j thru q. If right end of trace is positioned as described (see below), proceed with step t.



t. Observe CRT. If trace has a right-to-left downward (negative) slope (waveform A below), adjust potentiometer A2R19 slightly clockwise. Conversely, if trace has a right-to-left upward (positive) slope (waveform B below), adjust A2R19 slightly counterclockwise.



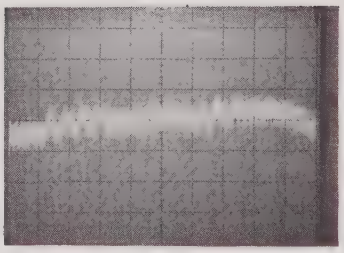
A



B

u. Repeat steps j thru o, above.

v. Observe CRT. If trace still has a slope, repeat steps j thru o and t, above, until trace is level at .2 dB per division of trace deflection. Now, if trace is level and superimposed on center graticule line, as shown below, proceed to step z. However, if trace is level but not centered, proceed to step w.



w. Observe CRT. If level trace is above center graticule line, rotate A2R24 slightly clockwise. Conversely, if level trace is below center graticule line, rotate A2R24 slightly counterclockwise.

x. Repeat steps j thru o, above.

y. Observe CRT. If trace is level and superimposed on center graticule line, proceed to step z. If trace is not centered, repeat steps w thru y until trace is centered.

NOTE

The purpose of steps z thru ah is to balance A2R19 so that the vertical A/D converter has equal gain (slope) for Channel A and Channel B signals.

z. Depress MEMORY OFF.

aa. Depress 10 dB PER DIVISION pushbutton.

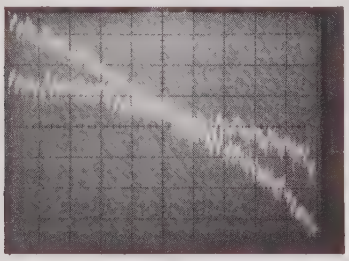
ab. Depress CHANNEL B ON pushbutton (turn Channel B on).

ac. Depress and hold Channel B REF POS LOCATE and adjust SET potentiometer to center Channel B trace on center graticule line.

ad. Adjust Channel B OFFSET control to superimpose Channel B trace over Channel A trace.

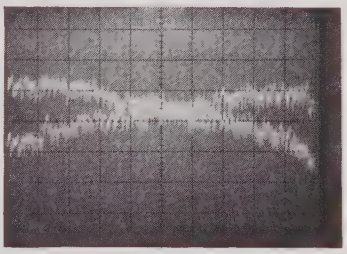
ae. Repeat steps j thru o, above, for both channels.

af. Observe CRT. If the left-to-right excursion of the Channel B trace slopes more than ±3 major divisions from the center graticule line (see waveform below), readjust A2R19 either slightly clockwise or slightly counterclockwise. The direction of A2R19 rotation depends on whether the trace-slope is positive or negative, as described in step t.



ag. Repeat steps j thru o, above, for both channels.

ah. Observe CRT. The ends of the Channel A and Channel B traces, in the criss-cross waveform pattern (see below), should be contained within the 6 major divisions that extend ±3 divisions on either side of the center graticule line. If the distance between the trace ends is as described, the adjustment is complete. If, however, the distance between the trace ends is not correct, repeat steps j thru o, af, and ag, above, until trace end distance is within the ±3 division tolerance.



NOTE

If no other calibration adjustments are to be performed, proceed to step ai. If additional calibration adjustments are required, however, disregard steps ai thru ap and proceed to next calibration adjustment paragraph.

ai. Depress CHANNEL B ON pushbutton (turn Channel B off).

aj. Depress Channel A and Channel B MEMORY OFF.

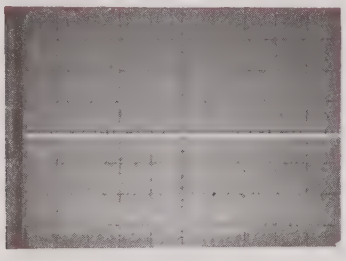
ak. Position A3 PCB TEST-NORMAL switch to NORMAL.

am. Refasten A3 PCB to chassis and position 560A upright.

an. Adjust OFFSET control until trace is positioned to center graticule line.

ao. Adjust CRT mainframe HORIZ POSITION to position left end of trace on left graticule edge.

ap. Adjust CRT mainframe X-Gain potentiometer to position right end of trace on right graticule edge. The HORIZ POSITION control and X-Gain potentiometer are interactive; repeat steps ao and ap until trace is positioned as shown below.



5-3.8 Channel A and Channel B Memory and Subtract Balance Adjustments

This paragraph provides instructions for adjusting the Channel A and Channel B storage memory and memory-subtract balance potentiometers. The storage memory potentiometers, A2R138 and A2R133, are located on the digital (A2) PCB. The memory-subtract balance potentiometers, A1R84 and A1R86, are located on the front panel (A1) PCB. To perform these adjustments, proceed as follows:

a. Perform voltage checks per paragraph 5-3.1.

b. Perform horizontal clamp and CRT mainframe horizontal deflection adjustments per paragraph 5-3.2.

c. Perform refresh horizontal gain adjustments per paragraph 5-3.3.

d. Perform Channel A and Channel B OFFSET ZERO adjustments per paragraph 5-3.4.

e. Perform CRT mainframe vertical calibration per paragraph 5-3.5.

f. Perform storage memory digital-to-analog converter calibration per paragraph 5-3.6.

g. Perform vertical analog-to-digital converter calibration per paragraph 5-3.7.

h. Position 560A controls as follows (controls in bold type indicate changes from previous step):

CHANNEL A ON: On
INPUT: R
MEMORY: Off
dB PER DIVISION: .2
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
CHANNEL B ON: Off
INPUT: R
MEMORY: Off
dB PER DIVISION: .2
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
THRESHOLD: Off
REAL TIME: On
SMOOTHING: Off
A3 PCB TEST-NORMAL: TEST

i. Depress INPUT A pushbutton lightly so that all three Channel A INPUT switches are released.

j. Depress and hold REF POS LOCATE and adjust SET screwdriver potentiometer to position trace on center graticule line.

k. Release REF POS LOCATE.

m. Depress OFFSET ZERO.

n. Depress STORE TRACE momentarily.

o. Depress RECALL.

p. Observe CRT and adjust A2R138 (see Figure 5-14 for location) to position trace on the center graticule line.

q. Depress SUBTRACT.

CAUTION

In step r, A1R84 is difficult to reach, particularly on the horizontal chassis. To reach the potentiometer, place the A3 PCB in the horizontal (closed) position. To perform the adjustment, use an insulated adjustment tool; exercise caution to avoid slipping off the potentiometer and causing damage to the A1 PCB.

r. Observe CRT and adjust A1R84 (see Figure 5-13 for location) to position trace on center graticule line.

s. Depress RECALL and SUBTRACT alternately; there should be no change in trace position. If change is observed, repeat steps p thru s until trace position shows no change.

t. Depress (release) OFFSET ZERO.

u. Depress Channel A INPUT R.

v. Depress CHANNEL B ON and CHANNEL A ON pushbuttons (turn Channel B on and Channel A off).

w. Depress INPUT B pushbutton lightly so that all three Channel B INPUT switches are released.

x. Depress and hold REF POS LOCATE and adjust SET screwdriver potentiometer to position trace on center graticule line.

y. Release REF POS LOCATE.

z. Depress OFFSET ZERO.

aa. Depress STORE TRACE momentarily.

ab. Depress RECALL.

ac. Observe CRT and adjust A2R133 to position trace on center graticule line.

ad. Depress SUBTRACT.

CAUTION

In step ae, A1R86 is difficult to reach, particularly on the horizontal chassis. To reach the potentiometer, place the A3 PCB in the horizontal (closed) position. To perform the adjustment, use an insulated adjustment tool; exercise caution to avoid slipping off the potentiometer and causing damage to the A1 PCB.

ae. Observe CRT and adjust A1R86 to position trace on center graticule line.

af. Depress RECALL and SUBTRACT alternately; there should be no change in trace position. If change is observed, repeat steps ac thru af until trace position shows no change.

ag. Depress (release) OFFSET ZERO.

ah. Depress Channel B INPUT R.

ai. Depress Channel A and Channel B MEMORY OFF pushbuttons.

NOTE

The purpose of the following steps is to recheck the vertical A/D converter's gain and offset.

aj. Depress CHANNEL A ON pushbutton (turn Channel A on).

ak. Depress Channel A and Channel B 10 dB PER DIVISION pushbuttons.

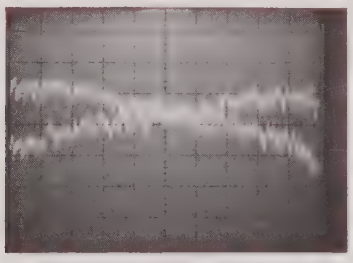
am. Depress REFRESH.

an. Readjust Channel B OFFSET to superimpose Channel B trace on Channel A trace.

ao. Depress Channel A and Channel B STORE TRACE; then SUBTRACT.

ap. Depress Channel A and Channel B .2 dB PER DIVISION pushbuttons.

aq. Observe CRT. The ends of the Channel A and Channel B traces, in the criss-cross waveform pattern (see below), should be contained within the 6 major divisions that extend ±3 divisions on either side of the center graticule line. If the criss-cross waveform pattern is positioned as described, proceed to step ar. If, however, the criss-cross pattern is offset from the center graticule line, readjust A2R24 as described in step w of paragraph 5-3.7.



NOTE

If no other calibration adjustments are to be performed, proceed to step ar. If additional calibration adjustments are required, however, disregard steps ar thru ax and proceed to next calibration adjustment paragraph.

ar. Depress Channel B INPUT R.

as. Depress Channel A and Channel B MEMORY OFF.

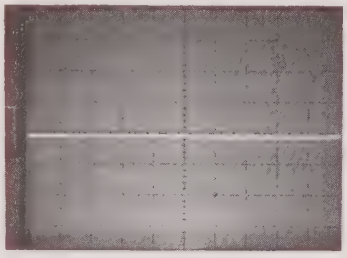
at. Position A3 PCB TEST-NORMAL switch to NORMAL.

au. Refasten A3 PCB to chassis and position 560A upright.

av. Adjust OFFSET control until trace is positioned to center graticule line.

aw. Adjust CRT mainframe HORIZ POSITION to position left end of trace on left graticule edge.

ax. Adjust CRT mainframe X-Gain potentiometer to position right end of trace on right graticule edge. The HORIZ POSITION control and X-Gain potentiometer are interactive; repeat steps aw and ax until trace is positioned as shown below.



5-3.9 Refresh Digital-to-Analog Converter Calibration and Dot Connector Adjustments

This paragraph provides instructions for calibrating the refresh memory's offset and gain potentiometers, A2R43 and A2R40 respectively, and adjusting the dot connector potentiometers A2R46 and A2R50. To perform these adjustments, proceed as follows.

a. Perform voltage checks per paragraph 5-3.1.

b. Perform horizontal clamp and CRT mainframe horizontal deflection adjustments per paragraph 5-3.2.

c. Perform refresh horizontal gain adjustments per paragraph 5-3.3.

d. Perform Channel A and Channel B OFFSET ZERO adjustments per paragraph 5-3.4.

e. Perform CRT mainframe vertical calibration per paragraph 5-3.5.

f. Perform storage memory digital-to-analog converter calibration per paragraph 5-3.6.

g. Perform vertical analog-to-digital converter calibration per paragraph 5-3.7.

h. Perform Channel A and Channel B memory and subtract balance adjustments per paragraph 5-3.8.

i. Position 560A controls as follows (controls not indicated may be in any position; those in bold type are changes from the previous step):

CHANNEL A ON: On
INPUT: R
MEMORY: Off
dB PER DIVISION: 5
REFERENCE dB/dBm: dBm
OFFSET: −30.0
OFFSET ZERO: Not depressed
CHANNEL B ON: Off
MEMORY: Off
MARKER THRESHOLD: Off
REAL TIME: On
SMOOTHING: Off
A3 PCB TEST-NORMAL: TEST

j. Depress INPUT A pushbutton lightly so that all three Channel A INPUT switches are released.

k. Depress and hold REF POS LOCATE.

m. Observe CRT and adjust SET screwdriver potentiometer to position trace on next-to-bottom graticule line.

n. Release REF POS LOCATE.

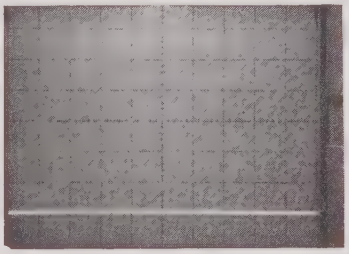
o. Observe CRT and adjust OFFSET control to position trace on next-to-top graticule line.

p. Depress OFFSET ZERO and insure that trace deflects to next-to-bottom graticule line. Depress (release) OFFSET ZERO. If trace is not coincident with the REF POS LOCATE reference trace (next-to-bottom graticule line), refer to paragraph 5-3.4 and repeat the OFFSET ZERO adjustments.

q. Depress REFRESH; insure REFRESH HOLD is not depressed.

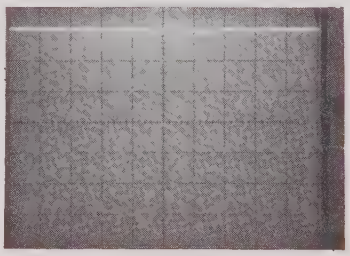
r. Depress OFFSET ZERO.

s. Observe CRT and adjust potentiometer A2R43 (see Figure 5-14 for location) to position trace on next-to-bottom graticule line. See waveform below.



t. Depress (release) OFFSET ZERO.

u. Observe CRT and adjust potentiometer A2R40 to position trace on next-to-top graticule line. See waveform below.



v. Depress REAL TIME.

w. Depress and hold REF POS LOCATE.

x. Observe CRT and adjust SET potentiometer to position trace to next-to-top graticule line.

y. Release REF POS LOCATE.

z. Observe CRT and adjust OFFSET control to position trace on next-to-bottom graticule line (≅ -30.0).

aa. Depress OFFSET ZERO and insure that trace deflects to next-to-top graticule line. Depress (release) OFFSET ZERO.

ab. Depress REFRESH.

ac. Depress OFFSET ZERO and insure that trace deflects to next-to-top graticule line ±1 minor division. If trace deflection is not as described, A2 PCB is faulty.

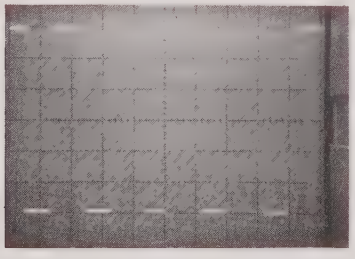
ad. Depress REAL TIME.

ae. Set controls for a 10 s sweep.

af. Observe CRT and when intensified dot reaches the right side of the screen, depress REFRESH.

ag. Depress OFFSET ZERO; when refresh sweep starts, alternately release and depress OFFSET ZERO to obtain approximately 10 to 12 rectangular pulses on the CRT. At the conclusion of the refresh sweep, immediately depress REFRESH HOLD to save the display.

ah. Adjust A2R46 to obtain optimum pulse response--no overshoot or ringing; see waveform below.



ai. Depress X-Y PLOT and adjust A2R50 to obtain optimum pulse response--no overshoot or ringing.

aj. Depress (release) REFRESH HOLD.

ak. Set controls for 100 ms sweep.

am. Depress REAL TIME.

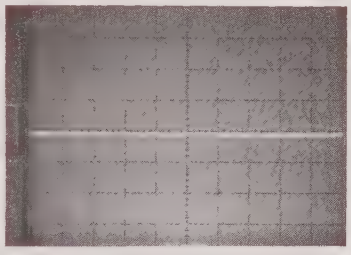
an. Position A3 PCB TEST-NORMAL switch to NORMAL.

ao. Refasten A3 PCB to chassis and position 560A upright.

ap. Adjust OFFSET control until trace is positioned to center graticule line.

aq. Adjust CRT mainframe X-position potentiometer (see Figure 5-12 for location) to position left end of trace on left graticule edge.

ar. Adjust CRT mainframe X-Gain potentiometer to position right end of trace on right graticule edge. The HORIZ POSITION control and the X-Gain potentiometer are interactive; repeat steps aq and ar until trace is positioned as shown below.



5-4 LOG AMPLIFIER (A3) PCB ADJUSTMENTS

The adjustments required to calibrate the log amplifier PCB circuits are described in the following paragraphs. These adjustments should only be performed by qualified personnel, and only when the performance verification tests of Section IV indicate an out-of-tolerance condition exists. The log amplifier accuracy adjustments in paragraph 5-4.3 are particularly critical and should not be attempted unless it is reasonably certain that log amplifier accuracy specifications are not being met (refer to paragraph 4-4.1 and Table 4-3). If the performance tests in Section IV indicate that the log amplifier is within the range of tolerances specified in Table 1-1, do not adjust log amplifier potentiometers.

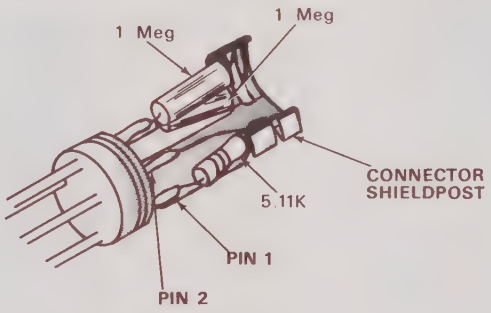
5-4.1 Channels A, B, A&B, and R Power Supply, Offset, Reference, and Thermistor Voltage Checks and Adjustments

This paragraph provides instructions for checking and/or adjusting the Channel A,

B, A&B, and R power supply, offset, reference, and thermistor voltages. To check and adjust these voltages does not require that a sweep generator be connected to the 560A. However, the sweep generator may be left connected if desired; it will not affect voltage readings. To check and adjust the offset, reference, and thermistor voltages requires the use of a simulated detector. This simulated detector contains precision resistors for simulating the detector diode, offset potentiometer, and thermistor resistances. Figure 5-5 shows this simulated detector and provides both fabrication instructions and a parts list. To perform the checks and adjustments in this paragraph, gain access to the A3 PCB (paragraph 5-2) and proceed as follows:

a. Depress 560A POWER to ON. Other controls may be in any position.

b. Perform Channel A, Channel B, Channel A&B, and Channel R power supply checks as follows:



Fabricate simulated detector as follows:

1. Solder one end of 5.11 kΩ resistor to pin 1. Solder the other resistor lead to the connector shieldpost and to pin 2.

2. Solder 1 MΩ resistor to pin 3. Solder the other resistor lead to shieldpost.

3. Solder 1 MΩ resistor to pin 4. Solder the other resistor lead to shieldpost.

Simulated Detector Parts List

Part Description	Part Number	Vendor
Connector, Plug	09CL4M	Switchcraft, Inc.
Resistor, Metal Film, 5.11 kΩ, 1/8W, 1% (1 each)	EMF55T1-5.11k-1%	Dale Elect.
Resistor, Metal Film, 1 MΩ, 1/8W, 0.1% (2 each)	EMF55T9-1 Meg-0.1% RNC55J1DO4BS	Dale Elect. Mil. Spec.

Figure 5-5. Simulated Detector Fabrication Instructions and Parts List

1. Connect DVM test leads between TP19 and TP20 (see Figure 5-10 for location). Meter should indicate 30.0 ±1.2Vdc.

2. Connect DVM test leads between TP21 and TP22. Meter should indicate 30.0 ±1.2Vdc.

3. Connect DVM test leads between TP1 and TP4 (common). Meter should indicate +15.0 ±0.6Vdc.

4. Connect DVM test leads between TP2 and TP4 (common). Meter should indicate -15.0 ±0.6Vdc.

5. Connect DVM test leads between TP9 and TP12 (common). Meter should indicate +15.0 ±0.6Vdc.

6. Connect DVM test leads between TP10 and TP12 (common). Meter should indicate -15.0 ±0.6Vdc.

c. Connect simulated detector to front panel A connector.

d. Depress CHANNEL A ON pushbutton (turn Channel A on). Insure that CHANNEL B ON pushbutton is not depressed (Channel B off).

e. Perform Channel A&B zero tracking, and Channel A offset and thermistor checks and/or adjustments as follows:

1. Connect DVM test leads between TP3 and TP4 (common). Adjust potentiometer A3R68 for 0 volts ±50μV.

2. Connect DVM test leads between TP16 and TP4 (common). Adjust potentiometer A3R18 for 0 volts ±20mV.

3. Connect DVM test leads between TP15 and TP4 (common). Meter should indicate 0 ±0.1 volts.

f. Connect simulated detector to front panel B connector.

g. Depress CHANNEL A ON and CHANNEL B ON pushbuttons. (Turn Channel A off and Channel B on.)

h. Perform Channel B offset, thermistor, and reference voltage checks and adjustments as follows:

1. Connect DVM test leads between TP16 and TP4 (common). Adjust potentiometer A3R27 for 0 volts ±20mV.

2. Connect DVM test leads between TP15 and TP4 (common). Meter should indicate 0 ±0.1Vdc.

3. Connect DVM test leads between TP5 and TP6. Adjust potentiometer A3R182 for 8.25 volts ±3.0mV.

i. Connect simulated detector to front panel R connector.

j. Perform Channel R zero tracking, offset, thermistor, LOG 1 R, LOG 2 R, and reference voltage checks and/or adjustments as follows:

1. Connect DVM test leads between TP11 and TP12 (common). Adjust potentiometer A3R209 for 0 volts ±50μV.

2. Connect DVM test leads between TP18 and TP12 (common). Adjust potentiometer A3R255 for 0 volts ±20mV.

3. Connect DVM test leads between TP17 and TP12 (common). Meter should indicate 0 ±0.1V.

4. Connect DVM test leads between TP7 and TP12 (common). Adjust potentiometer A3R190 for 0 volts ±100μV.

5. Connect DVM test leads between TP8 and TP12 (common). Adjust potentiometer A3R194 for 0 volts ±3.0mV.

6. Connect DVM test leads between TP13 and TP14. Adjust potentiometer A3R284 for 8.25 volts ±3.0mV.

5-4.2 Channels A&B Detector Balance Adjustment

This paragraph provides instructions for adjusting Detector A Balance and Detector B Balance potentiometers R315 and R312 respectively. For these adjustments, the 560A must be interconnected with the sweeper as shown in Figure 5-4. To perform these adjustments, proceed as follows:

a. Perform the voltage checks and adjustments in paragraph 3-4.1.

b. Reinstall bottom cover and place 560A in upright position (normal operating configuration). Allow 30 minutes for temperature stabilization.

NOTE

To allow for normal airflow across the affected components, the 560A must be upright with all covers in place.

c. Position 560A controls as follows:

CHANNEL A ON: On
INPUT: A
MEMORY: Off
dB PER DIVISION: 10
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
CHANNEL B ON: Off
INPUT: B
MEMORY: Off
dB PER DIVISION: 10
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
MARKER THRESHOLD: Off
REFRESH: On
REFRESH HOLD: Off
SMOOTHING: OFF
POWER: On

d. Disconnect simulated detector from front panel R connector; leave front panel connectors A and B disconnected.

e. Position CHA A and CH B LOW LEVEL TRIM potentiometers (right side panel) to midrange.

f. Turn 560A upside down and slide bottom cover back.

g. Adjust OFFSET Channel A control to place the trace in the center of the display (≃-35 dBm).

h. Adjust R315 for waveform similar to the one shown below.

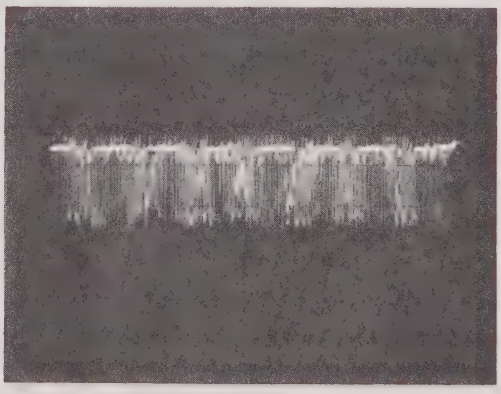
i. Depress CHANNEL A ON (release) and depress CHANNEL B ON.

j. Adjust OFFSET Channel B control to place the trace in the center of the display (≃-35 dBm).

k. Adjust R312 for waveform similar to the one shown below.

NOTE

Perform these adjustments as rapidly as possible, while the 560A's internal temperature is still stable.



5-4.3 Channels A & B and R Log Amplifier Accuracy Adjustments

This paragraph provides instructions for checking and adjusting the Channel A&B and Channel R log amplifier accuracy. There are two accuracy adjustments for each log amplifier channel (A&B and R); one adjusts the log amplifier channel to provide 125mV per dBm of input signal, and the other adjusts the log amplifier output so that 0 volts equals 0 dBm. Both of these adjustments are critical and should not be adjusted unless it is reasonably certain, based on the criteria in paragraph 4-4, that the log amplifier accuracy specifications are not being met. As explained in the NOTE preceding step j in paragraph 4-3, log amplifier accuracy testing is divided into two tests--one test for +10 to -55 dBm and a second test, if necessary, for +16 dBm. Figure 5-6 shows the test setup and provides initial sweep generator control positioning for the +10 to -55 dBm test.

To perform log amplifier accuracy test and adjustments, gain access to the A3 PCB (paragraph 5-2); then proceed as follows:

a. Calibrate the power meter and power sensor as follows:

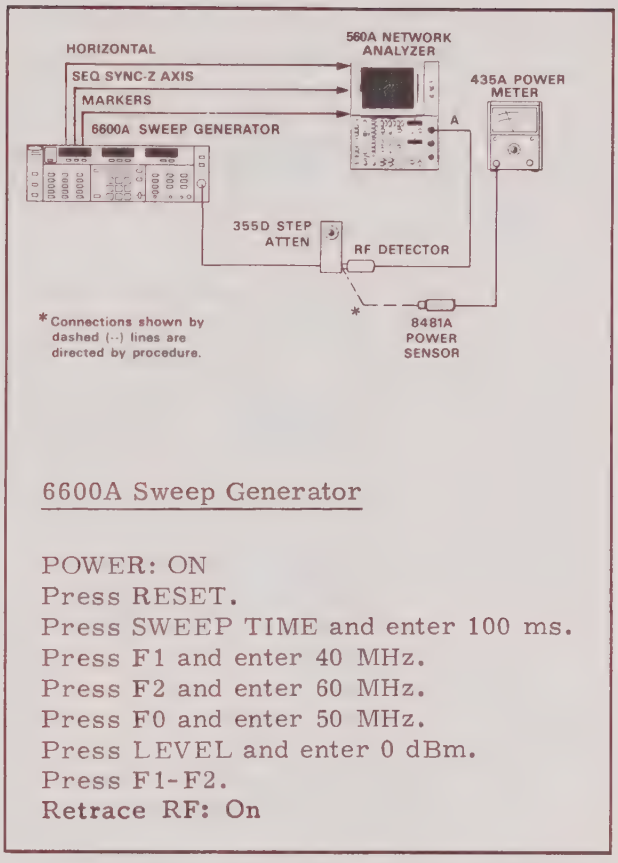
   1. Position CAL FACTOR control on power meter to specified calibrate factor, as indicated by chart on power sensor.

   2. Position Range control on power meter to 1mW.

   3. Connect power sensor to POWER REF connector; adjust CAL ADJ screwdriver potentiometer to position meter pointer on CAL mark.

   4. Disconnect power sensor from POWER REF connector.

b. Calibrate the sweep generator/step attenuator power output for +5 dBm and then +10 dBm.



6600A Sweep Generator

POWER: ON
Press RESET.
Press SWEEP TIME and enter 100 ms.
Press F1 and enter 40 MHz.
Press F2 and enter 60 MHz.
Press F0 and enter 50 MHz.
Press LEVEL and enter 0 dBm.
Press F1-F2.
Retrace RF: On

Figure 5-6. Test Setup for Power Accuracy Tests

Proceed as follows.

1. Setup the test equipment as shown in Figure 5-6, and connect the 8481A Power Sensor to the output of the step attenuator.

2. On the 6647A:

   (a) Press CW F0.
   (b) Press LEVEL and set for +5 dBm.

3. On the 355D, position the attenuator dial to 10.

4. On the 6647A, press LEVEL and operate the INCREASE-DECREASE lever to obtain a

-5 dBm reading on the power meter.

5. Record the 6647A's indicated output power level from the LEVEL LED display.

6. On the 6647A:

   (a) Set the power level for a +10 dBm reading on the LEVEL LED display.

   (b) Operate the INCREASE-DECREASE lever to obtain a 0 dBm reading on the power meter.

   (c) Record the 6647's indicated output power level from the LEVEL LED display.

   (d) Press F1-F2.

7. Disconnect the power sensor from the step attenuator.

c. Position 560A controls as follows:

CHANNEL A ON: On
INPUT: A
MEMORY: Off
dB PER DIVISION: 1
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
CHANNEL B ON: Off
INPUT: B
MEMORY: Off
dB PER DIVISION: 1
REFERENCE dB/dBm: dBm
OFFSET ZERO: Not depressed
MARKER THRESHOLD: Off
REFRESH: On
REFRESH HOLD: Off
SMOOTHING: MAX
POWER: On

d. Perform Channel A low Level calibration. In this and all subsequent steps, the directions to rotate controls clockwise and counterclockwise and to observe CRT trace for up or down movement assume that 560A is positioned upside down.

1. Connect RF detector to front panel A connector. (Leave detector unconnected from RF source.)

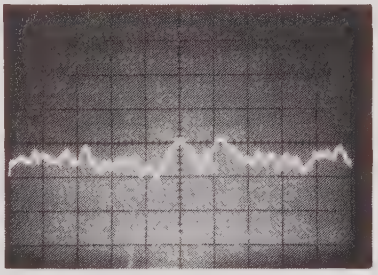
2. Depress and hold REF POS LOCATE and adjust SET potentiometer to position trace on center graticule line.

3. Release REF POS LOCATE.

4. Adjust OFFSET control for -58.0, as indicated on OFFSET dB display.

5. Adjust CH A LOW LEVEL TRIM control (right side panel) as follows:

   (a) If trace is above center graticule line, rotate potentiometer clockwise until trace is slightly below center graticule line and exhibits only random positive clipping. See waveform below.



   (b) If trace is either below center graticule line or off-screen, rotate potentiometer counterclockwise until trace is positioned as described in step (a), above.

e. Perform Channel A power accuracy test as follows:

1. Rotate OFFSET control clockwise to +10.0, as indicated on OFFSET dB display.

2. Connect RF detector to 355D output connector.

3. Depress .2 dB PER DIVISION pushbutton.

4. Construct a chart similar to that shown in Table 5-1.

5. Operate the chart of Table 5-1 as follows:

   (a) Position 355D to first Attenuator Dial Setting.

   (b) Adjust OFFSET control for first OFFSET dB Reading.

   (c) Read accuracy error at 50 MHz (center of trace) directly from CRT. If the trace is below the center graticule line, the accuracy error is + (positive); conversely, if the trace is above the center graticule line, the error is - (negative).

   (d) Record the accuracy error in the "Accuracy Error" column of the chart.

   (e) Repeat steps (a) through (d) for Attenuator Dial Settings of 10 through 50.

NOTE

The following steps recheck low level calibration. The LOW LEVEL TRIM potentiometers compensate for thermocouple junction voltage drops between the RF detector and the A3 PCB input circuits. With the bottom cover removed, thermocouple voltage drops between the A connector and the Channel A input circuit may have changed.

   (f) Rotate OFFSET counter-

Table 5-1. Channel A Power Accuracy Chart

Attenuator Dial Setting	OFFSET dB Reading	Accuracy Error	* Tolerance (dB)
0	+10.0		+0.6 -0.5
10	0.0		+0.6 -0.5
20	-10.0		+0.6 -0.5
30	-20.0		+0.7 -0.6
40	-30.0		±0.7
50	-40.0		±0.8
60	-50.0		±0.9
60	-55.0		+1.3 -1.2

*Tolerance arrived at through a statistical probability formula--refer to paragraph 4-4.1.

clockwise for -58.0, as indicated on the OFFSET dB display.

(g) Disconnect RF detector from 355D.

(h) Readjust CH A LOW LEVEL TRIM potentiometer if necessary so that trace is slightly below center graticule line and exhibits only random positive clipping.

(i) Rotate OFFSET control clockwise for -50.0, as indicated on OFFSET dB display.

(j) Reconnect RF detector to 355D.

(k) Position 355D attenuator dial to 60.

(m) Read and record accuracy error, as described in steps (c) and (d) above.

(n) On the 6647A, press LEVEL and set the output power for the value recorded in step b.5 above.

(o) Read and record accuracy error, as described in steps (c) and (d) above.

(p) On the 6647A, press LEVEL and set the output power for the value recorded in step b.6(c) above.

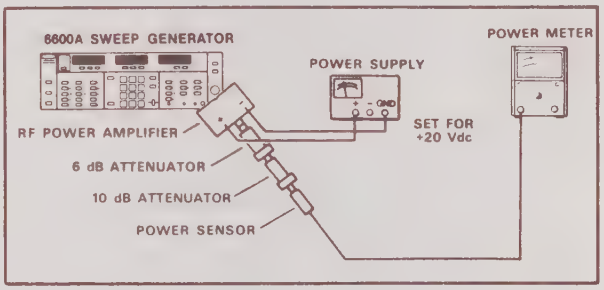
f. Perform Channel B low level calibration as follows:

1. Depress CHANNEL A ON and CHANNEL B ON pushbuttons (turn Channel A off and Channel B on).

2. Repeat subparagraphs d, steps 1 thru 5 for Channel B.

g. Perform Channel B power accuracy test by repeating for Channel B the instructions contained in subparagraph e, steps 1 thru 5.

h. Reconfigure and calibrate the test setup for the +16 dBm log amplifier accuracy test as shown below. If testing at +16 dBm is unnecessary (see NOTE preceeding step j, paragraph 4-3), skip this step and the one that follows; proceed to step j.



1. On 6647A:

a. Press FREQUENCY RANGE CW F0.

b. Press LEVEL.

c. Using the INCREASE-DECREASE lever, set output power for a 0 dBm reading on power meter.

2. Disconnect power sensor from 10 dB attenuator.

3. Remove both attenuators from test setup, and connect 560A RF detector to the power amplifier output.

4. On the 6647A, press FREQUENCY RANGE F1-F2.

i. Perform +16 dBm log amplifier accuracy test for Channel A, then Channel B, as follows:

1. Press CHANNEL A ON and CHANNEL B ON pushbuttons(turn Channel A on and Channel B off).

2. Move RF detector to front panel connector A.

3. Rotate OFFSET control counter-clockwise to +16.0, as indicated on OFFSET dB display.

4. Read and record the accuracy error at 50 MHz (center of trace) directly from CRT. If trace is below the center graticule line, accuracy error is + (positive); conversely, if the trace is above the center graticule line, the error is - (negative).

5. Depress CHANNEL A ON and CHANNEL B ON pushbuttons (turn Channel A off and Channel B on).

6. Move RF detector to front panel connector B.

7. Repeat step 4 above for Channel B.

j. If any of the Channel A or Channel B log amplifier accuracy readings are clearly out of tolerance (refer to paragraph 4-4), see below.

1. The accuracy error in both channels at each Attenuator Dial Setting (Power Accuracy Charts, subparagraph e4 and g4 above), and at ±16 dBm (subparagraph i above) should be within ±0.4 dBm of each other.

   (a) If the variation is greater than ±0.4 dBm, the out-of-tolerance condition is not caused by the common A&B log shaper circuit so the accuracy potentiometers (R154 and R181) will not correct the problem; the out-of-tolerance condition is caused by a defect or a maladjustment in the applicable channel's input circuit. (Applicable channel refers to the channel in which the out-of-tolerance condition occurs.) Repeat the adjustment instructions in paragraphs 5-4.1; if the out-of-tolerance condition still exists, troubleshoot the applicable channel's input circuit.

(b) If the variation is within ±0.4 dBm, but the reading(s) is out of tolerance, try a different RF detector and take the measurement again. If the reading(s) is still out of tolerance, proceed to step 2.

2. Construct a graph similar to that shown in Figure 5-7. When the accuracy error reading at each Attenuator Dial Setting (Table 5-1) and at +16 dBm is plotted onto the graph, the graph will show the overall shape of the log amplifier response curve. The two accuracy potentiometers, R181 and R154, do not adjust individual response points; they adjust the overall shape of the response curve. Potentiometer R181 (offset) moves the curve up or down and potentiometer R154 (gain) alters the response curve's slope.

3. Take the accuracy error data recorded in subparagraph e4, g4, or i and plot it onto the graph constructed in step 2 above.

4. Determine whether R181 or R154 needs to be adjusted. This determination is accomplished as follows:

   (a) If by moving the plot up or down all of the response points can be brought within the upper and lower error limits (Figure 5-7), adjust R181. Figure 5-8 describes the R181 adjustment.

   (b) If by changing the slope (gain) of the plot all of the response points can be brought within the upper and lower error limits, adjust R154. As a point of fact, however, it is very probable that if the response curve's slope is incorrect,

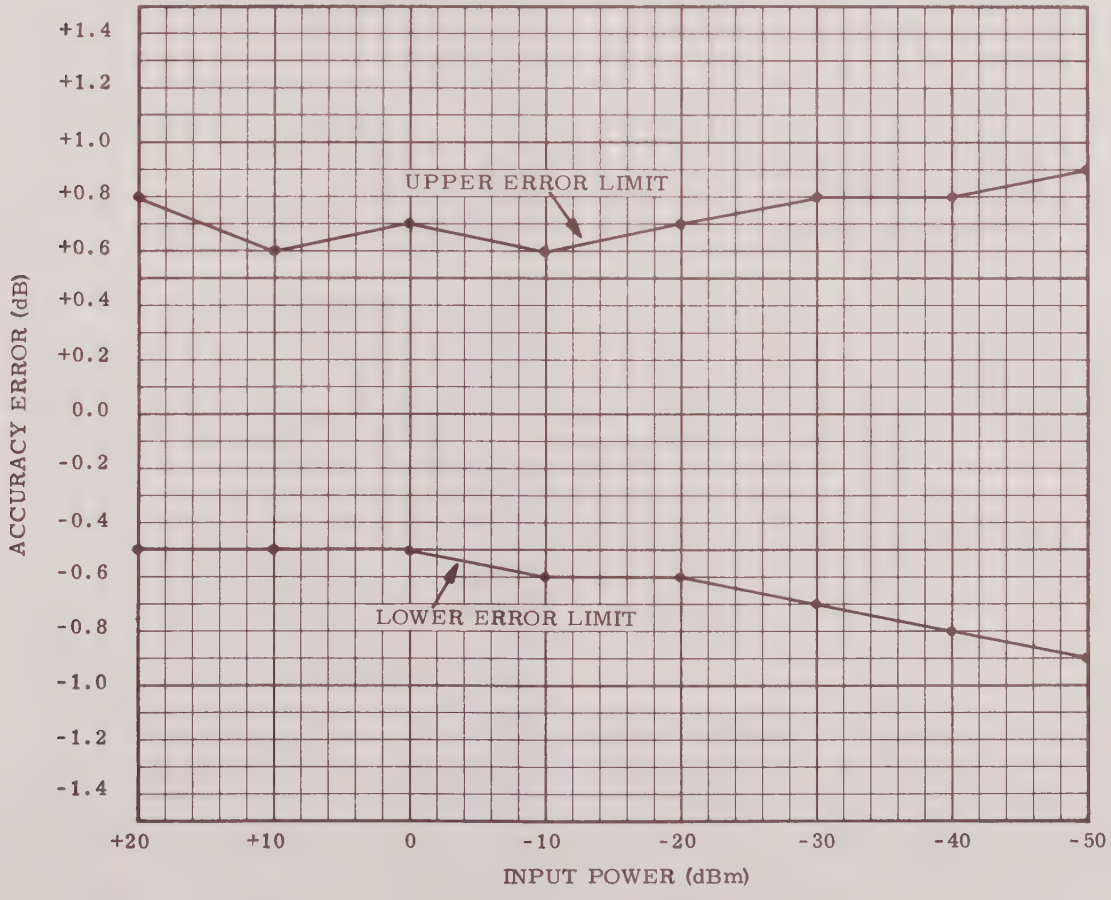


Figure 5-7. A&B Log Amplifier Response Graph

its offset will be incorrect also; consequently, both R181 and R154 will require adjustment. Figure 5-9 describes the adjustment of R181 and R154.

k. Perform Channel R Power Accuracy test as follows:

1. Disconnect RF detector from B and move to R front panel connector.

2. Depress Channel B INPUT R.

3. Adjust OFFSET control for +10.0, as indicated on OFFSET dB display.

4. Insure .2 dB PER DIVISION push-button is depressed.

5. Construct a chart similar to that shown in Table 5-2.

6. Operate the chart in Table 5-2 as follows:

(a) Position 355D to first Attenuator Dial Setting.

(b) Adjust OFFSET control for first OFFSET dB Reading.

(c) Read accuracy error at 50 MHz (center of trace) directly from CRT. If the trace is below the center graticule line, the accuracy error is + (positive); conversely, if the trace is above the center graticule line, the error is - (negative).

(d) Record the accuracy error in the "Accuracy Error" column of the chart.

(e) Repeat steps (a) thru (d) for remaining Attenuator Dial Settings.

m. If Channel R power accuracy readings are clearly out of tolerance (refer to paragraph 4-4), perform Channel R log accuracy adjustments in the same manner described for Channel A&B (refer to subparagraph j, above, and Figures 5-8 and 5-9). For the Channel R response curve, slope is adjusted using R230 and offset (up/down) is adjusted using R294.

5-5 GPIB INTERFACE (A6) PCB ADJUSTMENTS

The adjustments required to calibrate the GPIB interface PCB circuits are described

Table 5-2. Channel R Power Accuracy Chart

Attenuator Dial Setting	OFFSET dB Reading	Accuracy Error	* Tolerance (dB)
0	+10.0		+0.6 -0.5
10	- 0.0		+0.6 -0.5
20	- 10.0		+0.6 -0.5
30	-20.0		+0.7 -0.6
40	-30.0		±0.7

*Tolerance arrived at through a statistical probability formula - refer to paragraph 4-4.1.

Power Accuracy Chart

Attenuator Dial Setting	OFFSET dB Reading	Accuracy Error	* Tolerance (dB)
0	+10.0	+0.3	+0.6 -0.5
10	- 0.0	0	+0.6 -0.5
20	-10.0	+0.2	+0.6 -0.5
30	-20.0	0	+0.7 -0.6
40	-30.0	-0.4	±0.7
50	-40.0	-1.0	±0.8
60	-50.0	-0.8	±0.9

* Tolerance arrived at through statistical probability formula - refer to paragraph 4-4.1.

ADJUSTMENT PROCEDURE
Offset (R181) Potentiometer

1. Extract error data from power accuracy chart, above.
2. Plot error data on graph.
3. Connect error points together.
4. Study graph. As shown, if the error point at -40 dBm were moved upwards 0.2 dB, all error points would fall within the error range.
5. To make the adjustment, position 355D attenuator dial to 50; adjust OFFSET control for -40.8, as indicated on OFFSET dB display.
6. Adjust R181 counterclockwise to position trace on center graticule line.
7. Recheck power accuracy at all step attenuator dial settings.

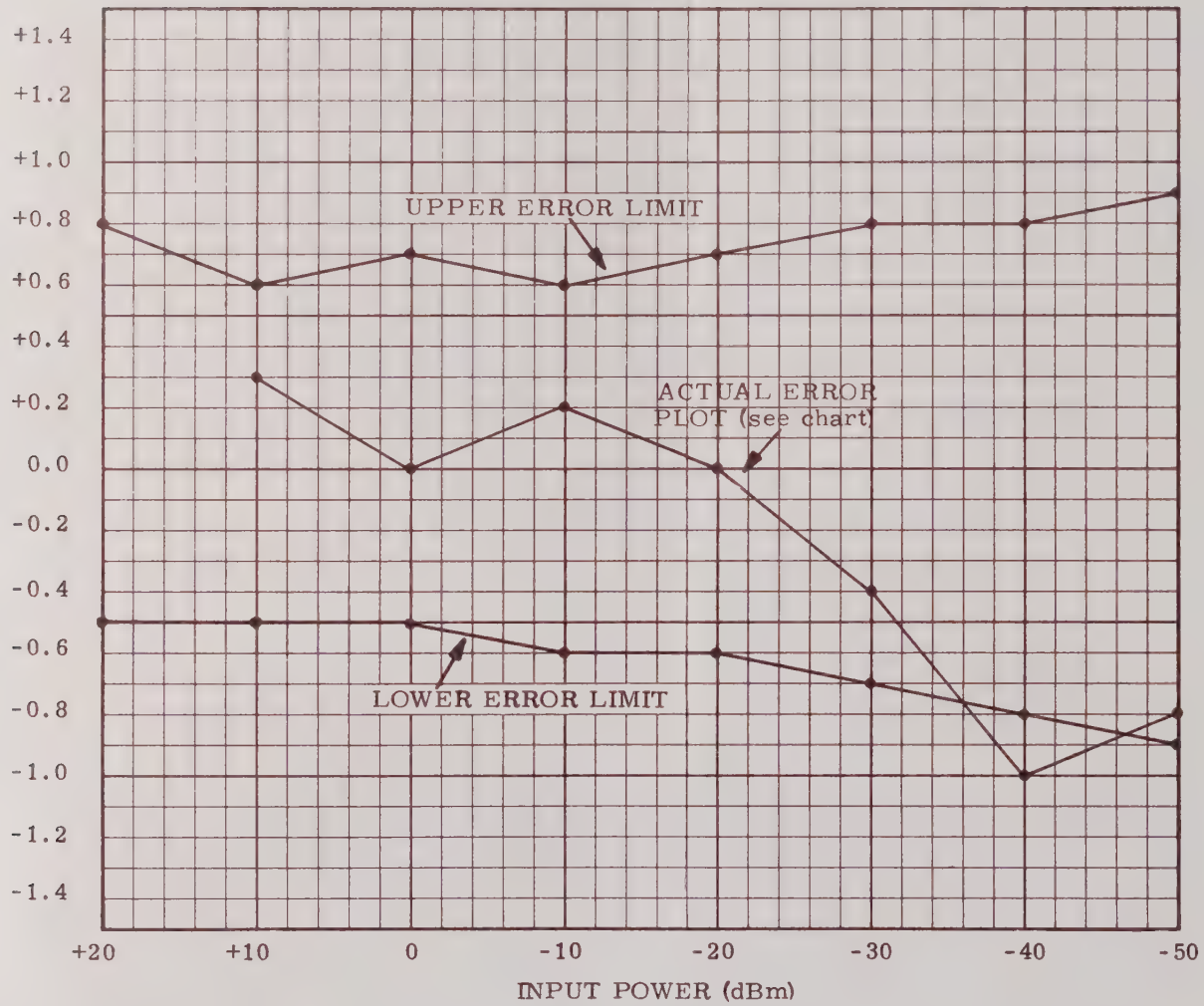


Figure 5-8. Example Describing How To Make R181 OFFSET ADJUSTMENT

Power Accuracy Chart

Attenuator Dial Setting	OFFSET dB Reading	Accuracy Error	*Tolerance (dB)
0	+10.0	+0.2	+0.6 -0.5
10	- 0.0	0.0	+0.7 -0.5
20	-10.0	0.0	±0.6
30	-20.0	-0.4	+0.7 -0.6
40	-30.0	-0.7	+0.8 -0.7
50	-40.0	-1.0	±0.8
60	-50.0	-1.3	±0.9

* Tolerance arrived at through a statistical probability formula - refer to paragraph 4-4.1.

ADJUSTMENT PROCEDURE
Gain (R154) and Offset (R181) Potentiometers

1. Extract error data from power accuracy chart, above.

2. Plot error data on graph.

3. Draw straight line between the error point at +10 dBm and the error point at -50 dBm.

4. Study graph. As shown, the response curve needs two corrections: slope and offset (up/down). R154 needs to correct slope approximately -1.0 dB; R181 needs to correct offset approximately +1.2 dB. Adjust offset first, then adjust slope.

5. To make the adjustments:
   a. Position 355D attenuator dial to 60; adjust OFFSET control for -50.0, as indicated on OFFSET dB display.
   b. Adjust R181 counterclockwise to position trace on center graticule line.
   c. Position 355D attenuator dial to 0; adjust OFFSET control for +10.0, as indicated on OFFSET dB display.
   d. Adjust R154 counterclockwise to position trace on center graticule line.

6. Recheck power accuracy at -50 dBm. If OFFSET dB reading is still out of tolerance, construct a new graph and repeat steps 5a thru d, above, until all power accuracy readings are within the error range.

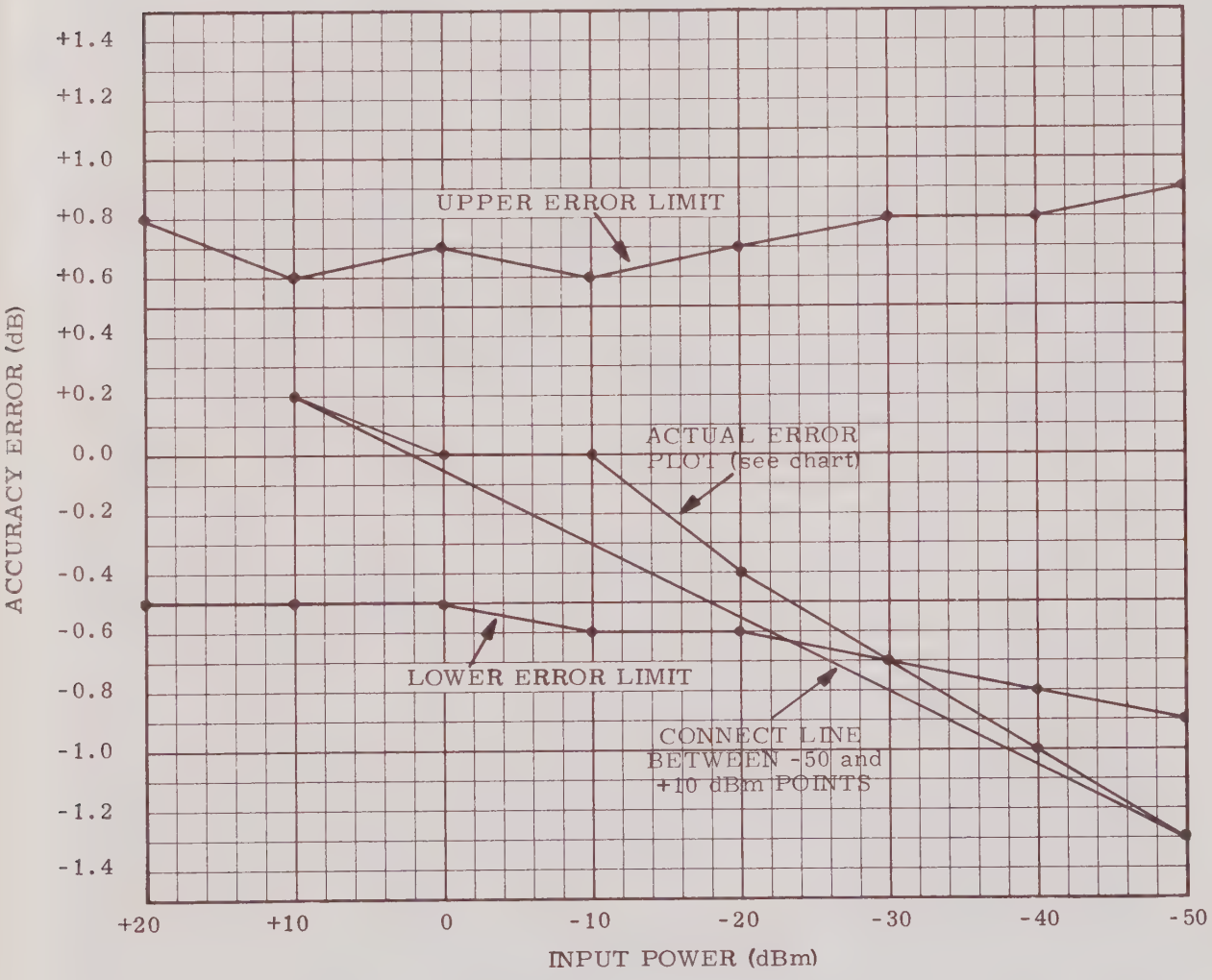


Figure 5-9. Example Describing How To Make R181/R154 OFFSET/SLOPE ADJUSTMENTS

below. These adjustments should be performed by qualified personnel, and only when the performance verification tests of Section IV indicate an out of tolerance condition exists. Calibration of the A6 PCB requires a sweep generator, a GPIB controller, and an oscilloscope. To calibrate the A6 PCB, proceed as follows:

a. Perform the GPIB checks in paragraph 4-3.3.

b. Gain access to the A6 PCB (paragraph 5-2).

CAUTION

Avoid contact with the ground tab on VR2. This tab is at a -18 Vdc potential. If the VR2 tab is shorted to ground, damage to A6 components will result.

c. Turn on 560A power and program controller to take data continuously from Channel A; see program below.

```
10 OUTPUT 706;"AI"
20 ENTER 706;X
30 DISP X
40 WAIT 50
50 GO TO 10
60 END
```

HP 85 Program

```
0: wrt 706,"AI"
1: red 706,X
2: dsp X
3: wait 50
4: gto 0
```

HP 9825A Program

d. Calibrate amplifier offset potentiometer A6R8 as follows:

1. Connect clip leads between test points A6TP12 and A6TP14 (Figure 5-11).

2. Connect oscilloscope to test point A6TP9.

3. Set vertical sensitivity to 10 mV/division; set horizontal time base to 10 ms/division.

4. Adjust A6R8 for lowest voltage point (maximum dip).

e. Calibrate A/D converter offset potentiometer A6R9 as follows:

1. Adjust A6R9 so that the controller display reads 00.01 dBm.

f. Calibrate +/- sign comparator reference potentiometer A6R29 as follows:

1. Connect oscilloscope to test points A6TP10.

2. Set vertical sensitivity to 2 volts/division.

3. Adjust A6R29 until a 0 to ≃+4V band of noise appears on the oscilloscope.

g. Calibrate amplifier gain potentiometer A6R41 as follows:

1. Disconnect clip leads from test points A6TP12 and A6TP14. Set sweep generator output to +10.0 dBm.

2. Estimate absolute power reading to the nearest .01 dBm as follows:

(a) Adjust Channel A OFFSET dB to place the trace on top of the center horizontal graticule line.

(b) Decrease OFFSET dB readout by .1 dB. For example, if the OFFSET dB readout was +10.0 dBm, decrease it to +9.9 dBm.

(c) Determine the distance from the trace to the center horizontal graticule line, to the nearest .01

of a division. Multiply the value by .2 dB/division to determine the value in dB's.

(d) If the trace is above the center graticule line, subtract the value determined in step (c) from the OFFSET dB readout in step (b). If the trace is below the center graticule line, add the value determined in step (c) to the OFFSET dB readout determined in step (b). For example, if the trace is .15 dB below the center graticule horizontal line and the OFFSET dB readout indicates +9.9 dBm, then add .15 dB and +9.9 dBm, for a final value of 10.05 dBm.

3. Set attenuator to 30 dB.

4. Adjust OFFSET dB control so trace is on top of the center horizontal graticule line (≈-30.0 dBm).

5. Estimate absolute power reading to the nearest .01 dBm, ±0.3 dB, using the method listed in step 2.

6. Adjust amplifier gain potentiometer A6R41 for a controller power reading that is the same as the absolute power determined in step 5.

7. Set attenuator to 10 dB.

8. Adjust OFFSET dB control so trace is on top of the center horizontal graticule line (≃+10.0 dBm).

9. Determine absolute power reading to the nearest .01 dB using the method listed in step 2.

10. Adjust A6R8 for a controller power reading that is the same as the absolute power reading determined in step 9.

h. Calibrate -30 dBm comparator reference potentiometer A6R37 as follows:

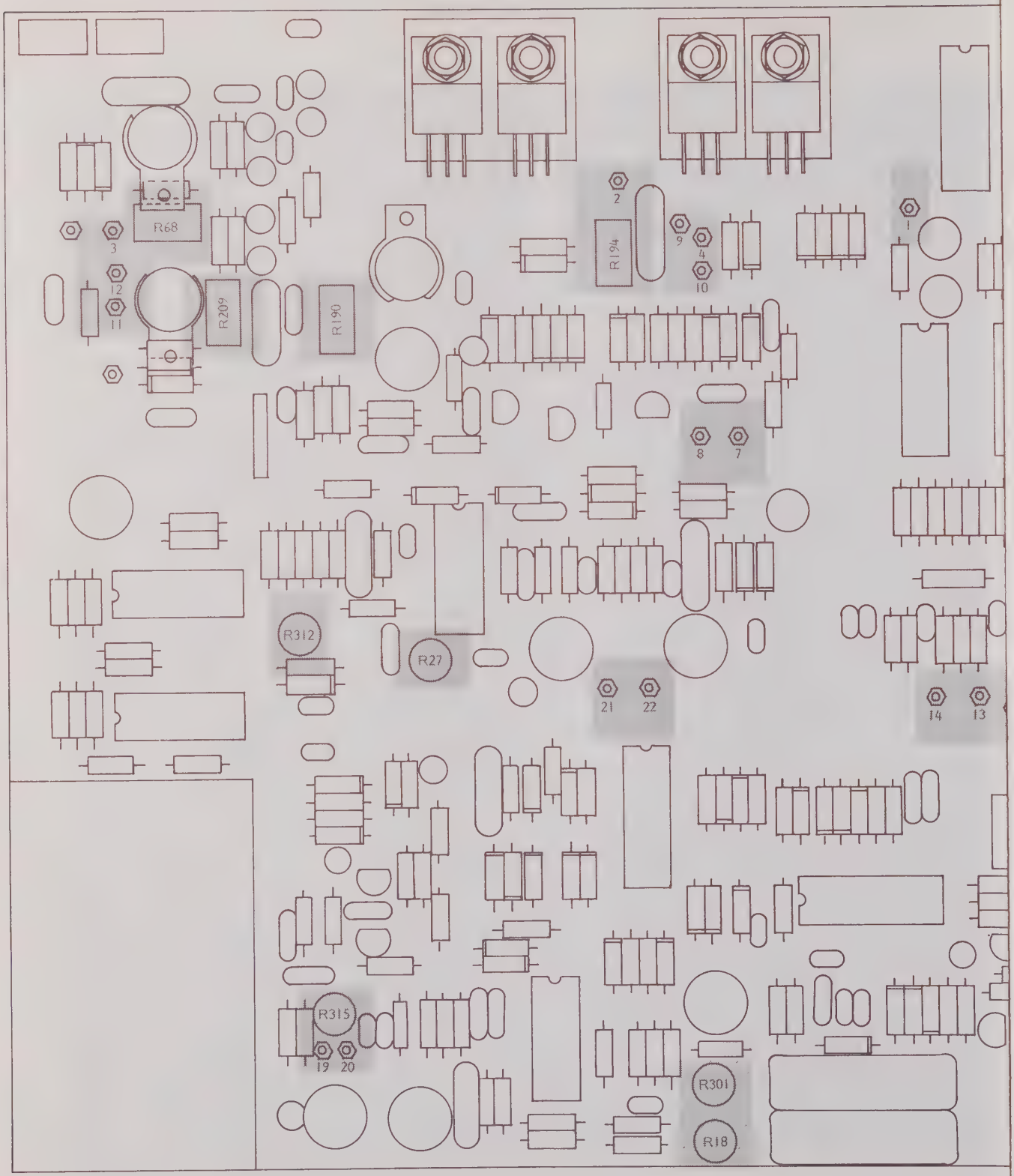
1. Adjust OFFSET dB control for a -30.0 dBm reading.

2. On sweep generator, manually adjust RF output so trace is on top of the 560A's center horizontal graticule line.

3. Connect oscilloscope to test point A6TP15.

4. Adjust A6R37 counterclockwise until the oscilloscope shows a waveform switching back and forth between ≃+5V and 0V.

5. Adjust A6R37 clockwise until the oscilloscope shows a waveform at ≃ +5V, with local calibrate pulses running across the screen.


R68
3
12
11
R209
R190
2
R194
9
4
10
1
8
7
R312
R27
21
22
14
13
R315
19
20
R301
R18

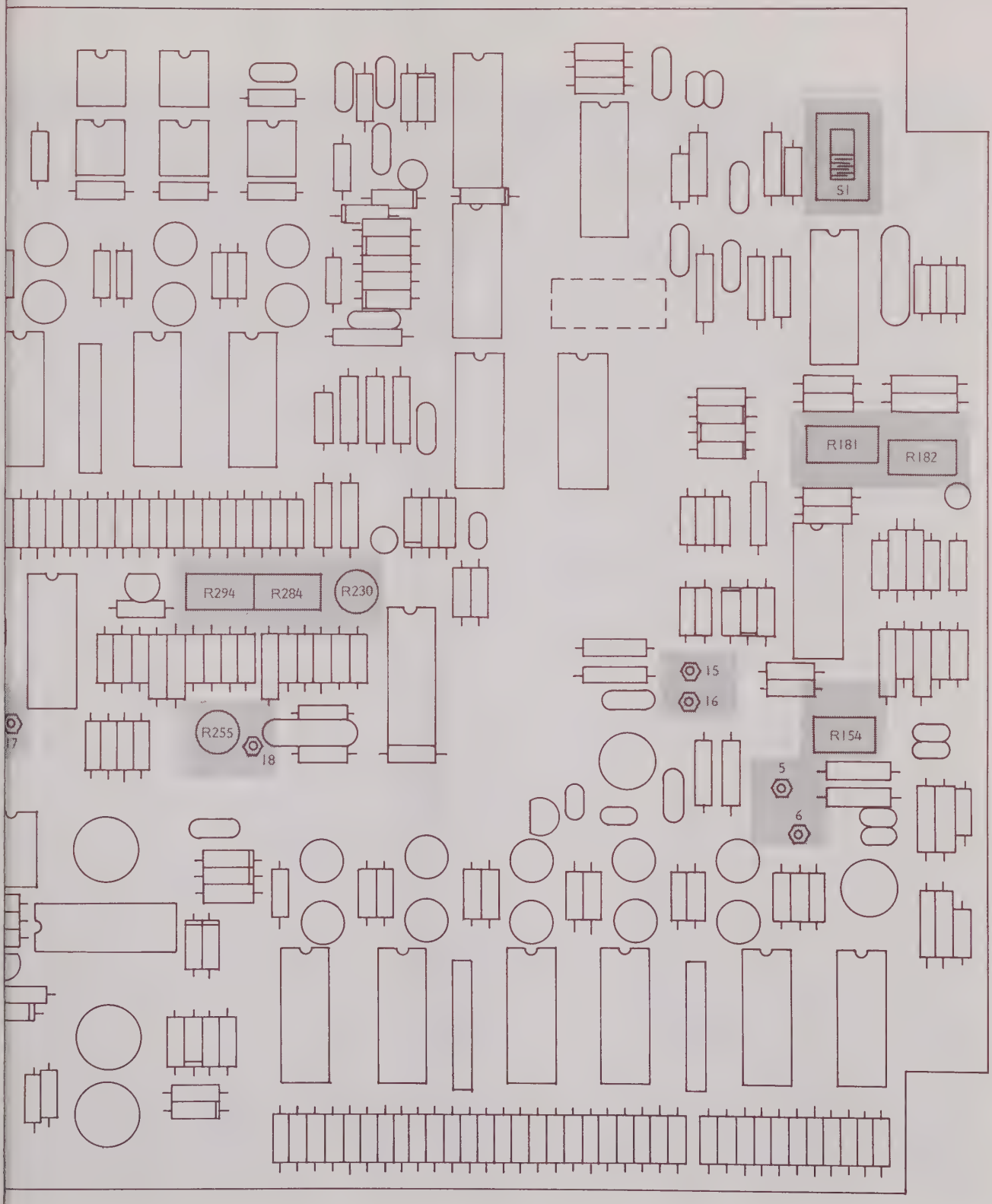


Figure 5-10. Locations of Test Points and Potentiometers, A3 PCB

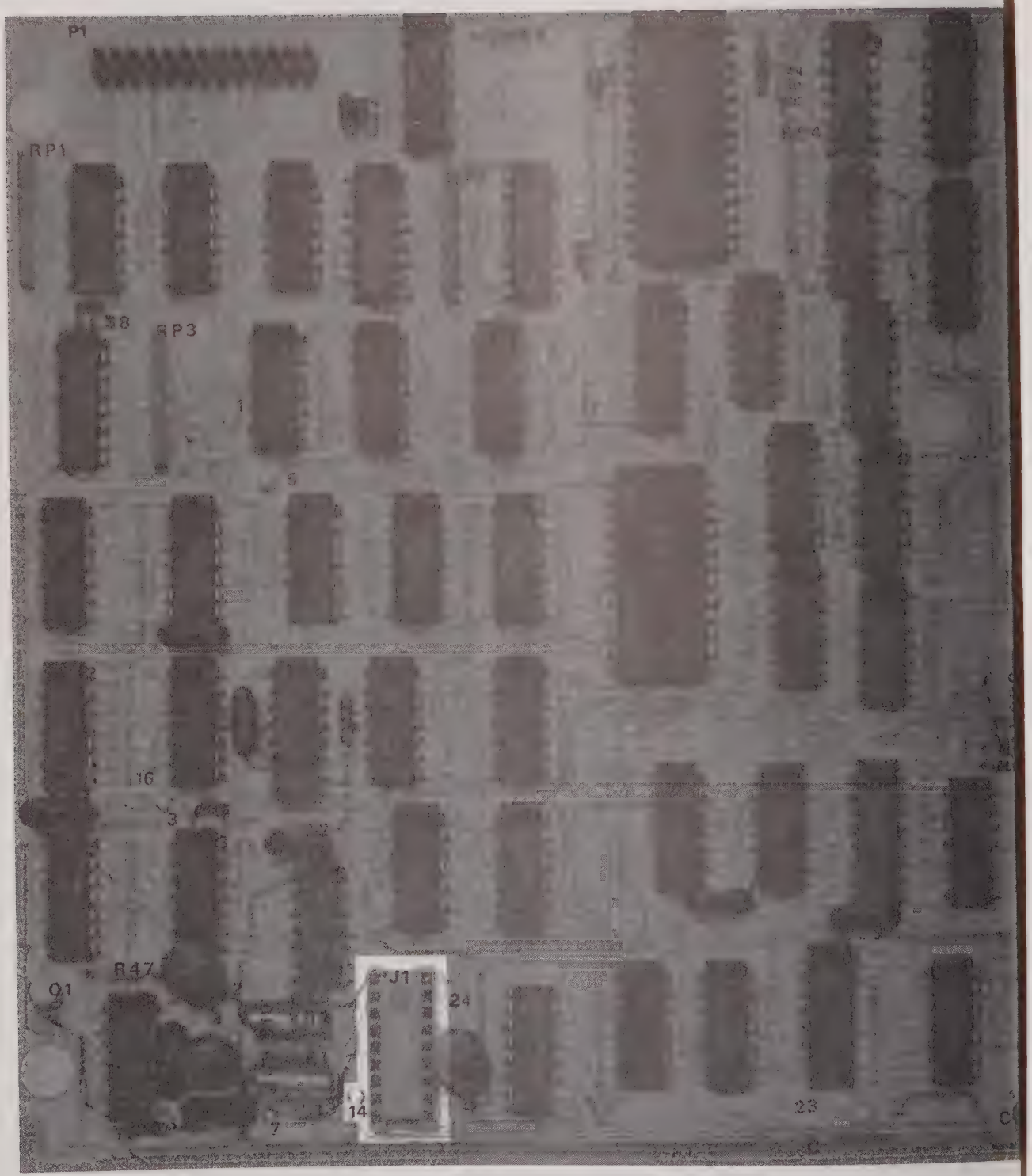
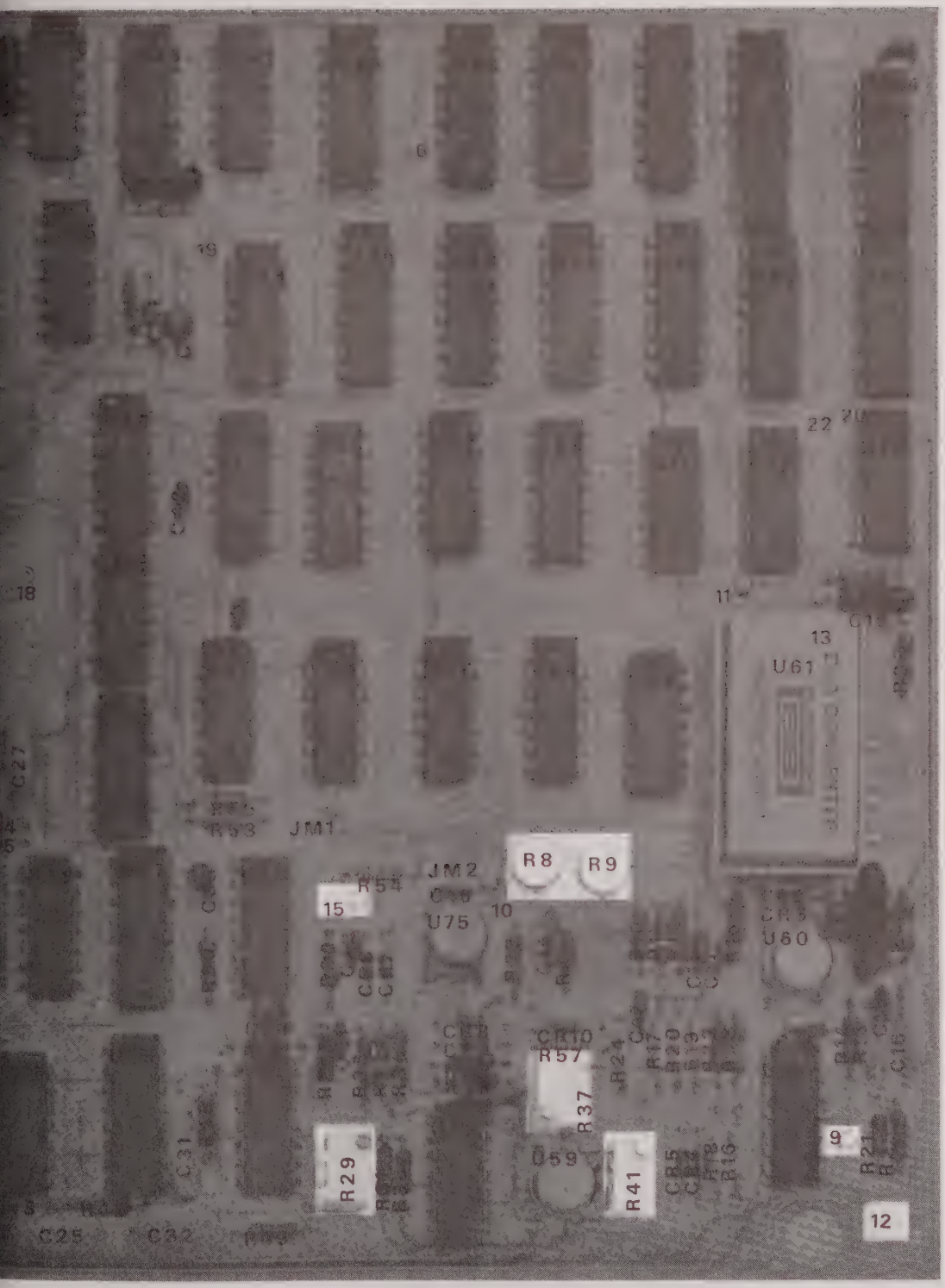


Figure 5-11. Locations of Test Points and Adjustments, A6 PCB


R8
R9
JM1
JM2
R54
U75
U61
U60
CR10
R57
R37
R29
R41
CR5
C25
C32
15
10
13
12

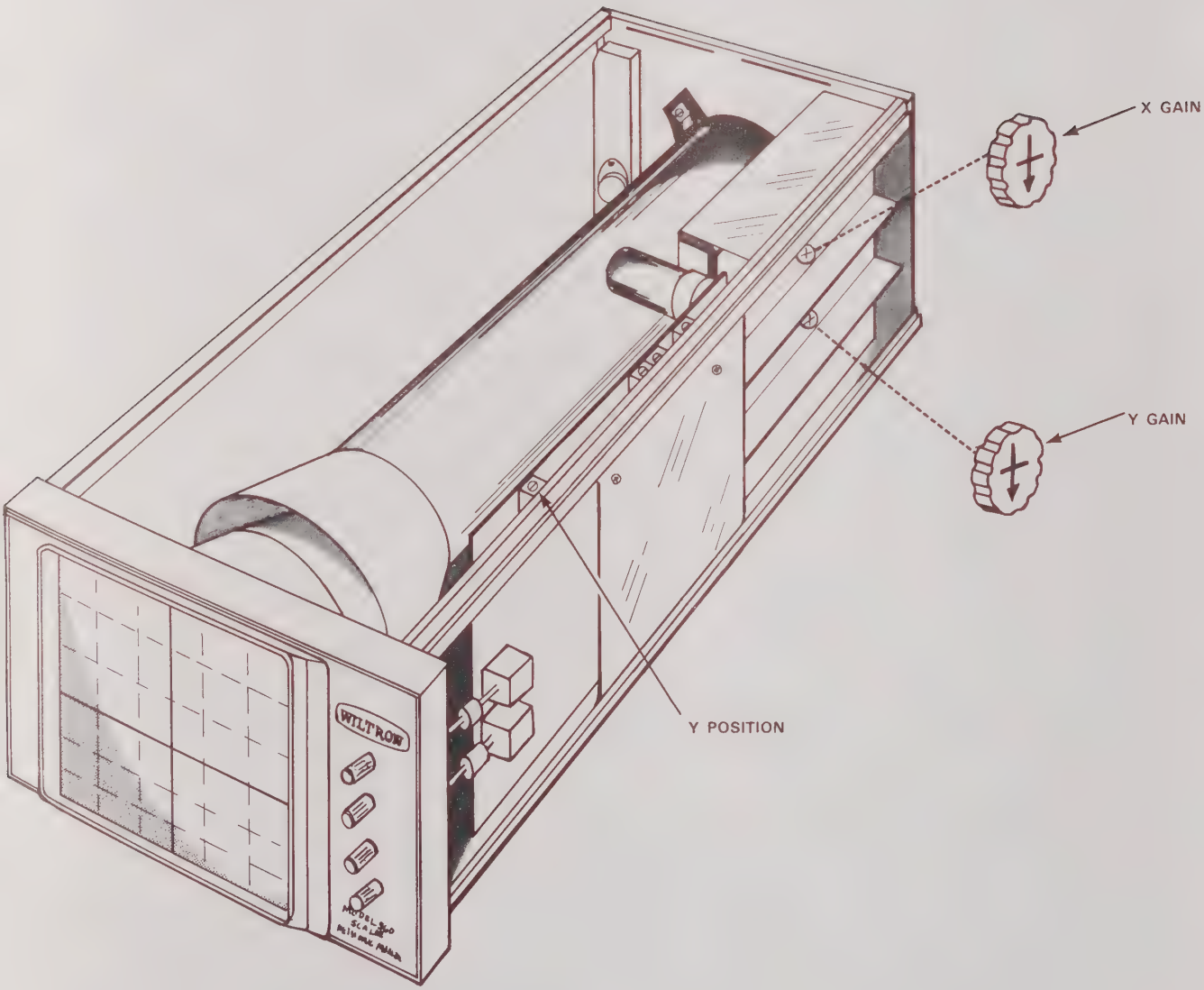


Figure 5-12. Locations of Test Points and Potentiometers, CRT Mainframe

Figure 5-11.

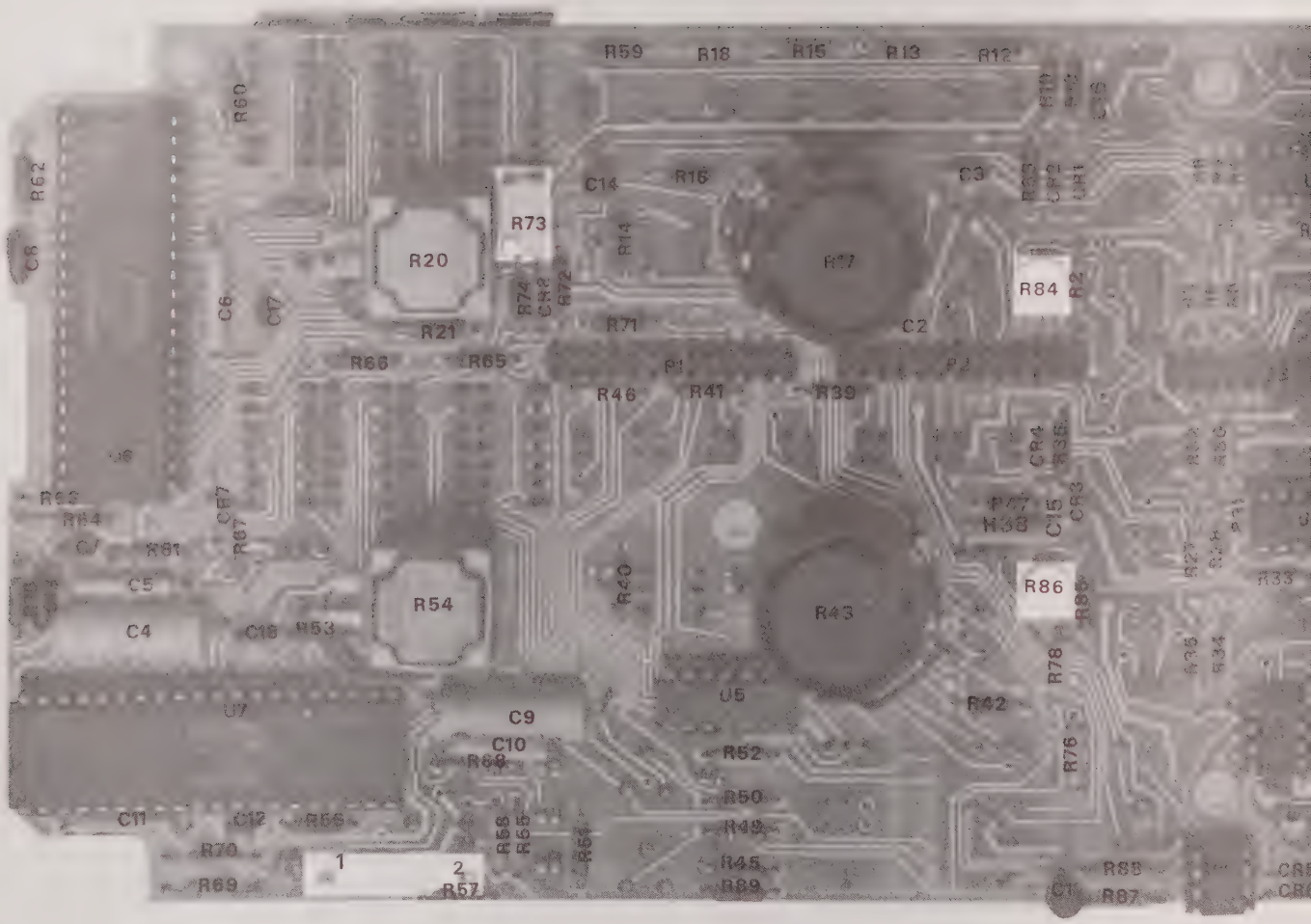
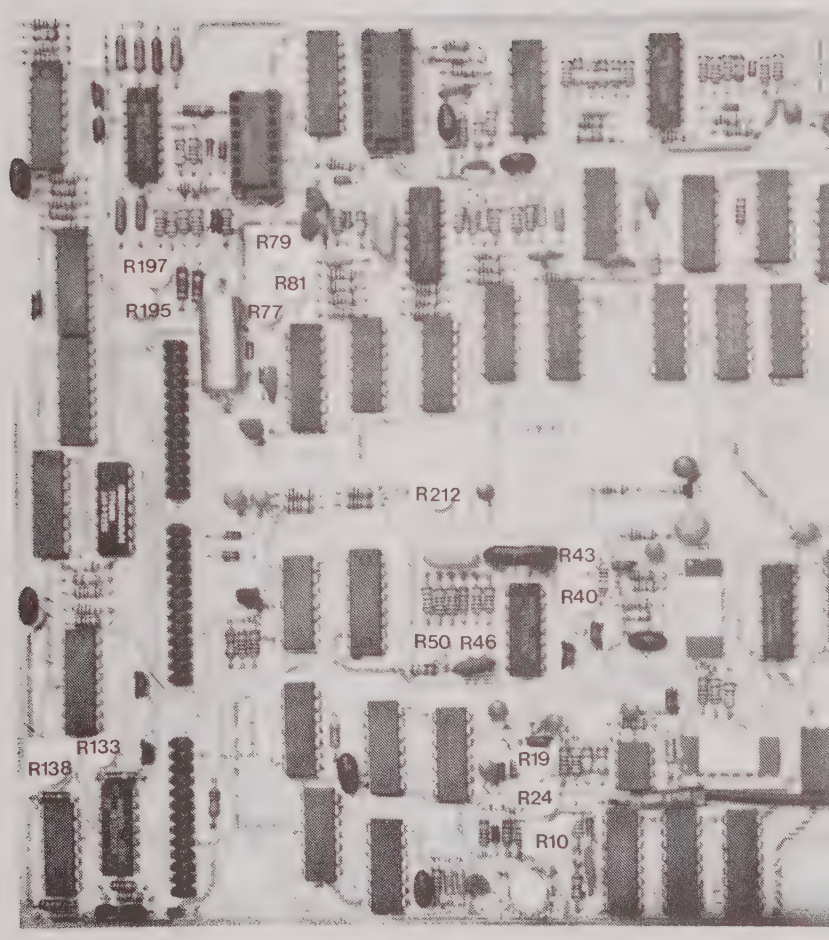


Figure 5-13. Locations of Test Points and Potentiometers, A1 PCB

R81
R77


R79
R197
R81
R195
R77
R212
R43
R40
R50
R46
R133
R138
R19
R24
R10

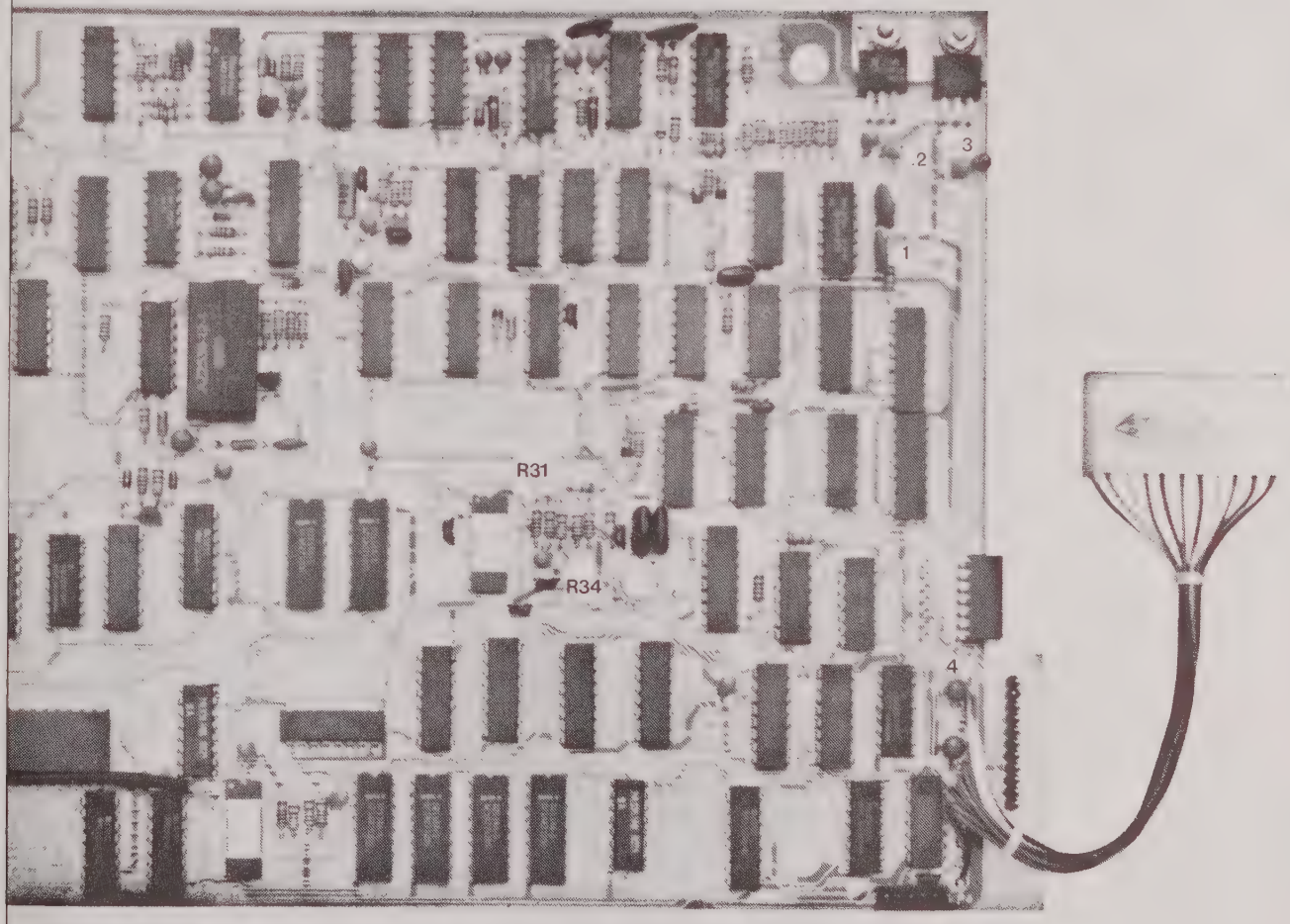
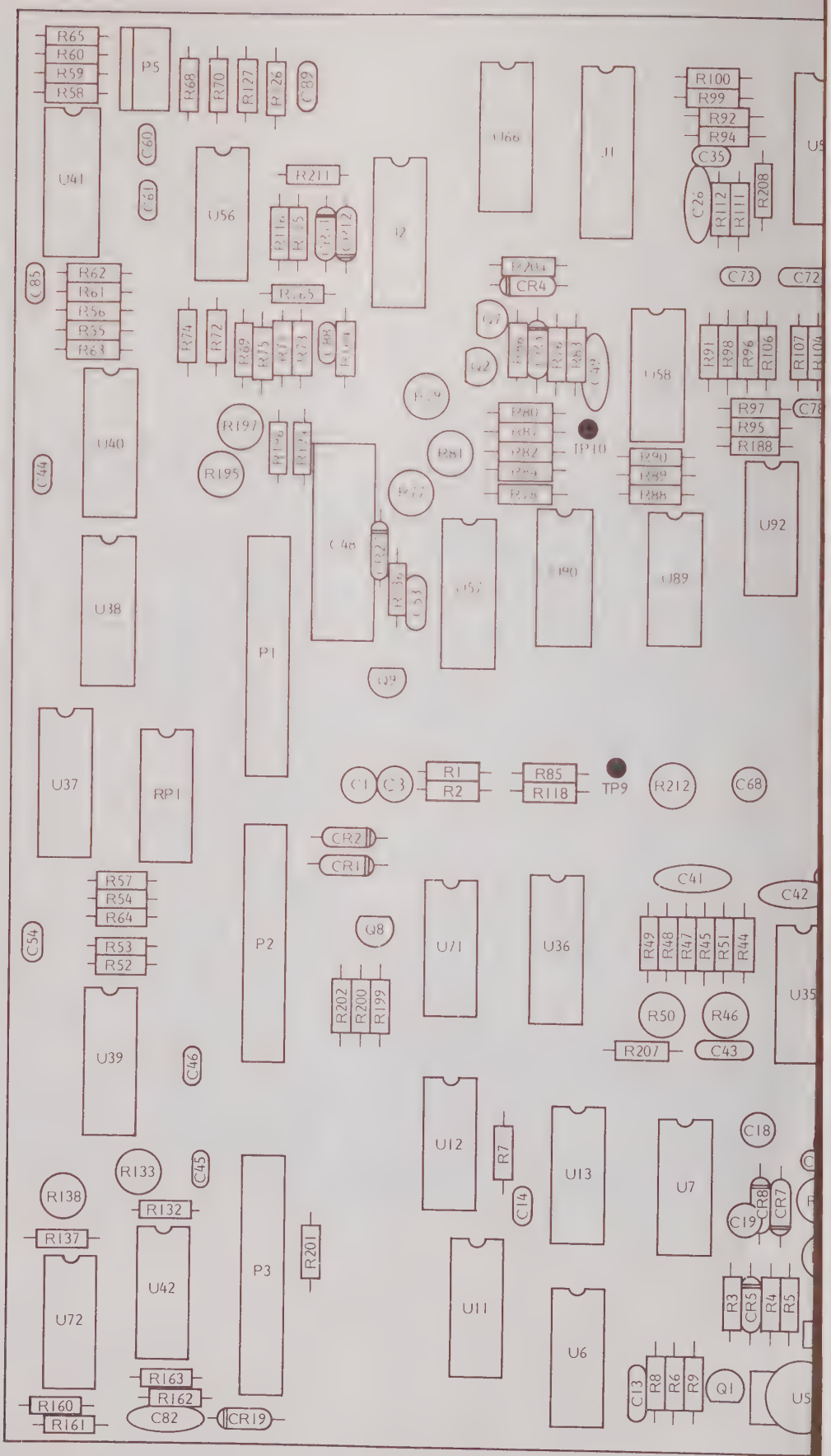
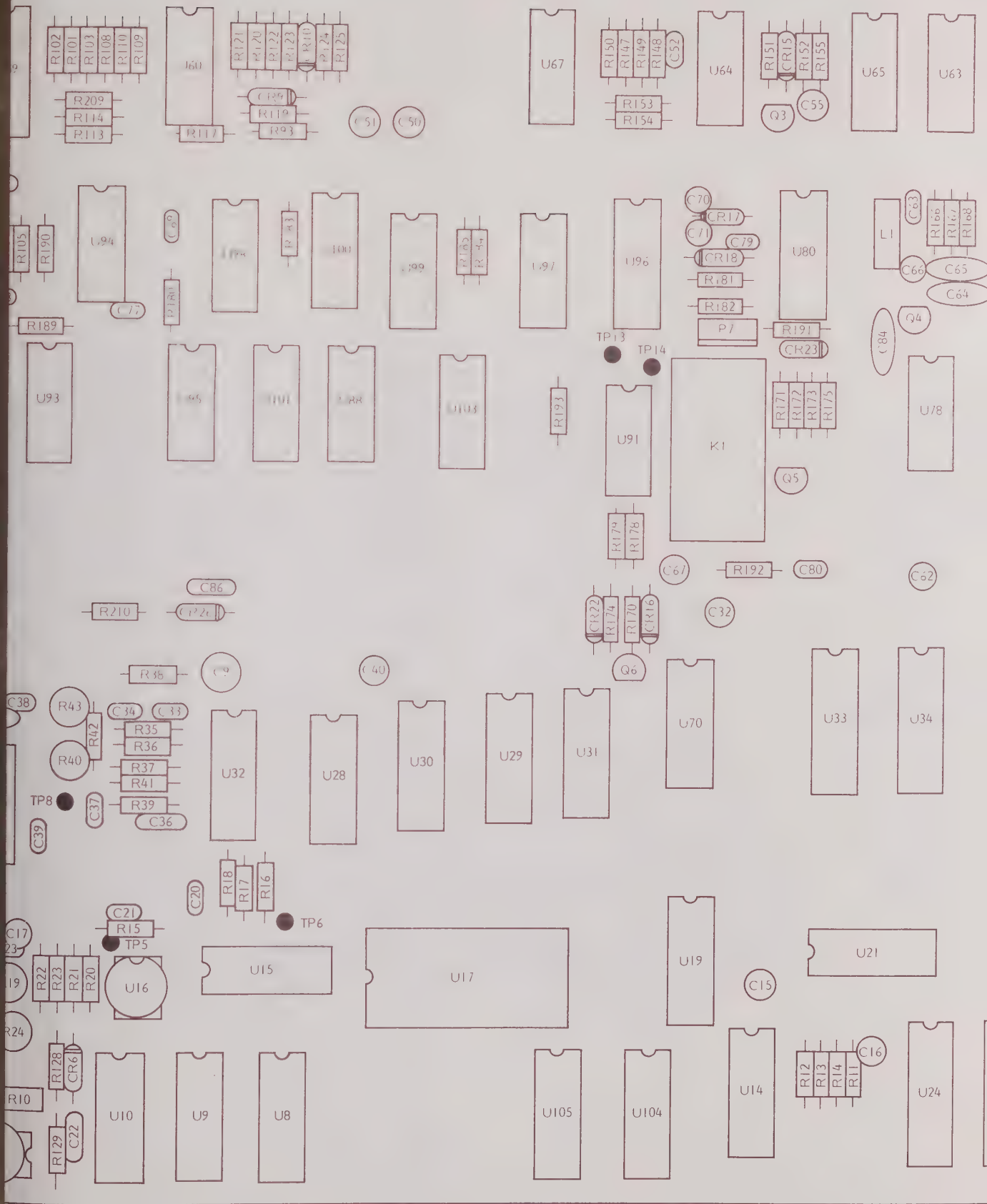


Figure 5-14. Locations of Test Points and Potentiometers, A2 PCB

Figure 5-13.


R65
R60
R59
R58
P5
R68
R70
R127
R26
C89
U41
C60
C61
U56
R211
R112
R111
C112
J2
U66
J1
R100
R99
R92
R94
C35
C26
R112
R111
R208
U5
C85
R62
R61
R56
R55
R63
R74
R72
R69
R75
R73
C88
C111
R204
CR4
C7
C42
C73
C72
U58
R91
R98
R96
R106
R107
R104
R97
R95
R188
C78
U40
C44
R197
R195
R196
R194
R281
C77
R280
R282
TP10
R290
R289
R288
U92
C48
C82
C53
U57
I90
U89
U38
P1
U9
U37
RP1
C1
C3
R1
R2
R85
R118
TP9
R212
C68
C41
C42
R57
R54
R64
R53
R52
C54
P2
CR2
CR1
Q8
R202
R200
R199
U71
U36
R49
R48
R47
R45
R51
R44
R50
R46
R207
C43
U35
U39
C46
U12
R7
C14
U13
U7
C18
C19
CR8
CR7
R133
C45
R138
R132
R137
U72
U42
P3
R201
U11
U6
R3
CR5
R4
R5
C13
R8
R6
R9
Q1
R163
R162
R160
R161
C82
CR19


R102
R101
R103
R108
R110
R109
R209
R114
R113
J60
R117
R121
R120
R122
R123
R124
R125
CR9
R119
R93
C51
C50
U67
R150
R147
R149
R148
C52
R153
R154
U64
R151
CR15
R152
R155
Q3
C55
U65
U63
R105
R190
U94
C9
C77
R180
R43
R189
U93
U99
R182
R44
U97
U96
C70
CR17
C71
C79
CR18
R181
R182
P7
U80
R191
CR23
TP13
TP14
L1
C63
R166
R167
R168
C66
C65
C64
Q4
C84
U78
R171
R172
R173
R175
U91
K1
R193
R179
R178
C67
R192
C80
C62
Q5
C86
R210
C32
CR22
R174
R170
CR16
Q6
R38
C40
C38
R43
C34
C33
R35
R42
R40
R36
R37
R41
R39
C36
C37
TP8
C39
U32
U28
U30
U29
U31
U70
U33
U34
R18
R17
R16
C20
C21
R15
TP5
TP6
C17
R22
R23
R21
R20
U16
U15
U17
U19
U21
C15
R24
R128
CR6
R10
R129
C22
U10
U9
U8
U105
U104
U14
R12
R13
R14
R11
C16
U24

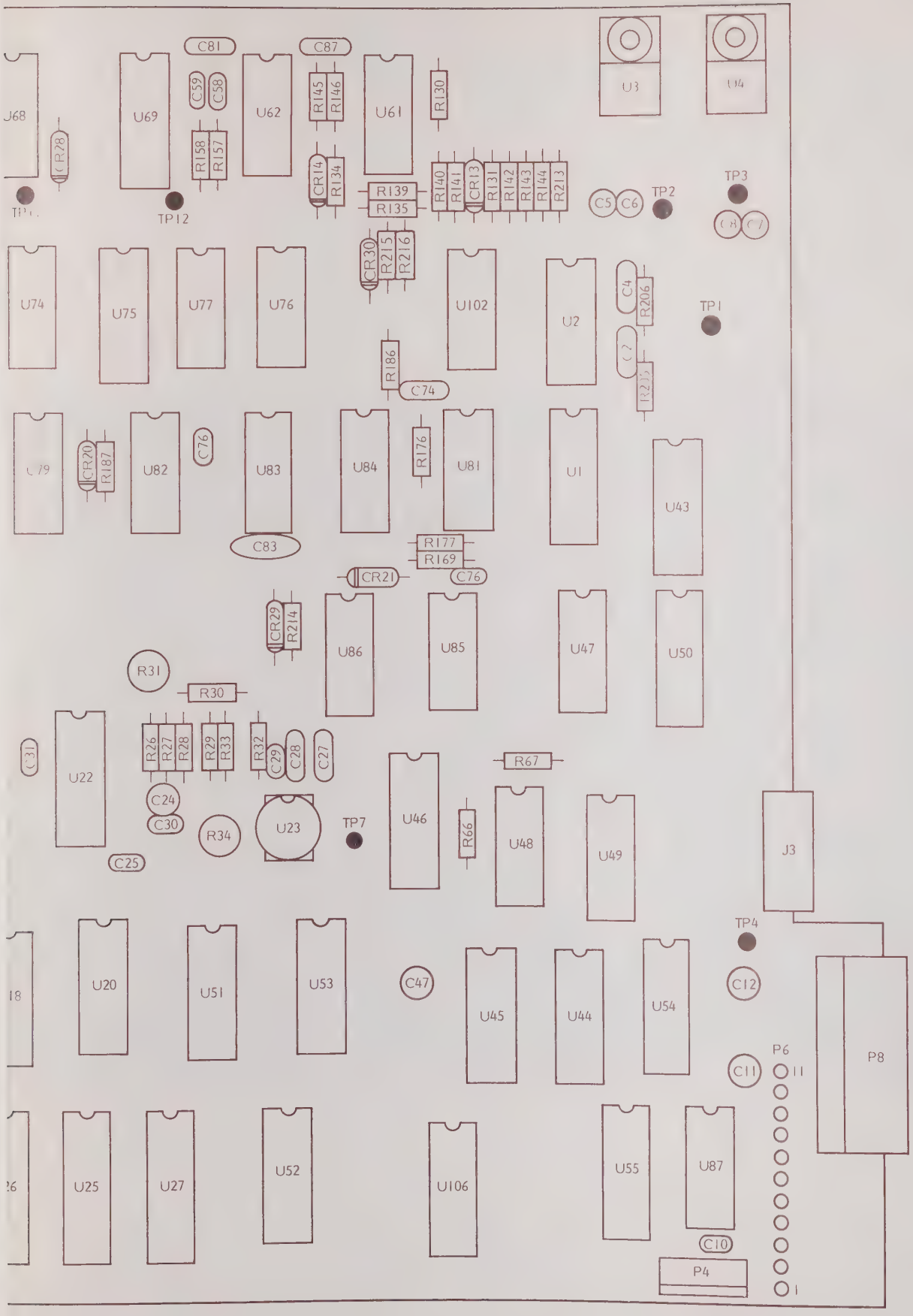


Figure 5-15. A2 (Digital) board

SECTION VI
PARTS LISTS

6-1 INTRODUCTION

This section contains replaceable parts lists and data for the Model 560A Scalar Network Analyzer. The parts lists and data are organized as follows: Network Analyzer Section; CRT Mainframe --Electrical Parts; and CRT Mainframe -- Mechanical Parts.

6-2 PARTS - ORDERING INFORMATION

Replaceable parts may be ordered either through your local representative or directly from:

WILTRON Company
P. O. Box 7290
805 East Middlefield Road
Mountain View, California 94042-7290

Telephone: (415) 969-6500
TWX: 910-379-6578

When placing your order, give complete information including the model and serial number of the instrument, the full part description, WILTRON part number, and the quantity required.

6-3 ABBREVIATIONS

The following abbreviations appear in the "DESCRIPTION" column of the WILTRON parts lists:

CC - Carbon Composition
MF - Metal Film
PLA - Programmable Logic Array
GC - Gold Contacts

6-4 REPLACEABLE PARTS - NETWORK ANALYZER SECTION

The replaceable parts lists for the network analyzer section are arranged as follows:

Table	Title	Page
6-1.	Chassis Parts	6-2
6-2.	Option 3 (A6) GPIB Parts	6-2
6-3.	Front Panel (A1) PCB Parts	6-5
6-4.	Digital (A2) Parts	6-6
6-5.	Log Amplifier (A3) PCB Parts	6-10
6-6.	Power Supply (A4) PCB Parts	6-16
6-7.	5V Regulator Assembly Parts	6-16
6-8.	Interface Control (A8) PCB Parts	6-16

Table 6-1. Replaceable Electrical and Mechanical Parts, Chassis

REF DES.	DESCRIPTION	WILTRON PART NO.
	Basic Frame Assembly	
--	Block Swage	787-651
—	Cable Assembly, Digital to Interface Control Board	560A-A-11354
--	Cable Assembly, Front Panel to Digital Board	803-26C1-3.25
--	Cable Assembly, Log Amplifier to Digital Board	802-16E-10.50
—	Casting, Front	2000-61A
—	Casting, Rear	2000-61B
—	Clamp, Cable	720-3/16
--	CRT Shield	560-C-9194
—	Frame Section, Corner	2000-61C
--	Grommet	790-55
--	Mounting Clip	721-10
—	Plunger	790-56
—	Pushbutton, grey	SPEC-C-8187-1
—	Pushbutton, white	SPEC-C-8187-2
—	Spacer	785-623
—	Spring Clip	560-A-9193
--	Washer, Nylon	900-406
	Input Connector Assembly	
--	Cable	800-115
--	Connector, 4-Pin	551-152
--	Connector, 5-Pin, 0.1 in Spacing	551-153
—	Lug, Ground	706-45
—	Receptacle, .028-Pin	551-154
	Front Panel Assembly	
C1	Capacitor, Disc, .05μF, 25V	230-35
C2	Capacitor, Disc, .05μF, 25V	230-35
C3	Capacitor, Disc, .05μF, 25V	230-35
--	Front Panel	560-D-7020-1
--	Knob, Retainer	710-56
—	Pushbutton (STORE TRACE)	SPEC-C-8187-3
--	Spring	670-8
--	Washer, Nylon	900-458
--	Knob, OFFSET	61084-A-5452
--	Knob, THRESHOLD	560-A-7069
--	Knob, TILT	61084-A-5452
—	Setscrew, ZERO dB SET	560-A-7047
	Rear Panel Assembly	
--	Cable, 560A to 6600A Interconnect	560-B-11359-1
—	Cable, Rear Panel to Digital PCB	802-14A-120
—	Cable, Rear Panel to Interface Control Board	800-182
--	Cable, Rear Panel to Digital Board	802-14A-12.0
—	Cable, Shielded, Input	800-5
—	Cable, Shielded, Penlift	800-28
—	Connector, BNC	510-5
—	Connector, BNC, Insulated	510-31
—	Connector, 2-Pin	551-123
—	Connector, 4-Pin	551-124
—	Connector Housing, 7-Pin	551-117
—	Connector Pin	551-35
—	Connector, Rear Panel to Interface Control Board	551-256
—	Connector, D-Type, Sub-miniature, 4-pin	551-315
--	Fuse, 110V, 1A	631-11
—	Fuse, 220V, .5A	631-3
—	Ground Lug, 3/8	706-5
—	Ground Lug, #6	706-12
—	Line Module Label	560-A-14656
—	Receptacle, .045-Pin	551-155
R1	Resistor:MF,51.1kΩ,1/4W,1%	110-51.1k-1
R2	Resistor:MF,15.4kΩ,1/4W,1%	110-15.4k-1
—	Solder Ferrels	771-2
S3	Switch, DP3T	430-531
—	Switch, Power	430-139
—	Switch, Slide, DPDT	430-49
S1,S2	Switch, Slide, DPDT	430-110
—	Transformer, Power Assembly	560-B-9777
S4, S5	Switch, Slide	430-156
	Cabinet Assembly	
—	Foot, Bottom	2000-61G
—	Foot, Rear	2000-61H
—	Handle	783-100
—	Interlock, Frame Section, Inner	2000-61D
—	Interlock, Frame Section, Outer	2000-61E
—	Power Cord	800-73
—	Retainer, Cabinet	2000-61I
--	Tilt Bail, Horizontal Chassis	2000-61F
--	Tilt Basil, Vertical Chassis	2000-61J

Table 6-2. Replaceable Electrical Parts, Option 3 GPIB Interface (A6) and Connector (A7) PCBs

A7	**GPIB Connector Panel Assembly**	**560-A-7007-2**
	GPIB Interconnect Panel Assembly	560-A-7042
--	Cable Assembly	804-26B1-16 1/4
--	Cable Clips	553-118
--	Connector, GPIB Interface	553-72
--	Connector Mounting Hardware	553-72A
—	Connector, Ribbon Cable Transition	551-322
R1	Resistor,10 ohm,1/4W,1%	110-10-1
—	Switch, SPST, 6 Section	430-157
A6	GPIB Interface PC Board Assembly	560A-D-7006-3
	CABLES	
--	Cable, GPIB Interface PCB to Digital PCB	802-18C-6.0
--	Clips, Cable	553-118
	CAPACITORS	
C1	Mica, 270 pF	220-270
C2	Mica, 200 pF	220-200
C3	Mica, 270 pF	220-270
C4	Mica, 820 pF	220-820
C5	Mica, 820 pF	220-820
C6	Tantalum, 10μF, 25V	250-42A
C7	Mica, 820 pF	220-820

Table 6-2. Replaceable Electrical Parts, Option 3 GPIB Interface (A6) and Connector (A7) PCBs (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
C8	Tantalum, 10µF, 25V	250-42
C9	Tantalum, 1µF, 35V	250-19A
C10	Tantalum, 1µF, 35V	250-19A
C11	Tantalum, 47µF, 35V	250-74
C12	Tantalum, 47µF, 35V	250-74
C13	Monolithic, 0.1µF, 50V	230-37
C14	Disc, .01µF, 100V	230-11
C15	Monolithic, 0.1µF, 50V	230-37
C16	Mylar, 0.1µF, 250V	210-30
C17	Monolithic, 0.1µF, 50V	230-37
C18	Monolithic, 0.1µF, 50V	230-37
C19	Mica, 390 pF	220-390
C20	Mica, 820 pF	220-820
C21	Monolithic, 0.1µF, 50V	230-37
C22	Monolithic, 0.1µF, 50V	230-37
C23	Disc, .01µF, 100V	230-11
C24	Mica, 820 pF	220-820
C25	Mylar, 0.1µF, 250V	210-30
C26	Tantalum, 10µF, 25V	250-42A
C27	Mylar, 0.1µF, 250V	210-30
C28	Mica, 820 pF	220-820
C29	Tantalum, 47µF, 35V	250-74
C30	Mylar, 0.1µF, 250V	210-30
C31	Mylar, 0.1µF, 250V	210-52
C32	Mylar, 0.1µF, 250V	210-52
C33	Tantalum, 1µF, 35V	250-98
C34	Tantalum, 10µF, 25V	250-99
C35	Mica, .0022µF	227-51
C36	Monolithic, 0.1µF, 50V	230-37
C37	Monolithic, 0.1µF, 50V	230-37
C38	Monolithic, 0.1µF, 50V	230-37
C39	Monolithic, 0.1µF, 50V	230-37
C40	Monolithic, 0.1µF, 50V	230-37
C41	Monolithic, 0.1µF, 50V	230-37
C42	Monolithic, 0.1µF, 50V	230-37
C43	Monolithic, 0.1µF, 50V	230-37
C44	Monolithic, 0.1µF, 50V	230-37
C45	Monolithic, 0.1µF, 50V	230-37
C46	Monolithic, 0.1µF, 50V	230-37
C47	Monolithic, 0.1µF, 50V	230-37
C48	Mica, 1000 pF	227-13
C49	Monolithic, 0.1µF, 50V	230-37
	CONNECTORS	
P1	26-Pin, 0.1-in Spacing	551-102
	DIODES	
CR1	Silicon, 1N4446	10-1N4446
CR2	Silicon, 1N4446	10-1N4446
CR3	Silicon, 1N4446	10-1N4446
CR4	Silicon, 1N4446	10-1N4446
CR5	Silicon, 1N4446	10-1N4446
CR6	Silicon, 1N4446	10-1N4446
CR7	Silicon, 1N4446	10-1N4446
CR8	Silicon, 1N4446	10-1N4446
CR9	Silicon, 1N4446	10-1N4446
CR10	Silicon, 1N4446	10-1N4446
	INTEGRATED CIRCUITS	
U1	GPIB Bus Transceiver (MC3441P)	54-75
U2	GPIB Bus Transceiver (MC3441P)	54-75
U3	GPIB Bus Transceiver (MC3441P)	54-75
	(MC3440P)	54-126
U4	GPIB Bus Transceiver (MC3441P)	54-75
	(MC3440P)	54-126
U5	74C86 Quad 2-Input EXOR	54-69
U6	74C86 Quad 2-Input EXOR	54-69
U7	74C30 Single 8-Input NAND	54-66
U8	74C08 Quad 2-Input AND	54-35
U9	74C04 Hex Inverter	54-34
U10	74C32 Quad 2-Input OR	54-67
U11	74C107 Dual J-K Flip-Flop	54-37
U12	74C04 Hex Inverter	54-34
U13	74C10 Triple 3-Input NAND	54-64
U14	74C00 Quad 2-Input NAND	54-32
U15	74C08 Quad 2-Input AND	54-35
U16	74C107 Dual J-K Flip-Flop	54-37
U17	74C08 Quad 2-Input AND	54-35
U18	74C221 Dual One-Shot	54-70
U19	74C02 Quad 2-Input NOR	54-33
U20	74C107 Dual J-K Flip-Flop	54-37
U21	74C08 Quad 2-Input AND	54-35
U22	74C32 Quad 2-Input OR	54-67
U23	74C04 Hex Inverter	54-34
U24	74C10 Triple 3-Input NAND	54-64
U25	Not used	
U26	74C107 Dual J-K Flip-Flop	54-37
U27	74C00 Quad 2-Input NAND	54-32
U28	Programmable Logic Array	54-123
U29	Dual 2-BIT Decoder (MC14555BCP)	54-73
U30	4-BIT Decoder (MC14514P)	54-71
U31	74C175 Quad D Flip-Flop	54-81
U32	74C175 Quad D Flip-Flop	54-81
U33	74C175 Quad D Flip-Flop	54-81
U34	74C08 Quad 2-Input AND	54-35
U35	74C00 Quad 2-Input NAND	54-32
U36	74C04 Hex Inverter	54-34
U37	74C04 Hex Inverter	54-34
U38	74C10 Triple 3-Input NAND	54-64
U39	74C20 Dual 4-Input NAND	54-65
U40	74C02 Quad 2-Input NOR	54-33
U41	74C74 Dual D Flip-Flop	54-68
U42	74C74 Dual D Flip-Flop	54-68
U43	Triple 3-Input NOR (CD4025B)	54-85
U44	74C10 Triple 3-Input NAND	54-64
U45	74C32 Quad 2-Input OR	54-67
U46	Hex Tri-State Buffer (DM80C98)	54-78
U47	Hex Tri-State Buffer (DM80C98)	54-78
U48	Hex Tri-State Buffer (DM80C98)	54-78
U49	Hex Tri-State Buffer (DM80C98)	54-78
U50	Hex Tri-State Buffer (DM80C98)	54-78
U51	Octal D-Latch Tri-State Outputs	54-88
U52	Hex Tri-State Buffer (DM80C98)	54-78
U53	Hex Tri-State Buffer (DM80C98)	54-78
U54	Hex Tri-State Buffer (DM80C98)	54-78
U55	Hex Tri-State Buffer (DM80C98)	54-78
U56	74C161 Synchronous Up Counter	54-80
U57	74C42 Single 4:10 Decoder	54-79
U58	74C08 Quad 2-Input AND	54-35
U59	Dual Analog Switch (DG200B)	50-DG200BA
U60	Dual Comparator (LM319H)	54-49
U61	16-Bit D/A .	60-9
U62	74C00 Quad 2-Input NAND	54-32
U63	74C04 Hex Inverter	54-34

Table 6-2. Replaceable Electrical Parts, Option 3 GPIB Interface (A6) and Connector (A7) PCBs (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
U64	74C00 Quad 2-Input NAND	54-32
U65	Successive Approximation Register (MC14559BCP)	54-74
U66	Successive Approximation Register (MC14549BCP)	54-72
U67	74C107 Dual J-K Flip-Flop	54-37
U68	74C30 Single 8-Input NAND	54-66
U69	74C04 Hex Inverter	54-34
U70	74C04 Hex Inverter	54-34
U71	74C04 Hex Inverter	54-34
U72	74C04 Hex Inverter	54-34
U73	Quad Op. Amp. (TL074)	54-132
U74	74C74 Dual D Flip-Flop	54-68
U75	Dual Comparator (LM319H)	54-49
U76	74C86 Quad 2-Input EXOR	54-69
U77	Quad Analog Switch (DG201 or LF13201)	54-24
U78	74C107 Dual J-K Flip-Flop	54-37
U79	74C02 Quad 2-Input NOR	54-33
U80	74C221 Dual One-Shot	54-70
U81	74C221 Dual One-Shot	54-70
U82	74C04 Hex Inverter	54-34
U83	74C107 Dual J-K Flip-Flop	54-37
U84	74C107 Dual J-K Flip-Flop	54-37
U85	74C74 Dual D Flip-Flop	54-68
U86	74C221 Dual One-Shot	54-70
U87	74C221 Dual One-Shot	54-70
U88	Dual 2-Bit Decoder (MC14555BCP)	54-73
U89	74C74 Dual D Flip-Flop	54-68
U90	74C10 Triple 3-Input NAND	54-64
U91	74C00 Quad 2-Input NAND	54-32
U92	74C32 Quad 2-Input OR	54-67
U93	74C32 Quad 2-Input OR	54-67
VR1	+15V Regulator	54-21
VR2	-15V Regulator	54-MC7915CP
	RESISTORS	
R1	MF, 10.7k, 1/4W, 1%	110-10.7k-1
R2	MF, 10k, 1/4W, 1%	110-10k-1
R3	MF, 82.5k, 1/4W, 1%	110-82.5k-1
R4	MF, 10Ω, 1/4W, 1%	110-10-1
R5	Not used	
R6	CC, 4.7M, 1/2W, 5%	101-4.7M-5
R7	Not used	
R8	Trimmer, 10k	158-8
R9	Trimmer, 50k	158-1
R10	MF, 150k, 1/4W, 1%	110-150k-1
R11	MF, 6.19k, 1/4W, 1%	110-6.19k-1
R12	MF, 150k, 1/4W, 1%	110-150k-1
R13	MF, 100Ω, 1/4W, 1%	110-100-1
R14	MF, 150Ω, 1/4W, 1%	110-150-1
R15	MF, 3.74k, 1/4W, 1%	110-3.74k-1
R16	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R17	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R18	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R19	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R20	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R21	MF, 5.49k, 1/4W, 1%	110-5.49k-1
R22	MF, 11.5k, 1/4W, 1%	110-11.5k-1
R23	MF, 4.99k, 1/4W, 0.1%	113-4.99k-1
R24	MF, 20k, 1/4W, 0.1%	113-20k-1
R25	MF, 4.53k, 1/4W, 0.1%	113-4.53k-1
R26	MF, 3.32k, 1/4W, 1%	110-3.32k-1
R27	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R28	MF, 100k, 1/4W, 1%	110-100k-1
R29	Trimmer, 100k	157-100k-A
R30	MF, 1k, 1/4W, 1%	110-1k-1
R31	MF, 49.9k, 1/4W, 1%	110-49.9k-1
R32	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R33	MF, 100k, 1/4W, 1%	110-100k-1
R34	MF, 34k, 1/4W, 1%	110-34k-1
R35	MF, 1k, 1/4W, 1%	110-1k-1
R36	MF, 100k, 1/4W, 1%	110-100k-1
R37	Trimmer, 50k	157-50k-A
R38	MF, 76.8k, 1/4W, 1%	110-76.8k-1
R39	MF, 76.8k, 1/4W, 1%	110-76.8k-1
R40	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R41	Trimmer, 2k	157-2k-A
R42	MF, 49.9k, 1/4W, 1%	110-49.9k-1
R43	MF, 10k, 1/4W, 1%	110-10k-1
R44	MF, 10k, 1/4W, 1%	110-10k-1
R45	MF, 10k, 1/4W, 1%	110-10k-1
R46	MF, 4.53k, 1/4W, 1%	110-4.53k-1
R47	MF, 20k, 1/4W, 1%	110-20k-1
R48	MF, 60.4k, 1/4W, 1%	110-60.4k-1
R49	MF, 60.4k, 1/4W, 1%	110-60.4k-1
R50	MF, 34k, 1/4W, 1%	110-34k-1
R51	MF, 19.6k, 1/4W, 1%	110-19.6k-1
R52	MF, 10k, 1/4W, 1%	110-10k-1
R53	MF, 10k, 1/4W, 1%	110-10k-1
R54	MF, 10k, 1/4W, 1%	110-10k-1
R55	MF, 10k, 1/4W, 1%	110-10k-1
R56	MF, 10k, 1/4W, 1%	110-10k-1
R57	MF, 10k, 1/4W, 1%	110-10k-1
R58	MF, 10k, 1/4W, 1%	110-10k-1
RP1	Resistor Pack, Single In-Line, 10k	123-6
RP2	Resistor Pack, Single In-Line, 10k	123-6
RP3	Resistor Pack, Single In-Line, 10k	123-6
RP4	Resistor Pack, Single In-Line, 10k	123-6
	SOCKETS	
J1	Socket, DIP, 18-Pin	551-148
--	Socket, DIP, 24-Pin, for U61	553-67
	TEST POINTS	
TP1 thru TP26	Test Points	706-44
	TRANSISTORS	
Q1	2N2222A	20-2N2222A

Table 6-3. Replaceable Electrical Parts, Front Panel (A1) PCB

REF DES.	DESCRIPTION	WILTRON PART NO.
A1	**Front Panel PC Board Assembly**	**560A-D-7001-3**
	CAPACITORS	
C1	Tantalum, 10µF, 25V	250-42
C2	Monolithic, 0.1µF	230-37
C3	Monolithic, 0.1µF	230-37
C4	0.22µF	227-47
C5	Mylar, 0.1µF	227-45
C6	Mylar, 0.1µF	227-45
C7	Monolithic, 0.1µF	230-37
C8	Mica, 100pF	223-100
C9	0.22µF	227-47
C10	Mylar, 0.1µF	227-45
C11	Mylar, 0.1µF	227-45
C12	Monolithic, 0.1µF	230-37
C13	Mica, 100pF	223-100
C14	Tantalum, 4.7µF, 35V	250-39A
C15	Mica, 270pF	223-270
C16	Mica, 270pF	223-270
C17	Monolithic, 0.1µF	230-37
C18	Monolithic, 0.1µF	230-37
	CONNECTORS	
P1	26-Pin, 0.1 in. Spacing	551-102
P2	26-Pin, 0.1 in. Spacing	551-102
P3	26-Pin, 0.1 in. Spacing	551-102
	DIODES	
CR1	Zener, 1N758A, 10V, 0.4W	10-43
CR2	Zener, 1N758A, 10V, 0.4W	10-43
CR3	Zener, 1N758A, 10V, 0.4W	10-43
CR4	Zener, 1N758A, 10V, 0.4W	10-43
CR5	Silicon, 1N4446	10-1N4446
CR6	Silicon, 1N4446	10-1N4446
CR7	Zener, 1N751A, 5.1V, 0.4W	10-1N751A
CR8	Reference, 1N823, 6.2V	10-1N823
	DISPLAYS	
DS1	LED, ±1, MAN73A	15-3
DS2	LED, 7 Segment, MAN71A	15-4
DS3	LED, 7 Segment, MAN71A	15-4
DS4	LED, 7 Segment, MAN71A	15-4
DS5	LED, ±1, MAN73A	15-3
DS6	LED, 7 Segment, MAN71A	15-4
DS7	LED, 7 Segment, MAN71A	15-4
DS8	LED, 7 Segment, MAN71A	15-4
DS9	Diode, Light Emitting, Red, RL4484	15-5
DS10	Diode, Light Emitting, Yellow, MV5374C	15-7
DS11	Diode, Light Emitting, Yellow, MV5374C	15-7
DS12	Diode, Light Emitting, Red, RL4484	15-5
DS13	Diode, Light Emitting, Yellow, MV5374C	15-7
DS14	Diode, Light Emitting, Yellow, MV5374C	15-7
DS15	Diode, Light Emitting, Yellow, MV5374C	15-7
DS16	Diode, Light Emitting, Yellow, MV5374C	15-7
DS17	Diode, Light Emitting, Yellow, MV5374C	15-7
DS18	Diode, Light Emitting, Yellow, MV5374C	15-7
DS19	Diode, Light Emitting, Yellow, MV5374C	15-7
DS20	Diode, Light Emitting, Yellow, MV5374C	15-7
DS21	Diode, Light Emitting, Red, RL4484	15-5
DS22	Diode, Light Emitting, Red, RL4484	15-5
	INTEGRATED CIRCUITS	
U1	Quad Op. Amp. (TL074)	54-132
U2	Quad Op. Amp. (TL074)	54-132
U3	Dual Op. Amp. (TL072)	54-53
U4	Dual Op. Amp. (TL072)	54-53
U5	74LS00 Quad NOR	54-74LS00
U6	3 1/2 Digit DVM (ICL7107CPL)	54-31
U7	3 1/2 Digit DVM (ICL7107CPL)	54-31
	RESISTORS	
R1	MF, 261Ω, 1/4W, 1%	110-261-1
R2	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R3	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R4	MF, 20k, 1/4W, 1%	110-20k-1
R5	MF, 20k, 1/4W, 1%	110-20k-1
R6	MF, 10k, 1/4W, 1%	110-10k-1
R7	MF, 10k, 1/4W, 1%	110-10k-1
R8	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R9	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R10	MF, 10.2k, 1/4W, 1%	110-10.2k-1
R11	Variable, 20k	146-4
R12	MF, 21k, 1/4W, 1%	110-21k-1
R13	MF, 54.9k, 1/4W, 1%	110-54.9k-1
R14	MF, 261Ω, 1/4W, 1%	110-261-1
R15	MF, 124k, 1/4W, 1%	110-124k-1
R16	MF, 10Ω, 1/4W, 1%	110-10-1
R17	Variable, 10k	150-10kB
R18	MF, 332k, 1/4W, 1%	110-332k-1
R19	MF, 499k, 1/4W, 1%	110-499k-1
R20	Variable, 10k	150-10kB
R21	MF, 2.49k, 1/4W, 1%	110-2.49k-1
R22	MF, 261Ω, 1/4W, 1%	110-261-1
R23	MF, 261Ω, 1/4W, 1%	110-261-1
R24	MF, 11k, 1/4W, 1%	110-11k-1
R25	MF, 1k, 1/4W, 1%	110-1k-1
R26	Variable, 500k	146-2
R27	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R28	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R29	Variable, 20k	146-3
R30	MF, 20k, 1/4W, 1%	110-20k-1
R31	MF, 20k, 1/4W, 1%	110-20k-1
R32	MF, 10k, 1/4W, 1%	110-10k-1
R33	MF, 10k, 1/4W, 1%	110-10k-1
R34	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R35	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R36	MF, 10.2k, 1/4W, 1%	110-10.2k-1

Table 6-3. Replaceable Electrical Parts, Front Panel (A1) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
R37	Variable, 20k	146-4
R38	MF, 21k, 1/4W, 1%	110-21k-1
R39	MF, 54.9k, 1/4W, 1%	110-54.9k-1
R40	MF, 261Ω, 1/4W, 1%	110-261-1
R41	MF, 124k, 1/4W, 1%	110-124k-1
R42	MF, 10Ω, 1/4W, 1%	110-10-1
R43	Variable, 10k	150-10kB
R44	Variable, 20k	146-5
R45	MF, 261Ω, 1/4W, 1%	110-261-1
R46	MF, 332k, 1/4W, 1%	110-332k-1
R47	MF, 499k, 1/4W, 1%	110-499k-1
R48	Variable, 5k	146-6
R49	MF, 7.87k, 1/4W, 1%	110-7.87k-1
R50	MF, 287k, 1/4W, 1%	110-287k-1
R51	MF, 261Ω, 1/4W, 1%	110-261-1
R52	MF, 20k, 1/4W, 1%	110-20k-1
R53	MF, 2.49k, 1/4W, 1%	110-2.49k-1
R54	Variable, 10k	150-10kB
R55	MF, 10k, 1/4W, 1%	110-10k-1
R56	MF, 261Ω, 1/4W, 1%	110-261-1
R57	MF, 261Ω, 1/4W, 1%	110-261-1
R58	MF, 10k, 1/4W, 1%	110-10k-1
R59	MF, 499Ω, 1/4W, 1%	110-499-1
R60	MF, 499Ω, 1/4W, 1%	110-499-1
R61	MF, 221k, 1/4W, 1%	110-221k-1
R62	MF, 100k, 1/4W, 1%	110-100k-1
R63	MF, 115k, 1/4W, 0.1%	113-115k-0.1
R64	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R65	MF, 499Ω, 1/4W, 1%	110-499-1
R66	MF, 499Ω, 1/4W, 1%	110-499-1
R67	MF, 1.78k, 1/4W, 1%	110-1.78k-1
R68	MF, 221k, 1/4W, 1%	110-221k-1
R69	MF, 115k, 1/4W, 0.1%	113-115k-0.1
R70	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R71	MF, 1.13k, 1/4W, 1%	110-1.13k-1
R72	MF, 24.3k, 1/4W, 1%	110-24.3k-1
R73	Trimmer, 1k, 10 Turn	157-1kA
R74	MF, 4.22k, 1/4W, 1%	110-4.22k-1
R75	MF, 100k, 1/4W, 1%	110-100k-1
R76	MF, 10k, 1/4W, 1%	110-10k-1
R77	MF, 196k, 1/4W, 1%	110-196k-1
R78	MF, 10k, 1/4W, 1%	110-10k-1
R79	MF, 10k, 1/4W, 1%	110-10k-1
R80	MF, 95.3k, 1/4W, 1%	110-95.3k-1
R81	MF, 10k, 1/4W, 1%	110-10k-1
R82	MF, 10k, 1/4W, 1%	110-10k-1
R83	CC, 2.2M, 1/4W, 5%	101-2.2M-5
R84	Trimmer, 50k, 1 Turn	158-1
R85	CC, 2.2M, 1/4W, 5%	101-2.2M-5
R86	Trimmer, 50k, 1 Turn	158-1
R87	MF, 10k, 1/4W, 1%	110-10k-1
R88	MF, 10k, 1/4W, 1%	110-10k-1
R89	MF, 261Ω, 1/4W, 1%	110-261-1
	SOCKETS	
---	14-Pin DIP, Low Profile	553-63
---	40-Pin DIP, Low Profile	553-66
---	Spacer, Nylon, 13/16 inch	790-95
	SWITCHES	
S1-S3	Switch Assembly, 3 x DPDT, GC	430-95
S4	DPDT, Push On, Push Off, GC	430-138
S5	SPDT, Momentary, GC	430-99
S6-S9	Switch Assembly, 4 x DPST, GC	430-94
S10-S15	Switch Assembly, 6 x DPST, GC	430-93
S16	SPDT, Momentary, GC	430-99
S17	DPDT, Push On, Push Off, GC	430-138
S18	SPDT, Push On, Push Off, GC	430-151
S19-S21	Switch Assembly, 3 x DPDT, GC	430-95
S22	DPDT, Push On, Push Off, GC	430-138
S23	SPDT, Momentary, GC	430-99
S24	P/O Threshold Potentiometer R26	146-2
S25-S28	Switch Assembly, 4 x DPST, GC	430-94
S29-S34	Switch Assembly, 6 x DPST, GC	430-93
S35	SPDT, Momentary, GC	430-99
S36 & S37	Switch Assembly, 1 x DPDT, 1 x SPDT, GC	430-96
S38	DPDT, Push On, Push Off, GC	430-138
S39	DPDT, Push On, Push Off, GC	430-138
S40	SPDT, Momentary, GC	430-99
S41	SPDT, Momentary, GC	430-99
S42	SPDT, Push On, Push Off, GC	430-151
	TEST POINTS	
TP1, TP2	Test Points	706-44
	MISCELLANEOUS	
--	Shaft, Extender, OFFSET Control	560A-A-12545

Table 6-4. Replaceable Electrical Parts, Digital (A2) PCB

A2	**Digital PC Board Assembly**	**560A-D-7002-3**
	CAPACITORS	
C1	Tantalum, 10µF, 25V	250-42
C2	Disc, 0.001µF, 1kV	230-3
C3	Tantalum, 10µF, 25V	250-42
C4	Disc, 0.001µF, 1kV	230-3
C5	Tantalum, 10µF, 25V	250-42A
C6	Tantalum, 10µF, 25V	250-42A
C7	Tantalum, 10µF, 25V	250-42A
C8	Tantalum, 10µF, 25V	250-42A
C9	Tantalum, 150µF, 6V	250-57
C10	Monolithic, 0.1µF, 50V	230-37
C11	Tantalum, 4.7µF, 35V	250-39A
C12	Tantalum, 4.7µF, 35V	250-39A
C13	Mica, 100pF	223-100
C14	Mica, 330pF	223-330
C15	Tantalum, 10µF, 25V	250-42A
C16	Tantalum, 10µF, 25V	250-42A
C17	Tantalum, 10µF, 25V	250-42A
C18	Tantalum, 10µF, 25V	250-42A
C19	Tantalum, 10µF, 25V	250-42A

Table 6-4. Replaceable Electrical Parts, Digital (A2) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
C20	Monolithic, 0.1µF, 50V	230-37
C21	Tantalum, 10µF, 25V	250-42A
C22	Disc, .01µF	230-11
C23	Monolithic, 0.1µF, 50V	230-37
C24	Tantalum, 10µF, 25V	250-42A
C25	Monolithic, 0.1µF, 50V	230-37
C26	Mica, 110pF	223-110
C27	Mica, 27pF	220-27
C28	Not used	
C29	Monolithic, 0.1µF, 50V	230-37
C30	Monolithic, 0.1µF, 50V	230-37
C31	Monolithic, 0.1µF, 50V	230-37
C32	Tantalum, 10µF, 25V	250-42A
C33	Tantalum, 10µF, 25V	250-42A
C34	Monolithic, 0.1µF, 50V	230-37
C35	Disc, 0.001µF, 50V	230-30
C36	Mica, 68pF	223-68
C37	Monolithic, 0.1µF, 50V	230-37
C38	Monolithic, 0.1µF, 50V	230-37
C39	Monolithic, 0.1µF, 50V	230-37
C40	Tantalum, 10µF, 25V	250-42
C41	Mylar, 0.1µF, 100V	210-30
C42	Mica, 1000pF	227-13
C43	Disc, 0.001µF, 1kV	230-3
C44	Monolithic, 0.1µF, 50V	230-37
C45	Monolithic, 0.1µF, 50V	230-37
C46	Monolithic, 0.1µF, 50V	230-37
C47	Tantalum, 10µF, 25V	250-42A
C48	Polycarbonate, 20µF	210-55
C49	Mylar, 0.1µF, 100V	210-30
C50	Tantalum, 10µF, 25V	250-42A
C51	Tantalum, 10µF, 25V	250-42A
C52	Tantalum, 10µf, 25V	250-42A
C53	Disc, .002µF	230-33
C54	Mica, 270pF	223-270
C55	Tantalum, 10µF, 25V	250-42A
C56	Tantalum, 2.2µF, 20V	250-40A
C57	NOT USED	
C58	Tantalum, 10µF, 25V	250-42A
C59	Tantalum, 10µF, 25V	250-42A
C60	Monolithic, 0.1µF, 50V	230-37
C61	Monolithic, 0.1µF, 50V	230-37
C62	Tantalum, 10µF, 25V	250-42A
C63	Monolithic, 0.1µF, 50V	230-37
C64	Mica, 560pF	220-560
C65	Mica, 470pF	220-470
C66	Tantalum, 10µF, 25V	250-42A
C67	Tantalum, 68µF, 6V	250-58A
C68	Tantalum, 10µF, 25V	250-42A
C69	Disc, 0.001µF, 50V	230-30
C70	Tantalum, 4.7µF, 35V	250-39A
C71	Tantalum, 68µF, 6V	250-58A
C72	Mica, 130pF	223-130
C73	Disc, 0.001µF, 50V	230-30
C74	Mica, 330pF	223-330
C75	Monolithic, 0.1µF, 50V	230-37
C76	Monolithic, 0.1µF, 50V	230-37
C77	Disc, 0.001µF, 50V	230-30
C78	Disc, 0.001µF, 50V	230-30
C79	Disc, 0.001µF, 50V	230-30
C80	Disc, 0.001µF, 50V	230-30
C81	Disc, 0.05µF, 25V	230-35
C82	Mica, 330pF	220-330
C83	Disc, .01µF	230-11
C84	Monolithic, .01µF	230-11
C85	Mica, 270pF	223-270
C86	Tantalum, 68µF, 6V	250-58
C87	Monolithic, .0047µF	230-36
C88	Monolithic, 0.1µF, 50V	230-37
C89	Monolithic, .01µF, 50v	250-77
	CONNECTORS	
P1	Male, 26-Pin	551-102
P2	Male, 26-Pin	551-102
P3	Male, 26-Pin	551-102
P4	Male, 6-Pin	551-131
P5	Male, 4-Pin	551-120
P6	Not used	
P7	Male, 3-Pin	551-146
	Connector Housing	551-85
	Connector Socket	551-35
P8	Male, 11-Pin	551-272
	DIODES	
CR1	Silicon, 1N4446	10-1N4446
CR2	Silicon, 1N4446	10-1N4446
CR3	Silicon, 1N4446	10-1N4446
CR4	Silicon, 1N4446	10-1N4446
CR5	Silicon, 1N4446	10-1N4446
CR6	Silicon, 1N4446	10-1N4446
CR7	Silicon, 1N4446	10-1N4446
CR8	Silicon, 1N4446	10-1N4446
CR9	Silicon, 1N4446	10-1N4446
CR10	Silicon, 1N4446	10-1N4446
CR11	Silicon, 1N4446	10-1N4446
CR12	Silicon, 1N4446	10-1N4446
CR13	Silicon, 1N4446	10-1N4446
CR14	Zener, 1N750A, 4.7V, 0.4W	10-11
CR15	Silicon, 1N4446	10-1N4446
CR16	Silicon, 1N4446	10-1N4446
CR17	Silicon, 1N4446	10-1N4446
CR18	Silicon, 1N4446	10-1N4446
CR19	Silicon, 1N4446	10-1N4446
CR20	Germanium, 1N270	10-10
CR21	Germanium, 1N270	10-10
CR22	Silicon, 1N4446	10-1N4446
CR23	Germanium, 1N270	10-10
CR24	Germanium, 1N270	10-10
CR25	Germanium, 1N270	10-10
CR26	Germanium, 1N270	10-10
CR27	Silicon, 1N4446	10-1N4446
CR28	Germanium, 1N270	10-10
CR29	Germanium, 1N270	10-10
CR30	Zener, IN750A, 4.7V	10-11
	INDUCTOR	
L1	100µH	310-45
	INTEGRATED CIRCUITS	
U1	Quad ±10V FET Switch	54-20
U2	Quad JFET Op. Amp. (TL074CN)	54-132
U3	+15V Regulator (MC7815CP)	54-21
U4	-15V Regulator (MC7915CP)	54-MC7915CP
U5	Dual Comparator (LM319H)	54-49
U6	74LS02 Quad NOR	54-57
U7	74LS74 Dual D Flip-Flop	54-44

Table 6-4. Replaceable Electrical Parts, Digital (A2) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
U8	74LS161 Binary Counter	54-60
U9	74LS161 Binary Counter	54-60
U10	74LS161 Binary Counter	54-60
U11	74LS74 Dual D Flip-Flop	54-44
U12	74LS00 Quad NAND	54-74LS00
U13	74LS00 Quad NAND	54-74LS00
U14	10 Bit D/A Converter (MC3410CP)	54-48
U15	10 Bit D/A Converter (MC3410CP)	54-48
U16	Comparator (LM311H)	54-30
U17	SAR (DM2504CN)	54-55
U18	74LS367 Hex Tri-State Buffer	54-74LS367
U19	74LS367 Hex Tri-State Buffer	54-74LS367
U20	74LS174 Hex Latch	54-43
U21	74LS175 Quad Latch	54-74LS175
U22	10 Bit D/A Converter (MC3410CP)	54-48
U23	Operational Amplifier (LF356N)	50-9
U24	4k Static RAM (2114)	54-47
U25	4k Static RAM (2114)	54-47
U26	4k Static RAM (2114)	54-47
U27	4k Static RAM (2114)	54-47
U28	74LS367 Hex Tri-State Buffer	54-74LS367
U29	74LS367 Hex Tri-State Buffer	54-74LS367
U30	74LS174 Hex Latch	54-43
U31	74LS175 Quad Latch	54-74LS175
U32	10 Bit D/A Converter (MC3410CP)	54-48
U33	4k Static RAM (2114)	54-47
U34	4k Static RAM (2114)	54-47
U35	Quad JFET Op. Amp. (TL074CN)	54-132
U36	Quad ±10V FET Switch	54-20
U37	74LS174 Hex Latch	54-43
U38	74LS174 Hex Latch	54-43
U39	Quad ±10V FET Switch	54-20
U40	Quad ±10V FET Switch	54-20
U41	Quad ±10V FET Switch	54-20
U42	Quad JFET Op. Amp. (TL074CN)	54-132
U43	74LS161 Binary Counter	54-60
U44	74LS161 Binary Counter	54-60
U45	74LS161 Binary Counter	54-60
U46	74LS161 Binary Counter	54-60
U47	74LS00 Quad NAND	54-74LS00
U48	74LS02 Quad NOR	54-57
U49	74LS00 Quad NAND	54-74LS00
U50	74LS174 Hex Latch	54-43
U51	74LS367 Hex Tri-State Buffer	54-74LS367
U52	74LS367 Hex Tri-State Buffer	54-74LS367
U53	74LS367 Hex Tri-State Buffer	54-74LS367
U54	74LS367 Hex Tri-State Buffer	54-74LS367
U55	74LS367 Hex Tri-State Buffer	54-74LS367
U56	Quad JFET Op. Amp. (TL074CN)	54-132
U57	Quad ±10V FET Switch	54-20
U58	Quad JFET Op. Amp. (TL074CN)	54-132
U59	Quad ±15V FET Switch (DG201CJ)	54-24
U60	Quad JFET Op. Amp. (TL074CN)	54-132
U61	Quad JFET Op. Amp. (TL074CN)	54-132
U62	74LS132 Quad Schmitt NAND	54-74LS132
U63	74LS02 Quad NOR	54-57
U64	Quad Comparator (MC3302P)	54-MC3302P
U65	74LS00 Quad NAND	54-74LS00
U66	74LS157 Quad 2-Input Multiplexer	54-59
U67	74LS73 Dual J-K Flip-Flop	54-74LS73
U68	74LS74 Dual D Flip-Flop	54-44
U69	96L02 Dual Monostable	54-96L02
U70	1k Static RAM (2102AL-4)	54-46
U71	74LS74 Dual D Flip-Flop	54-44
U72	74LS00 Quad NAND	54-74LS00
U73	Not used	
U74	74LS04 Hex Inverter	54-74LS04
U75	14 Stage Counter (CD4040BC)	54-56
U76	74LS00 Quad NAND	54-74LS00
U77	74LS10 Triple NAND	54-42
U78	74LS74 Dual D Flip-Flop	54-44
U79	74LS02 Quad NOR	54-57
U80	74LS157 Quad 2-Input Multiplexer	54-59
U81	74LS01 Quad NAND, Open Collector	54-74SL01
U82	74LS74 Dual D Flip-Flop	54-44
U83	74LS02 Quad NOR	54-57
U84	74LS02 Quad NOR	54-57
U85	74LS74 Dual D Flip-Flop	54-44
U86	74LS00 Quad NAND	54-74LS00
U87	74LS30 8-Input NAND	54-58
U88	74LS02 Quad NOR	54-57
U89	74LS74 Dual D Flip-Flop	54-44
U90	74LS00 Quad NAND	54-74LS00
U91	74LS04 Hex Inverter	54-74LS04
U92	74LS74 Dual D Flip-Flop	54-44
U93	74LS00 Quad NAND	54-74LS00
U94	74LS02 Quad NOR	54-57
U95	74LS74 Dual D Flip-Flop	54-44
U96	96L02 Dual Monostable	54-96L02
U97	74LS00 Quad NAND	54-74LS00
U98	74LS10 Triple NAND	54-42
U99	74LS00 Quad NAND	54-74LS00
U100	74LS02 Quad NOR	54-57
U101	74LS74 Dual D Flip-Flop	54-44
U102	74LS00 Quad NAND	54-74LS00
U103	74LS02 Quad NOR	54-57
U104	1k Static RAM (2102AL-4)	54-46
U105	1k Static RAM (2102AL-4)	54-46
U106	1k Static RAM (2102AL-4)	54-46
	RELAYS	
RLY1	DPST, 5V	690-19
	RESISTORS	
R1	MF, 10k, 1/4W, 1%	110-10k-1
R2	MF, 10k, 1/4W, 1%	110-10k-1
R3	MF, 1k, 1/4W, 1%	110-1k-1
R4	MF, 511Ω, 1/4W, 1%	110-511-1
R5	MF, 26.1k, 1/4W, 1%	110-26.1k-1
R6	MF, 3.32k, 1/4W, 1%	110-3.32k-1
R7	MF, 215Ω, 1/4W, 1%	110-215-1
R8	MF, 1k, 1/4W, 1%	110-1k-1
R9	MF, 3.32k, 1/4W, 1%	110-3.32k-1
R10	Trimmer, 500Ω	157-500A
R11	MF, 10Ω, 1/4W, 1%	110-10-1
R12	MF, 1k, 1/4W, 1%	110-1k-1
R13	MF, 7.5k, 1/4W, 1%	110-7.5k-1
R14	MF, 1.15k, 1/4W, 1%	110-1.15k-1

Table 6-4. Replaceable Electrical Parts, Digital (A2) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.	REF DES.	DESCRIPTION	WILTRON PART NO.
R15	MF, 10Ω, 1/4W, 1%	110-10-1	R79	Trimmer, 1k	158-2
R16	MF, 7.5k, 1/4W, 1%	110-7.5k-1	R80	MF, 2.8k, 1/4W, 1%	110-2.8k-1
R17	MF, 1.15k, 1/4W, 1%	110-1.15k-1	R81	Trimmer, 100k	158-6
R18	MF, 1k, 1/4W, 1%	110-1k-1	R82	MF, 115k, 1/4W, 1%	110-115k-1
R19	Trimmer, 1k	158-2	R83	MF, 13.3k, 1/4W, 1%	110-13.3k-1
R20	MF, 4.53 k, 1/4W, 1%	110-4.53k-1	R84	MF, 100k, 1/4W, 1%	110-100k-1
R21	MF, 4.99k, 1/4W, 1%	110-4.99k-1	R85	MF, 1k, 1/4W, 1%	110-1k-1
R22	MF, 1k, 1/4W, 1%	110-1k-1	R86	MF, 10k, 1/4W, 1%	110-10k-1
R23	MF, 2k, 1/4W, 1%	110-2k-1	R87	MF, 10k, 1/4W, 1%	110-10k-1
R24	Trimmer, 1k	158-2	R88	MF, 20k, 1/4W, 1%	110-20k-1
R25	MF, 3.32k, 1/4W, 1%	110-3.32k-1	R89	MF, 20k, 1/4W, 1%	110-20k-1
R26	MF, 1k, 1/4W, 1%	110-1k-1	R90	MF, 20k, 1/4W, 1%	110-20k-1
R27	MF, 1.15k, 1/4W, 1%	110-1.15k-1	R91	MF, 20k, 1/4W, 1%	110-20k-1
R28	MF, 7.5k, 1/4W, 1%	110-7.5k-1	R92	MF, 13k, 1/4W, 1%	110-13k-1
R29	MF, 10Ω, 1/4W, 1%	110-10-1	R93	MF, 1.5k, 1/4W, 1%	110-1.5k-1
R30	MF, 4.53k, 1/4W, 1%	110-4.53k-1	R94	MF, 38.3k, 1/4W, 1%	110-38.3k-1
R31	Trimmer, 1k	158-2	R95	MF, 2k, 1/4W, 1%	110-2k-1
R32	MF, 4.99k, 1/4W, 1%	110-4.99k-1	R96	MF, 215Ω, 1/4W, 1%	110-215-1
R33	MF, 2k, 1/4W, 1%	110-2k-1	R97	MF, 2k, 1/4W, 1%	110-2k-1
R34	Trimmer, 1k	158-2	R98	MF, 215Ω, 1/4W, 1%	110-215-1
R35	MF, 1k, 1/4W, 1%	110-1k-1	R99	MF, 59k, 1/4W, 1%	110-59k-1
R36	MF, 1.15k, 1/4W, 1%	110-1.15k-1	R100	MF, 1k, 1/4W, 1%	110-1k-1
R37	MF, 7.5k, 1/4W, 1%	110-7.5k-1	R101	MF, 49.9k, 1/4W, 1%	110-49.9k-1
R38	MF, 10Ω, 1/4W, 1%	110-10-1	R102	MF, 20k, 1/4W, 1%	110-20k-1
R39	MF, 4.99k, 1/4W, 1%	110-4.99k-1	R103	MF, 24.9k, 1/4W, 1%	110-24.9k-1
R40	Trimmer, 1k	158-2	R104	MF, 121k, 1/4W, 1%	110-121k-1
R41	MF, 4.99k, 1/4W, 1%	110-4.99k-1	R105	MF, 3.32k, 1/4W, 1%	110-3.32k-1
R42	MF, 2k, 1/4W, 1%	110-2k-1	R106	MF, 20k, 1/4W, 1%	110-20k-1
R43	Trimmer, 1k	158-2	R107	MF, 20k, 1/4W, 1%	110-20k-1
R44	MF, 10k, 1/4W, 1%	110-10k-1	R108	MF, 49.9k, 1/4W, 1%	110-49.9k-1
R45	MF, 11.5k, 1/4W, 1%	110-11.5k-1	R109	MF, 20k, 1/4W, 1%	110-20k-1
R46	Trimmer, 5k	158-4	R110	MF, 24.9k, 1/4W, 1%	110-24.9k-1
R47	MF, 10k, 1/4W, 1%	110-10k-1	R111	MF, 6.98k, 1/4W, 1%	110-6.98k-1
R48	MF, 10k, 1/4W, 1%	110-10k-1	R112	MF, 1k, 1/4W, 1%	110-1k-1
R49	MF, 232k, 1/4W, 1%	110-232k-1	R113	MF, 27.4k, 1/4W, 1%	110-27.4k-1
R50	Trimmer, 100k	158-6	R114	MF, 1k, 1/4W, 1%	110-1k-1
R51	MF, 10k, 1/4W, 1%	110-10k-1	R115	MF, 10k, 1/4W, 1%	110-10k-1
R52	MF, 10.2k, 1/4W, 1%	110-10.2k-1	R116	MF, 90.9k, 1/4W, 1%	110-90.9k-1
R53	MF, 21k, 1/4W, 1%	110-21k-1	R117	MF, 10k, 1/4W, 1%	110-10k-1
R54	MF, 54.9k, 1/4W, 1%	110-54.9k-1	R118	MF, 1k, 1/4W, 1%	110-1k-1
R55	MF, 124k, 1/4W, 1%	110-124k-1	R119	MF, 10k, 1/4W, 1%	110-10k-1
R56	MF, 332k, 1/4W, 1%	110-332k-1	R120	MF, 10k, 1/4W, 1%	110-10k-1
R57	MF, 499k, 1/4W, 1%	110-499k-1	R121	MF, 10k, 1/4W, 1%	110-10k-1
R58	MF, 10.2k, 1/4W, 1%	110-10.2k-1	R122	MF, 2.21k, 1/4W, 1%	110-2.21k-1
R59	MF, 21k, 1/4W, 1%	110-21k-1	R123	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R60	MF, 54.9k, 1/4W, 1%	110-54.9k-1	R124	MF, 10k, 1/4W, 1%	110-10k-1
R61	MF, 124k, 1/4W, 1%	110-124k-1	R125	MF, 10k, 1/4W, 1%	110-10k-1
R62	MF, 332k, 1/4W, 1%	110-332k-1	R126	MF, 100k, 1/4W, 0.1%	113-100k-0.1
R63	MF, 499k, 1/4W, 1%	110-499k-1	R127	MF, 50k, 1/4W, 0.1%	113-50k-0.1
R64	MF, 10k, 1/4W, 1%	110-10k-1	R128	MF, 2.1k, 1/4W, 1%	110-2.1k-1
R65	MF, 10k, 1/4W, 1%	110-10k-1	R129	MF, 150Ω, 1/4W, 1%	110-150-1
R66	MF, 22.1k, 1/4W, 1%	110-22.1k-1	R130	MF, 10k, 1/4W, 1%	110-10k-1
R67	MF, 22.1k, 1/4W, 1%	110-22.1k-1	R131	MF, 10k, 1/4W, 1%	110-10k-1
R68	MF, 20k, 1/4W, 0.1%	113-20k-0.1	R132	CC, 4.7M, 1/4W, 5%	101-4.7M-5
R69	MF, 20k, 1/4W, 1%	110-20k-1	R133	Trimmer, 50k	158-1
R70	MF, 20k, 1/4W, 0.1%	113-20k-0.1	R134	MF, 2.21k, 1/4W, 1%	110-2.21k-1
R71	MF, 26.1k, 1/4W, 1%	110-26.1k-1	R135	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R72	MF, 20k, 1/4W, 0.1%	113-20k-0.1	R136	MF, 180Ω, 1/8W, 5%	109-180-5
R73	MF, 20k, 1/4W, 1%	110-20k-1	R137	CC, 4.7M, 1/4W, 5%	101-4.7M-5
R74	MF, 20k, 1/4W, 0.1%	113-20k-0.1	R138	Trimmer, 50k	158-1
R75	MF, 26.1k, 1/4W, 1%	110-26.1k-1	R139	MF, 10k, 1/4W, 1%	110-10k-1
R76	MF, 4.99k, 1/4W, 1%	110-4.99k-1	R140	MF, 40.2k, 1/4W, 1%	110-40.2k-1
R77	Trimmer, 50k	158-1	R141	MF, 10k, 1/4W, 1%	110-10k-1
R78	MF, 46.4k, 1/4W, 1%	110-46.4k-1	R142	MF, 10k, 1/4W, 1%	110-10k-1

Table 6-4. Replaceable Electrical Parts, Digital (A2) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
R143	MF, 2.21k, 1/4W, 1%	110-2.21k-1
R144	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R145	MF, 3.16k, 1/4W, 1%	110-3.16k-1
R146	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R147	MF, 6.98k, 1/4W, 1%	110-6.98k-1
R148	MF, 100Ω, 1/4W, 1%	110-100-1
R149	MF, 3.32k, 1/4W, 1%	110-3.32k-1
R150	MF, 2k, 1/4W, 1%	110-2k-1
R151	MF, 3.32k, 1/4W, 1%	110-3.32k-1
R152	MF, 22.1k, 1/4W, 1%	110-22.1k-1
R153	MF, 2k, 1/4W, 1%	110-2k-1
R154	MF, 4.02k, 1/4W, 1%	110-4.02k-1
R155	MF, 10k, 1/4W, 1%	110-10k-1
R156	MF, 53.6k, 1/4W, 1%	110-53.6k-1
R157	Variable, 50k	158-1
R158	MF, 301k, 1/4W, 1%	110-301k-1
R159	CC, 2.2M, 1/4W, 5%	101-2.2M-5
R160	MF, 22.1k, 1/4W, 1%	110-22.1k-1
R161	MF, 3.32k, 1/4W, 1%	110-3.32k-1
R162	MF, 33.2k, 1/4W, 1%	110-33.2k-1
R163	MF, 33.2k, 1/4W, 1%	110-33.2k-1
R164	MF, 10k, 1/4W, 1%	110-10k-1
R165	MF, 100k, 1/4W, 1%	110-100k-1
R166	MF, 31.6k, 1/4W, 1%	110-31.6k-1
R167	MF, 100k, 1/4W, 1%	110-100k-1
R168	MF, 5.62k, 1/4W, 1%	110-5.62k-1
R169	MF, 215Ω, 1/4W, 1%	110-215-1
R170	MF, 5.62k, 1/4W, 1%	110-5.62k-1
R171	MF, 5.62k, 1/4W, 1%	110-5.62k-1
R172	MF, 10k, 1/4W, 1%	110-10k-1
R173	MF, 121k, 1/4W, 1%	110-121k-1
R174	MF, 1k, 1/4W, 1%	110-1k-1
R175	MF, 10k, 1/4W, 1%	110-10k-1
R176	MF, 22.1k, 1/4W, 1%	110-22.1k-1
R177	MF, 22.1k, 1/4W, 1%	110-22.1k-1
R178	MF, 215Ω, 1/4W, 1%	110-215-1
R179	MF, 5.62k, 1/4W, 1%	110-5.62k-1
R180	MF, 215Ω, 1/4W, 1%	110-215-1
R181	MF, 68.1k, 1/4W, 1%	110-68.1k-1
R182	MF, 68.1k, 1/4W, 1%	110-68.1k-1
R183	MF, 22.1k, 1/4W, 1%	110-22.1k-1
R184	MF, 22.1k, 1/4W, 1%	110-22.1k-1
R185	MF, 22.1k, 1/4W, 1%	110-22.1k-1
R186	MF, 215Ω, 1/4W, 1%	110-215-1
R187	MF, 215Ω, 1/4W, 1%	110-215-1
R188	MF, 10k, 1/4W, 1%	110-10k-1
R189	MF, 10k, 1/4W, 1%	110-10k-1
R190	MF, 215Ω, 1/4W, 1%	110-215-1
R191	MF, 215Ω, 1/4W, 1%	110-215-1
R192	MF, 215Ω, 1/4W, 1%	110-215-1
R193	MF, 10k, 1/4W, 1%	110-10k-1
R194	CC, 4.7M, 1/4W, 5%	101-4.7M-5
R195	Trimmer, 50k	158-1
R196	CC, 4.7M, 1/4W, 5%	101-4.7M-5
R197	Trimmer, 50k	158-1
R198	Not used	
R199	MF, 1k, 1/4W, 1%	110-1k-1
R200	MF, 1k, 1/4W, 1%	110-1k-1
R201	MF, 365Ω, 1/4W, 1%	110-365-1
R202	MF, 365Ω, 1/4W, 1%	110-365-1
R203	MF, 22.1k, 1/4W, 1%	110-22.1k-1
R204	MF, 100k, 1/4W, 1%	110-100k-1
R205	MF, 187Ω, 1/4W, 1%	110-187-1
R206	MF, 187Ω, 1/4W, 1%	110-187-1
R207	MF, 187Ω, 1/4W, 1%	110-187-1
R208	MF, 28.7k, 1/4W, 1%	110-28.7k-1
R209	MF, 75k, 1/4W, 1%	110-75k-1
R210	MF, 100k, 1/4W, 1%	110-100k-1
R211	CC, 22M, 1/4W, 5%	101-22M-5
R212	Trimmer, 50k	158-1
R213	MF, 100k, 1/4W, 1%	110-100k-1
R214	MF, 100k, 1/4W, 1%	110-100k-1
RP1	Resistor Pack, 22k	123-4
R215	MF, 1k, 1/4W, 1%	110-1k-1
R216	MF, 536k, 1/4W, 1%	110-536k-1
	SOCKETS	
J1	18-Pin, DIP	551-148
J2	16-Pin, DIP	553-69
J3	14-Pin, DIP, Right Angle	551-158
	TEST POINTS	
TP1 thru TP14	Test Points	706-44
	TRANSISTORS	
Q1	NPN, 2N3694	20-2N3694
Q2	PNP, 2N4249	20-2N4249
Q3	NPN, 2N3694	20-2N3694
Q4	PNP, 2N2907	20-2N2907
Q5	NPN, 2N3694	20-2N3694
Q6	NPN, 2N3694	20-2N3694
Q7	PNP, 2N4249	20-2N4249
Q8	NPN, 2N3694	20-2N3694
Q9	NPN, 2N3694	20-2N3694

Table 6-5. Replaceable Electrical Parts, Log Amplifier (A3) PCB

A3	**Log Amplifier PC Board Assembly**	**560A-D-11348-3**
A10	Input Module Assembly	560A-B-11351
	CAPACITORS	
C1	Disc, 0.1μF, 50V	230-37
C2	Disc, 0.1μF, 50V	230-37
C3	Mylar, .047μF, 100V	210-28
C4	Disc, .01μF, 100V	230-11
C5	Mylar, 0.1μF, 100V	210-30
C6	Disc, 0.1μF, 50V	230-37
C7	Disc, 0.1μF, 50V	230-37
C8	Tantalum, 6.8μF, 50V	250-114
C9	Disc, .01μF, 50V (low tc)	230-39
C10	Disc, .01μF, 100V	230-11
C11	Disc, .001μF, 50V	230-30
C12	Disc, .01μF, 100V	230-11
C13	Disc, 0.1μF, 50V	230-37
C14	Disc, 0.1μF, 50V	230-37
C15	Tantalum, 6.8μF, 50V	250-114
C16	Disc, .01μF, 50V (low tc)	230-39
C17	Mylar, .047μF, 100V	210-28

Table 6-5. Replaceable Electrical Parts, Log Amplifier (A3) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
C18	Disc, .01µF, 100V	230-11
C19	Mylar, 0.1µF, 100V	210-30
C20	Disc, 0.1µF, 50V	230-37
C21	Disc, 0.1µF, 50V	230-37
C22	Tantalum, 10µF, 25V	250-42A
C23	Disc, .01µF, 100V	230-11
C24	Disc, .002µF	230-33
C25	Disc, .002µF	230-33
C26	Disc, .05µF, 25V	230-35
C27	Disc, .05µF, 25V	230-35
C28	Mica, 820pF	220-820
C29	Tantalum, 10µF, 25V	250-42A
C30	Tantalum, 10µF, 25V	250-42A
C31	Tantalum, 10µF, 25V	250-42A
C32	Disc, .02µF, 25V	230-20
C33	Mylar, 5µF, 50V	210-53
C34	Mylar, 5µF, 50V	210-53
C35	Tantalum, 10µF, 25V	250-42A
C36	Tantalum, 10µF, 25V	250-42A
C37	Mylar, 0.1µF, 100V	210-30
C38	Disc, 0.1µF, 50V	230-37
C39	Disc, 0.1µF, 50V	230-37
C40	Mica, 15pF	220-15
C41	Mica, 15pF	220-15
C42	Mica, 15pF	220-15
C43	Tantalum, 10µF, 25V	250-42A
C44	Mica, 10pF	220-10
C45	Mylar, 0.1µF, 100V	210-30
C46	Mica, 10pF	220-10
C47	Disc, 0.1µF, 50V	230-37
C48	Disc, 0.1µF, 50V	230-37
C49	Disc, 0.1µF, 50V	230-37
C50	Disc, 0.1µF, 50V	230-37
C51	Tantalum, 10µF, 25V	250-42A
C52	Tantalum, 68µF, 6V	250-58A
C53	Disc, .01µF, 100V	230-11
C54	Disc, 0.1µF, 50V	230-37
C55	Mylar, .047µF, 100V	210-28
C56	Disc, 0.1µF, 50V	230-37
C57	Tantalum, 10µF, 25V	250-42A
C58	Disc, .02µF, 25V	230-20
C59	Disc, 0.1µF, 50V	230-37
C60	Tantalum, 10µF, 25V	250-42A
C61	Mylar, .1µF, 100V	210-30
C62	Mica, 10pF	220-10
C63	Mica, 10pF	220-10
C64	Tantalum, 10µF, 25V	250-42A
C65	Disc, 0.1µF, 50V	230-37
C66	Disc, 0.1µF, 50V	230-37
C67	Disc, 0.1µF, 50V	230-37
C68	Disc, 0.1µF, 50V	230-37
C69	Disc, 0.1µF, 50V	230-37
C70	Disc, 0.1µF, 50V	230-37
C71	Mica, 15pF	220-15
C72	Mica, 22pF	220-22
C73	Tantalum, 10µF, 25V	250-42A
C74	Mica, 15pF	220-15
C75	Mica, 22pF	220-22
C76	Not used	
C77	Not used	
C78	Disc, .001µF, 50V	230-30
C79	Mica, 3pF	223-3
C80	Mica, 3pF	223-3
C81	Mica, 330pF	220-330
C82	Disc, .0047µF, 100V	230-36
C83	Disc, 2700pF, 100V	230-34
C84	Mica, 330pF	220-330
C85	Disc, 2700pF, 100V	230-34
C86	Disc, 0.1µF, 50V	230-37
C87	Mylar, 0.1µF, 100V	210-30
C88	Mica, 270pF	223-270
C89	Disc, 2700pF, 100V	230-34
C90	Disc, 2700pF, 100V	230-34
C91	Disc, 2700pF, 100V	230-34
C94	Disc, .1µF, 50V	230-37
	DIODES	
CR1	Zener, 3.3V, 1W, 5%	10-14
CR2	Zener, 3.3V, 1W, 5%	10-14
CR3	Silicon, 1N4446	10-1N4446
CR4	Silicon, 1N4446	10-1N4446
CR5	Silicon, 1N4446	10-1N4446
CR6	Silicon, 1N4446	10-1N4446
CR7	Silicon, 1N4446	10-1N4446
CR8	Silicon, 1N4446	10-1N4446
CR9	Silicon, 1N4446	10-1N4446
CR10	Silicon, 1N4446	10-1N4446
CR11	Zener, 5.1V, 0.4W, 5%	10-1N751A
CR12	Zener, 5.1V, 0.4W, 5%	10-1N751A
CR13	Silicon, 1N4446	10-1N4446
CR14	Silicon, 1N4446	10-1N4446
CR15	Silicon, 1N4446	10-1N4446
CR16	Silicon, 1N4446	10-1N4446
CR17	Zener, 3.3V, 1W, 5%	10-14
CR18	Zener, 3.3V, 1W, 5%	10-14
CR19	Silicon, 1N4446	10-1N4446
CR20	Silicon, 1N4446	10-1N4446
CR21	Silicon, 1N4446	10-1N4446
CR22	Silicon, 1N4446	10-1N4446
CR23	Zener, 10V, 0.4W, 5%	10-1N758A
CR24	Silicon, 1N4446	10-1N4446
CR25	Silicon, 1N4446	10-1N4446
CR26	Silicon, 1N4446	10-1N4446
CR27	Zener, 11V, 0.4W, 5%	10-1N962B
CR28	Silicon, 1N4446	10-1N4446
CR29	Silicon, 1N4446	10-1N4446
CR30	Silicon, 1N4446	10-1N4446
CR31	Zener, 11V, 0.4W, 5%	10-1N962B
CR32	Zener, 12V, 0.4W, 5%	10-1N759A
CR33	Zener, 12V, 0.4W, 5%	10-1N759A
CR34	Zener, 5.1V, 0.4W, 5%	10-1N751A
CR35	Zener, 10V, 0.4W, 5%	10-1N758A
CR36	Zener, 10V, 0.4W, 5%	10-1N758A
CR37	Zener, 10V, 0.4W, 5%	10-1N758A
CR38	Zener, 10V, 0.4W, 5%	10-1N758A
CR39	Zener, 5.1V, 0.4W, 5%	10-1N751A
CR40	Zener, 5.1V, 0.4W, 5%	10-1N751A
CR41	Zener, 10V, 0.4W, 5%	10-1N758A
CR42	Silicon, 1N4446	10-1N4446
CR43	Silicon, 1N4446	10-1N4446
CR44	Reference, 6.2V	10-1N823
CR45	Zener, 10V, 0.4W, 5%	10-1N758A
CR46	Silicon, 1N4446	10-1N4446
CR47	Silicon, 1N4446	10-1N4446
CR48	Silicon, 1N4446	10-1N4446
CR49	Zener, 11V, 0.4W, 5%	10-1N962B
CR50	Zener, 10V, 0.4W, 5%	10-1N758A
CR51	Silicon, 1N4446	10-1N4446

Table 6-5. Replaceable Electrical Parts, Log Amplifier (A3) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
CR52	Silicon, 1N4446	10-1N4446
CR53	Zener, 3.3V, 1W, 5%	10-14
CR54	Zener, 3.3V, 1W, 5%	10-14
CR55	Zener, 5.1V, 0.4W, 5%	10-1N751A
CR56	Zener, 5.1V, 0.4W, 5%	10-1N751A
CR57	Reference, 6.2V	10-1N823
CR58	Silicon, 1N4446	10-1N4446
CR59	Silicon, 1N4446	10-1N4446
CR60	Silicon, 1N4446	10-1N4446
CR61	Silicon, 1N4446	10-1N4446
CR62	Silicon, 1N4446	10-1N4446
CR63	Silicon, 1N4446	10-1N4446
CR64	Silicon, 1N4446	10-1N4446
CR65	Silicon, 1N4446	10-1N4446
CR66	Silicon, 1N4446	10-1N4446
CR67	Silicon, 1N4446	10-1N4446
CR68	Silicon, 1N4446	10-1N4446
CR69 thru CR79	Silicon, 1N4446	10-1N4446
	INTEGRATED CIRCUITS	
U1	Quad Op. Amp. (TL074CN)	54-132
U2	+15V Regulator (UA78M15HC)	50-3
U3	-15V Regulator (UA79M15HC)	50-4
U4	Op. Amp. (LF356H)	50-2
U5	Quad Comparator (MC3302P)	54-MC3302P
U6	Quad Analog Switch (LF13201N)	54-20
U7	Quad Comparator (MC3302P)	54-MC3302P
U8	Quad Op. Amp. (TL074CN)	54-132
U9	+15V Regulator (UA78M15HC)	50-3
U10	-15V Regulator (UA79M15HC)	50-4
U11	Not used	
U12	Op. Amp. (OP 05EJ)	54-87
U13	Quad Analog Switch (DG201CJ)	54-24
U14	Dual Op. Amp. (TL072CP)	54-53
U15	Op. Amp. (LF356H)	50-2
U16	+15V Regulator (MC7815CP)	54-21
U17	-15V Regulator (MC7915CP)	54-MC7915CP
U18	Op. Amp. (NE5534FE)	50-20
U19	Quad Analog Switch (DG201CJ)	54-24
U20	Low Current Op. Amp. (LH0042CH)	50-23
U21	Low Current Op. Amp. (LH0042CH)	50-23
U22	Op. Amp. (CA3054N)	54-77**
U23	Op. Amp. (CA3054N)	54-77**
U24	Op. Amp. (CA3054N)	54-77**
U25	Op. Amp. (CA3054N)	54-77**
U26	Op. Amp. (CA3054N)	54-77**
U27	Op. Amp. (CA3054N)	54-77**
U28	Op. Amp. (LF356H)	50-2
U29	Optical Isolator (FCD820)	20-820
U30	Quad 2-Input NOR (74C02N)	54-33
U31	Quad 2-Input NOR (74C02N)	54-33
U32	Optical Isolator (FCD820)	20-820
U33	Optical Isolator (FCD820)	20-820
U34	Triple 3-Input NAND (74C10N)	54-64
U35	Optical Isolator (FCD820)	20-820
U36	Optical Isolator (FCD820)	20-820
U37	Triple 3-Input NAND (74C10N)	54-64
U38	Quad Op. Amp. (TL074CN)	54-132
U39	Quad Op. Amp. (TI.074CN)	54-132
U40	Op. Amp. (OP05EJ)	54-87
U41	Op. Amp. (LF356H)	50-2
U42	+15V Regulator (MC7815CP)	54-21
U43	-15V Regulator (MC7915CP)	54-MC7915CP
U44	Op. Amp. (NE5534FE)	50-20
U45	Op. Amp. (CA3054N)	54-77**
U46	Op. Amp. (CA3054N)	54-77**
U47	Op. Amp. (CA3054N)	54-77**
U48	Op. Amp. (CA3054N)	54-77**
U49	Quad Op. Amp. (TL074CN)	54-132
U50	Op. Amp. (LF356H)	50-2
U51	Quad Op. Amp. (TL074CN)	54-132
U52	Quad Exclusive OR (74C86N)	54-69
--	Heat Clip for U18, U44	553-2
--	Insulator Pad	553-25
	**These IC's are not field-replaceable.	
	PLUGS	
P1	Plug, 5-Pin	551-151
	RESISTORS	
R1	MF, 1M, 1/4W, 1%	110-1M-1A
R2	MF, 10k, 1/4W, 1%	110-10k-1
R3	MF, 1M, 1/4W, 1%	110-1M-1A
R4	MF, 1M, 1/4W, 1%	110-1M-1A
R5	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R6	MF, 10k, 1/4W, 1%	110-10k-1
R7	MF, 5.11k, 1/4W, 1%	110-5.11k-1
R8	MF, 14.7Ω, 1/4W, 1%	110-14.7-1
R9	MF, 475Ω, 1/4W, 1%	110-475-1
R10	MF, 1M, 1/4W, 1%	110-1M-1A
R11	MF, 7.32k, 1/4W, 1%	110-7.32k-1
R12	Trimmer, 100k	156-100k
R13	MF, 14.7Ω, 1/4W, 1%	110-14.7-1
R14	MF, 1M, 1/4W, 1%	110-1M-1A
R15	MF, 953k, 1/4W, 1%	110-953k-1
R16	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R17	Not used	
R18	Trimmer, 100k	158-6
R19	MF, 10k, 1/4W, 1%	110-10k-1
R20	Not used	
R21	Not used	
R22	MF, 21.5k, 1/4W, 1%	110-21.5k-1
R23	MF, 10k, 1/4W, 1%	110-10k-1
R24	Not used	
R25	MF, 21.5k, 1/4W, 1%	110-21.5k-1
R26	Not used	
R27	Trimmer, 100k	158-6
R28	Not used	
R29	MF, 14.7Ω, 1/4W, 1%	110-14.7-1
R30	MF, 1M, 1/4W, 1%	110-1M-1A
R31	MF, 953k, 1/4W, 1%	110-953k-1
R32	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R33	MF, 475Ω, 1/4W, 1%	110-475-1
R34	MF, 14.7Ω, 1/4W, 1%	110-14.7-1
R35	MF, 1M, 1/4W, 1%	110-1M-1A
R36	MF, 7.32k, 1/4W, 1%	110-7.32k-1
R37	Trimmer, 100k	156-100k
R38	MF, 5.11k, 1/4W, 1%	110-5.11k-1
R39	MF, 10k, 1/4W, 1%	110-10k-1
R40	MF, 1M, 1/4W, 1%	110-1M-1A
R41	MF, 10k, 1/4W, 1%	110-10k-1

Table 6-5. Replaceable Electrical Parts, Log Amplifier (A3) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
R42	MF, 1M, 1/4W, 1%	110-1M-1A
R43	MF, 1M, 1/4W, 1%	110-1M-1A
R44	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R45	MF, 14.7Ω, 1/4W, 1%	110-14.7-1
R46	MF, 1k, 1/4W, 1%	110-1k-1
R47	MF, 1k, 1/4W, 1%	110-1k-1
R48	MF, 20k, 1/4W, 1%	110-20k-1
R49	MF, 10k, 1/4W, 1%	110-10k-1
R50	MF, 10k, 1/4W, 1%	110-10k-1
R51	Not used	
R52	Not used	
R53	MF, 5.76k, 1/4W, 1%	110-5.76k-1
R54	MF, 287k, 1/4W, 1%	110-287k-1
R55	MF, 3.74k, 1/4W, 1%	110-3.74k-1
R56	MF, 499k, 1/4W, 1%	110-499k-1
R57	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R58	MF, 158k, 1/4W, 1%	110-158k-1
R59	Not used	
R60	MF, 511Ω, 1/4W, 1%	110-511-1
R61	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R62	MF, 1k, 1/4W, 1%	110-1k-1
R63	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R64	MF, 1k, 1/4W, 1%	110-1k-1
R65	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R66	MF, 1k, 1/4W, 1%	110-1k-1
R67	MF, 1k, 1/4W, 1%	110-1k-1
R68	Trimmer, 100k	157-100kA
R69	MF, 1k, 1/4W, 1%	110-1k-1
R70	MF, 10k, 1/4W, 1%	110-10k-1
R71	CC, 2.2M, 1/4W, 5%	101-2.2M-5
R72	MF, 51.1Ω, 1/4W, 1%	110-51.1-1
R73	MF, 2.21k, 1/4W, 1%	110-2.21k-1
R74	MF, 51.1Ω, 1/4W, 1%	110-51.1-1
R75	MF, 1k, 1/4W, 1%	110-1k-1
R76	MF, 10k, 1/4W, 1%	110-10k-1
R77	CC, 2.2M, 1/4W, 5%	101-2.2M-5
R78	MF, 3.01k, 1/4W, 1%	110-3.01k-1
R79	MF, 68.1k, 1/4W, 1%	110-68.1k-1
R80	MF, 12.1k, 1/4W, 1%	110-12.1k-1
R81	MF, 7.87k, 1/4W, 1%	110-7.87k-1
R82	MF, 6.65k, 1/4W, 1%	110-6.65k-1
R83	MF, 5.76k, 1/4W, 1%	110-5.76k-1
R84	MF, 2.15k, 1/4W, 1%	110-2.15k-1
R85	MF, 8.87k, 1/4W, 1%	110-8.87k-1
R86	MF, 4.32k, 1/4W, 1%	110-4.32k-1
R87	MF, 2.10k, 1/4W, 1%	110-2.10k-1
R88	MF, 15.8k, 1/4W, 1%	110-15.8k-1
R89	MF, 5.9k, 1/4W, 1%	110-5.9k-1
R90	MF, 2.10k, 1/4W, 1%	110-2.10k-1
R91	MF, 124Ω, 1/4W, 1%	110-124-1
R92	MF, 124Ω, 1/4W, 1%	110-124-1
R93	MF, 124Ω, 1/4W, 1%	110-124-1
R94	MF, 124Ω, 1/4W, 1%	110-124-1
R95	MF, 261Ω, 1/4W, 1%	110-261-1
R96	MF, 249Ω, 1/4W, 1%	110-249-1
R97	MF, 549Ω, 1/4W, 1%	110-549-1
R98	MF, 499Ω, 1/4W, 1%	110-499-1
R99	MF, 1.27k, 1/4W, 1%	110-1.27k-1
R100	MF, 1k, 1/4W, 1%	110-1k-1
R101	MF, 1.62k, 1/4W, 1%	110-1.62k-1
R102	MF, 1k, 1/4W, 1%	110-1k-1
R103	MF, 249Ω, 1/4W, 1%	110-249-1
R104	MF, 243Ω, 1/4W, 1%	110-243-1
R105	MF, 562Ω, 1/4W, 1%	110-562-1
R106	MF, 499Ω, 1/4W, 1%	110-499-1
R107	MF, 1.96k, 1/4W, 1%	110-1.96k-1
R108	MF, 1k, 1/4W, 1%	110-1k-1
R109	MF, 249Ω, 1/4W, 1%	110-249-1
R110	MF, 249Ω, 1/4W, 1%	110-249-1
R111	MF, 549Ω, 1/4W, 1%	110-549-1
R112	MF, 499Ω, 1/4W, 1%	110-499-1
R113	MF, 1.96k, 1/4W, 1%	110-1.96k-1
R114	MF, 1k, 1/4W, 1%	110-1k-1
R115	MF, 2.21k, 1/4W, 1%	110-2.21k-1
R116	MF, 5.11k, 1/4W, 1%	110-5.11k-1
R117	MF, 6.81k, 1/4W, 1%	110-6.81k-1
R118	MF, 8.06k, 1/4W, 1%	110-8.06k-1
R119	MF, 11.8k, 1/4W, 1%	110-11.8k-1
R120	MF, 8.25k, 1/4W, 1%	110-8.25k-1
R121	MF, 8.06k, 1/4W, 1%	110-8.06k-1
R122	MF, 7.32k, 1/4W, 1%	110-7.32k-1
R123	MF, 7.68k, 1/4W, 1%	110-7.68k-1
R124	MF, 6.81k, 1/4W, 1%	110-6.81k-1
R125	MF, 6.19k, 1/4W, 1%	110-6.19k-1
R126	MF, 20k, 1/4W, 1%	110-20k-1
R127	Trimmer, 500Ω	158-3
R128	Trimmer, 1k	158-2
R129	Trimmer, 5k	158-4
R130	Trimmer, 5k	158-4
R131	Trimmer, 5k	158-4
R132	Trimmer, 5k	158-4
R133	Trimmer, 2k	158-10
R134	Trimmer, 2k	158-10
R135	Trimmer, 2k	158-10
R136	Trimmer, 2k	158-10
R137	MF, 625Ω, 1/4W, 0.1%	113-625-0.1
R138	MF, 625Ω, 1/4W, 0.1%	113-625-0.1
R139	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R140	MF, 20k, 1/4W, 0.1%	113-30k-0.1
R141	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R142	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R143	MF, 499Ω, 1/4W, 1%	110-499-1
R144	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R145	MF, 499Ω, 1/4W, 1%	110-499-1
R146	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R147	MF, 499Ω, 1/4W, 1%	110-499-1
R148	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R149	MF, 499Ω, 1/4W, 1%	110-499-1
R150	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R151	MF, 499Ω, 1/4W, 1%	110-499-1
R152	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R153	MF, 4k, 1/4W, 0.1%	113-4k-0.1
R154	Trimmer, 1k	157-1kA
R155	MF, 6.19k, 1/4W, 1%	110-6.19k-1
R156	MF, 10k, 1/4W, 1%	110-10k-1
R157	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R158	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R159	MF, 10k, 1/4W, 1%	110-10k-1
R160	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R161	MF, 2.49k, 1/4W, 1%	110-2.49k-1
R162	MF, 825k, 1/4W, 1%	110-825k-1
R163	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R164	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R165	MF, 4k, 1/4W, 0.1%	113-4k-0.1
R166	MF, 147k, 1/4W, 1%	110-147k-1
R167	CC, 360k, 1/4W, 5%	101-360k-5
R168	MF, 10k, 1/4W, 1%	110-10k-1
R169	MF, 10k, 1/4W, 0.1%	113-10k-0.1

Table 6-5. Replaceable Electrical Parts, Log Amplifier (A3) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
R170	MF, 10k, 1/4W, 1%	110-10k-1
R171	MF, 10k, 1/4W, 1%	110-10k-1
R172	MF, 10k, 1/4W, 1%	110-10k-1
R173	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R174	MF, 10k, 1/4W, 1%	110-10k-1
R175	MF, 10k, 1/4W, 1%	110-10k-1
R176	MF, 10k, 1/4W, 1%	110-10k-1
R177	MF, 56.2k, 1/4W, 1%	110-56.2k-1
R178	MF, 715k, 1/4W, 1%	110-715k-1
R179	MF, 651k, 1/4W, 1%	110-651k-1
R180	MF, 8.25k, 1/4W, 1%	110-8.25k-1
R181	Trimmer, 1k	157-1kA
R182	Trimmer, 1k	157-1kA
R183	MF, 6.81k, 1/4W, 1%	110-6.81k-1
R184	NOT USED	
R185	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R186	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R187	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R188	MF, 976Ω, 1/4W, 1%	110-976-1
R189	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R190	Trimmer, 20k	157-20kA
R191	MF, 1.47k, 1/4W, 1%	110-1.47k-1
R192	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R193	MF, 1k, 1/4W, 1%	110-1k-1
R194	Trimmer, 20k	157-20kA
R195	MF, 10k, 1/4W, 1%	110-10k-1
R196	MF, 1k, 1/4W, 1%	110-1k-1
R197	MF, 20k, 1/4W, 1%	110-20k-1
R198	MF, 1.47k 1/4W, 1%	110-1.47k-1
R199	MF, 1M, 1/4W, 1%	110-1M-1A
R200	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R201	MF, 42.2k, 1/4W, 1%	110-42.2k-1
R202	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R203	MF, 1k, 1/4W, 1%	110-1k-1
R204	MF, 5.76k, 1/4W, 1%	110-5.76k-1
R205	MF, 287k, 1/4W, 1%	110-287k-1
R206	MF, 1k, 1/4W, 1%	110-1k-1
R207	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R208	MF, 5.11k, 1/4W, 1%	110-5.11k-1
R209	Trimmer, 100k	157-100kA
R210	MF, 22.1k, 1/4W, 1%	110-22.1k-1
R211	MF, 51.1Ω, 1/4W, 1%	110-51.1-1
R212	MF, 1.96k, 1/4W, 1%	110-1.96k-1
R213	MF, 51.1Ω, 1/4W, 1%	110-51.1-1
R214	MF, 68.1k, 1/4W, 1%	110-68.1k-1
R215	MF, 12.1k, 1/4W, 1%	110-12.1k-1
R216	MF, 7.87k, 1/4W, 1%	110-7.87k-1
R217	MF, 6.65k, 1/4W, 1%	110-6.65k-1
R218	MF, 5.76k, 1/4W, 1%	110-5.76k-1
R219	MF, 2.15k, 1/4W, 1%	110-2.15k-1
R220	MF, 8.87k, 1/4W, 1%	110-8.87k-1
R221	MF, 4.32k, 1/4W, 1%	110-4.32k-1
R222	MF, 900Ω, 1/4W, 0.1%	113-900-0.1
R223	MF, 900Ω, 1/4W, 0.1%	113-900-0.1
R224	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R225	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R226	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R227	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R228	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R229	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R230	Trimmer, 1k	158-2
R231	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R232	MF, 20k, 1/4W, 0.1%	113-20k-0.1
R233	MF, 1k, 1/4W, 1%	110-1k-1
R234	MF, 2.49k, 1/4W, 1%	110-2.49k-1
R235	MF, 953k, 1/4W, 1%	110-953k-1
R236	MF, 124Ω, 1/4W, 1%	110-124-1
R237	MF, 124Ω, 1/4W, 1%	110-124-1
R238	MF, 124Ω, 1/4W, 1%	110-124-1
R239	MF, 124Ω, 1/4W, 1%	110-124-1
R240	MF, 261Ω, 1/4W, 1%	110-261-1
R241	MF, 249Ω, 1/4W, 1%	110-249-1
R242	MF, 549Ω, 1/4W, 1%	110-549-1
R243	MF, 499Ω, 1/4W, 1%	110-499-1
R244	MF, 1.27k, 1/4W, 1%	110-1.27k-1
R245	MF, 1k, 1/4W, 1%	110-1k-1
R246	MF, 1.62k, 1/4W, 1%	110-1.62k-1
R247	MF, 1k, 1/4W, 1%	110-1k-1
R248	MF, 249Ω, 1/4W, 1%	110-249-1
R249	MF, 243Ω, 1/4W, 1%	110-243-1
R250	MF, 562Ω, 1/4W, 1%	110-562-1
R251	MF, 499Ω, 1/4W, 1%	110-499-1
R252	MF, 9.31k, 1/4W, 1%	110-9.31k-1
R253	MF, 10k, 1/4W, 1%	110-10k-1
R254	MF, 953k, 1/4W, 1%	110-953k-1
R255	Trimmer, 100k	158-6
R256	MF, 1k, 1/4W, 1%	110-1k-1
R257	MF, 14k, 1/4W, 1%	110-14k-1
R258	MF, 825k, 1/4W, 1%	110-825k-1
R259	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R260	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R261	MF, 1.96k, 1/4W, 1%	110-1.96k-1
R262	MF, 5.11k, 1/4W, 1%	110-5.11k-1
R263	MF, 6.81k, 1/4W, 1%	110-6.81k-1
R264	MF, 8.06k, 1/4W, 1%	110-8.06k-1
R265	MF, 11.8k, 1/4W, 1%	110-11.8k-1
R266	MF, 8.25k, 1/4W, 1%	110-8.25k-1
R267	MF, 7.15k, 1/4W, 1%	110-7.15k-1
R268	MF, 5.62k, 1/4W, 1%	110-5.62k-1
R269	MF, 651k, 1/4W, 1%	110-651k-1
R270	Trimmer, 500Ω	158-3
R271	Trimmer, 1k	158-2
R272	Trimmer, 5k	158-4
R273	Trimmer, 5k	158-4
R274	Trimmer, 5k	158-4
R275	Trimmer, 5k	158-4
R276	Trimmer, 5k	158-4
R277	Trimmer, 2k	158-10
R278	MF, 1M, 1/4W, 1%	110-1M-1A
R279	MF, 1M, 1/4W, 1%	110-1M-1A
R280	MF, 1M, 1/4W, 1%	110-1M-1A
R281	MF, 10k, 1/4W, 1%	110-10k-1
R282	MF, 10k, 1/4W, 1%	110-10k-1
R283	MF, 1M, 1/4W, 1%	110-1M-1A
R284	Trimmer, 1k	157-1kA
R285	MF, 10k, 1/4W, 1%	110-10k-1
R286	MF, 10k, 1/4W, 1%	110-10k-1
R287	MF, 7.15k, 1/4W, 1%	110-7.15k-1
R288	NOT USED	
R289	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R290	MF, 10k, 1/4W, 0.1%	113-10k-0.1
R291	MF, 56.2k, 1/4W, 1%	110-56.2k-1
R292	MF, 1M, 1/4W, 1%	110-1M-1A
R293	MF, 10k, 1/4W, 1%	110-10k-1
R294	Trimmer, 2k	157-2kA
R295	MF, 100k, 1/4W, 1%	110-100k-1
R296	MF, 147k, 1/4W, 1%	110-147k-1
R297	MF, 147k, 1/4W, 1%	110-147k-1
R298	MF, 100Ω, 1/4W, 1%	110-100-1
R299	MF, 100k, 1/4W, 1%	110-100k-1

Table 6-5. Replaceable Electrical Parts, Log Amplifier (A3) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
R300	MF, 34.8k, 1/4W, 1%	110-34.8k-1
R301	Trimmer, 20k	158-5
R302	MF, 54.9k, 1/4W, 1%	110-54.9k-1
R303	MF, 10k, 1/4W, 1%	110-10k-1
R304	Trimmer, 20k	158-5
R305	MF, 10k, 1/4W, 1%	110-10k-1
R306	MF, 97.6k, 1/4W, 1%	110-97.6k-1
R307	MF, 10k, 1/4W, 1%	110-10k-1
R308	NOT USED	
R309	MF, 10Ω, 1/4W, 1%	110-10-1
R310	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R311	MF, 1M, 1/4W, 1%	110-1M-1A
R312	Trimmer, 100k	158-6
R313	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R314	MF, 1M, 1/4W, 1%	110-1M-1A
R315	Trimmer, 100k	158-6
R316	MF, 10Ω, 1/4W, 1%	110-10-1
R317	MF, 15k, 1/4W, 1%	110-15k-1
R318	MF, 15k, 1/4W, 1%	110-15k-1
R319	MF, 15k, 1/4W, 1%	110-15k-1
R320	MF, 15k, 1/4W, 1%	110-15k-1
R321	MF, 15k, 1/4W, 1%	110-15k-1
R322	MF, 15k, 1/4W, 1%	110-15k-1
R323	MF, 15k, 1/4W, 1%	110-15k-1
R324	MF, 15k, 1/4W, 1%	110-15k-1
R325	MF, 10k, 1/4W, 1%	110-10k-1
R326	MF, 10k, 1/4W, 1%	110-10k-1
R327	MF, 48.7k, 1/4W, 1%	110-48.7k-1
R328	MF, 4.99k, 1/4W, 1%	110-4.99k-1
R329	MF, 100k, 1/4W, 1%	110-100k-1
R330	MF, 100k, 1/4W, 1%	110-100k-1
R331	MF, 100k, 1/4W, 1%	110-100k-1
R332	MF, 316k, 1/4W, 1%	110-316k-1
R333	MF, 36.5k, 1/4W, 1%	110-36.5k-1
R334	MF, 14.7k, 1/4W, 1%	110-14.7k-1
R335	MF, 24.9k, 1/4W, 1%	110-24.9k-1
R336	MF, 10k, 1/4W, 1%	110-10k-1
R337	MF, 10k, 1/4W, 1%	110-10k-1
R338	MF, 316k, 1/4W, 1%	110-316k-1
RP1	Resistor Pack, 1k	123-1
RP2	Resistor Pack, 1k	123-1
RP3	Resistor Pack, 1k	123-1
	SOCKETS	
J1	16-Pin DIP	553-69
J2	16-Pin SIP (cut to 16 pin)	551-173
J3	16-Pin SIP (cut to 16 pin)	551-173
	SWITCHES	
S1	Slide, DPDT	420-14
	TEST POINTS	
TP1 thru TP24	Test Points	706-44
	TRANSISTORS	
Q1	PNP, 2N4249	20-2N4249
Q2	NPN, 2N3694	20-2N3694
Q3	NPN, 2N3694	20-2N3694
Q4	PNP, 2N4249	20-2N4249
Q5	PNP, 2N4249	20-2N4249
Q6	NPN, 2N3694	20-2N3694
Q7	NPN, 2N3694	20-2N3694
Q8	NPN, 2N3694	20-2N3694
Q9	NPN, 2N3694	20-2N3694

Table 6-6. Replaceable Electrical Parts, Power Supply (A4) PCB

REF DES.	DESCRIPTION	WILTRON PART NO.
A4	**Power Supply PC Board Assembly**	**560A-C-7004-3**
	CAPACITORS	
C1	Monolithic, 0.1µF, 50V	230-37
C2	Monolithic, 0.1µF, 50V	230-37
C3	Electrolytic, 21000µF, 15V	250-79
C4	Monolithic, 0.1µF, 50V	230-37
C5	Monolithic, 0.1µF, 50V	230-37
C6	Electrolytic, 47µF, 63V	250-51
C7	Tantalum, 6.8µF, 35V	250-41A
C8	Monolithic, .01µF, 100V	230-11
C9	Monolithic, .01µF, 100V	230-11
C10	Electrolytic, 1000µF, 63V	250-18
C11	Tantalum, 6.8µF, 35V	250-41A
C12	Tantalum, 6.8µF, 35V	250-41A
C13	Tantalum, 6.8µF, 35V	250-41A
C14	Electrolytic, 1000µF, 63V	250-18
C15	Tantalum, 6.8µF, 35V	250-41A
C16	Tantalum, 6.8µF, 35V	250-41A
C17	Tantalum, 6.8µF, 35V	250-41A
C18	Tantalum, 6.8µF, 35V	250-41A
C19	Tantalum, 6.8µF, 35V	250-41A
	CONNECTORS	
J1	7-Pin	551-118
J2	3-Pin	551-50
J3	11-Pin	551-86
	DIODES	
CR1	Silicon Rectifier, 6A	10-12
CR2	Silicon Rectifier, 6A	10-12
CR3	Silicon Rectifier, 6A	10-12
CR4	Silicon Rectifier, 6A	10-12
CR5	Silicon Rectifier	10-SI2
CR6	Silicon Rectifier	10-SI2
CR7	Bridge, 2A	10-13
CR8	Bridge, 2A	10-13
CR9	Zener, 12V	10-17
CR10	Zener, 12V	10-17
CR11	Zener, 12V	10-17
CR12	Zener, 12V	10-17
CR13	Silicon Rectifier	10-SI2
CR14	Silicon Rectifier	10-SI2
CR15	Silicon Rectifier	10-SI2
	INTEGRATED CIRCUITS	
VR1	Voltage Regulator, -18V	54-63
VR2	Voltage Regulator, +18V	54-62
	RESISTORS	
R1	MF, 1k, 1/4W, 1%	110-1k-1
R2	CC, 750Ω, 1W, 5%	103-750-5
R3	MF, 100Ω, 1/4W, 1%	110-100-1
R4	CC, 1Ω, 1/2W, 5%	102-1-5
R5	CC, 750Ω, 1W, 5%	103-750-5
R6	CC, 1Ω, 1/2W, 5%	102-1-5
R7	MF, 100Ω, 1/4W, 1%	110-100-1
R8	MF, 23.7Ω, 1/4W, 1%	110-23.7-1
	TRANSISTORS	
Q1	NPN, 2N2218	20-2N2218
Q2	PNP, 2N2905	20-2N2905
Q3	NPN, Darlington	20-TIP112
Q4	PNP, Darlington (TIP117)	20-5
	MISCELLANEOUS	
—	**Fan Assembly**	**560-A-14250**

Table 6-7. Replaceable Electrical and Mechanical Parts, 5V Regulator Assembly

--	Front Panel	560A-A-7048-1
--	Resistor, CC, 1Ω, 1/2W, 5%	102-1-5
--	Knob, Retainer	710-56
--	X-Y Oscilloscope Monitor	2000-60
—	Connector	551-132
--	Cable	800-107
VR1	Regulator, 5V	54-17
—	Connector Pin	551-35
P2	Connector, 3-Pin	551-49
—	Ground Lug	706-12
—	Nylon Shoulder Washer	790-52
—	Insulator	790-71

Table 6-8. Replaceable Electrical Parts, Interface Control (A8) PCB

A8	**Interface Control PC Board Assembly**	**560A-C-11346-3**
	CAPACITORS	
C1	Mylar, 0.1µF	210-30
C2	Mica, 270pF	220-270
C3	Tantalum, 1µF, 35V	250-19
C4	Disc, .002µF, 50V	230-33
C5	Tantalum, 1µF, 35V	250-19
C6	Disc, .002µF, 50V	230-33
C7	Disc, .01µF	230-11
C8	Disc, .002µF, 50V	230-33
C9	Disc, .01µF	230-11
C10	Tantalum, 10µF, 25V	250-42
C11	Tantalum, 10µF, 25V	250-42
	CONNECTORS	
P1	Male, 11-pin	551-258
P2	Male, 11-pin	551-258
	DIODES	
CR1	Silicon, 1N4446	10-1N4446
CR2	Silicon, 1N4446	10-1N4446

Table 6-8. Replaceable Electrical Parts, Interface Control (A8) PCB (Continued)

REF DES.	DESCRIPTION	WILTRON PART NO.
CR3	Silicon, 1N4446	10-1N4446
CR4	Silicon, 1N4446	10-1N4446
CR5	Silicon, 1N4446	10-1N4446
CR6	Silicon, 1N4446	10-1N4446
CR7	Silicon, SI2	10-SI2
CR8	Silicon, SI2	10-SI2
CR9	Germanium, 1N270	10-10
CR10	Germanium, 1N270	10-10
CR11	Germanium, 1N270	10-10
CR12	Germanium, 1N270	10-10
CR13	Silicon, 1N4446	10-1N4446
CR14	Silicon, 1N4446	10-1N4446
CR15	Germanium, IN270	10-10
	INTEGRATED CIRCUITS	
U1	Quad Op Amp, TL074CN	54-132
U2	Quad Comparator, LM3302N	54-MC3302
U3	Dual Op Amp, TL072CP	54-53
	RESISTORS	
R1	MF, 10k, 1/4W, 1%	110-10k-1
R2	MF, 10k, 1/4W, 1%	110-10k-1
R3	MF, 100Ω, 1/4W, 1%	110-100-1
R4	MF, 10k, 1/4W, 1%	110-10k-1
R5	MF, 100k, 1/4W, 1%	110-100k-1
R6	MF, 1k, 1/4W, 1%	110-1k-1
R7	MF, 2.21k, 1/4W, 1%	110-2.21k-1
R8	MF, 82.5Ω, 1/4W, 1%	110-82.5-1
R9	MF, 147Ω, 1/4W, 1%	110-147-1
R10	MF, 10k, 1/4W, 1%	110-10k-1
R11	MF, 10k, 1/4W, 1%	110-10k-1
R12	MF, 196k, 1/4W, 1%	110-196k-1
R13	MF, 2M, 1/4W, 1%	110-2M-1
R14	MF, 2.21k, 1/4W, 1%	110-2.21k-1
R15	MF, 10k, 1/4W, 1%	110-10k-1
R16	MF, 10k, 1/4W, 1%	110-10k-1
R17	MF, 10k, 1/4W, 1%	110-10k-1
R18	MF, 82.5Ω, 1/4W, 1%	110-82.5-1
R19	MF, 10k, 1/4W, 1%	110-10k-1
R20	MF, 100k, 1/4W, 1%	110-100k-1
R21	MF, 100k, 1/4W, 1%	110-100k-1
R22	MF, 715k, 1/4W, 1%	110-715k-1
R23	MF, 715k, 1/4W, 1%	110-715k-1
R24	MF, 2.21k, 1/4W, 1%	110-2.21k-1
R25	MF, 10k, 1/4W, 1%	110-10k-1
R26	MF, 715k, 1/4W, 1%	110-715k-1
R27	MF, 5.11k, 1/4W, 1%	110-5.11k-1
R28	MF, 5.11k, 1/4W, 1%	110-5.11k-1
R29	MF, 715k, 1/4W, 1%	110-715k-1
R30	MF, 10k, 1/4W, 1%	110-10k-1
R31	MF, 17.8k, 1/4W, 1%	110-17.8k-1
R32	MF, 249Ω, 1/4W, 1%	110-249-1
R33	MF, 249Ω, 1/4W, 1%	110-249-1
R34	MF, 10k, 1/4W, 1%	110-10k-1
R35	MF, 78.7k, 1/4W, 1%	110-78.7k-1
R36	MF, 10k, 1/4W, 1%	110-10k-1
R37	MF, 10k, 1/4W, 1%	110-10k-1
R38	CC, 1k, 1/2W, 5%	102-1k-5
R39	MF, 34.8k, 1/4W, 1%	110-34.8k-1
R40	MF, 100k, 1/4W, 1%	110-100k-1
R41	MF, 10k, 1/4W, 1%	110-10k-1
	TRANSISTORS	
Q1	N-Channel, JFET, J112	20-17
Q2	N-Channel, JFET, J112	20-17
Q3	PNP, 2N4249	20-2N4249
Q4	NPN, 2N3694	20-2N3694
Q5	NPN, 2N3694	20-2N3694
Q6	NPN, 2N3694	20-2N3694
Q7	NPN, 2N3694	20-2N3694
Q8	PNP, 2N4249	20-2N4249
Q9	NPN, 2N3694	20-2N3694

6-5 REPLACEABLE ELECTRICAL PARTS - CRT MAINFRAME

The CRT mainframe is purchased from Tektronix, Inc. The replaceable electrical parts list, which is extracted from the Tektronix Model 620 Instruction Manual and reprinted here with their permission, is contained in Table 6-10.

6-5.1 Parts Ordering Information

Replacement parts that have a WILTRON part number assigned (Table 6-10) may be ordered directly from WILTRON; all other parts are available from Tektronix, Inc.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. It is therefore important, when ordering parts, to include the following information in your order: part number, instrument type or number, serial number, and modification number if applicable.

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

6-5.2 List of Assemblies

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

6-5.3 Cross-Index - Mfr. Code Number to Manufacturer

The Mfr. Code Number to Manufacturer index for the electrical parts list is located in Table 6-9. The cross index provides codes, names and addresses of manufacturers of components listed in Table 6-10.

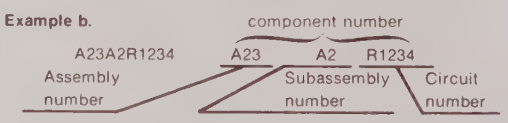
6-5.4 Abbreviations

Abbreviations conform to American National Standard Y1.1.

6-5.5 Component Number (Column 1 of Table 6-10)

A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Read: Resistor 1234 of Assembly 23



Read: Resistor 1234 of Subassembly 2 of Assembly 23

6-5.6 Textronix Part No. (Column 2 of Table 6-10)

Indicates part number to be used when ordering replacement part from Tektronix.

6-5.7 Name and Description (Column 3 of Table 6-10)

In the Parts List, an Item Name is separated from the description by a colon (:).

Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

6-5.8 Mfr. Code (Column 4 of Table 6-10)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

6-5.9 Mfr. Part Number (Column 5 of Table 6-10)

Indicates actual manufacturers part number.

6-5.10 WILTRON Part Number (Column 6 of Table 6-10)

Indicates part number to be used when ordering a replacement part from WILTRON.

Table 6-9. Cross-Index - Mfr. Code Number to Manufacturer

Mfr. Code	Manufacturer	Address	City, State, Zip
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
14099	SEMTECH CORP.	652 MITCHELL RD.	NEWBURY PARK, CA 91320
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
31918	IEE/SCHADOW INC.	8081 WALLACE ROAD	EDEN PRAIRIE, MN 55343
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
74276	SIGNALITE DIV., GENERAL INSTRUMENT CORP.	1933 HECK AVE.	NEPTUNE, NJ 07753
74970	JOHNSON, E.F., CO.	299 10TH AVE. S. W.	WASECA, MN 56093
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
84411	TRW ELECTRONIC COMPONENTS, TRW CAPACITORS	112 W. FIRST ST.	OGALLALA, NE 69153
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E WASHINGTON STREET P O BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
93410	ESSEX INTERNATIONAL, INC., CONTROLS DIV. LEXINGTON PLANT	P. O. BOX 1007	MANSFIELD, OH 44903

Table 6-10. Replaceable Electrical Parts - CRT Mainframe

Comp. No.	Tektronix Part No.	Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
A1	670-5732-00	CKT BOARD ASSY:DEFLECTION & Z AXIS	80009	670-5732-00	2000-79
A2	670-5731-02	CKT BOARD ASSY:POWER SUPPLY	80009	670-5731-00	2000-800
A1	670-5732-00	CKT BOARD ASSY:DEFLECTION & Z AXIS	80009	670-5732-00	
A1C121	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A1C128	281-0508-00	CAP.,FXD,CER DI:12PF,+/-0.6PF,500V	72982	301-000C0G0120J	
A1C133	281-0526-00	CAP.,FXD,CER DI:1.5PF,+/-0.5PF,500V	72982	301-000S2K0159D	
A1C171	281-0775-00	CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M	
A1C183	281-0526-00	CAP.,FXD,CER DI:1.5PF,+/-0.5PF,500V	72982	301-000S2K0159D	

Table 6-10. Replaceable Electrical Parts - CRT Mainframe (Continued)

Comp. No.	Tektronix Part No.	Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
A1C221	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A1C228	281-0508-00	CAP.,FXD,CER DI:12PF,+/-0.6PF,500V	72982	301-000C0G0120J	
A1C233	281-0526-00	CAP.,FXD,CER DI:1.5PF,+/-0.5PF,500V	72982	301-000S2K0159D	
A1C271	281-0775-00	CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M	
A1C283	281-0526-00	CAP.,FXD,CER DI:1.5PF,+/-0.5PF,500V	04222	7001-1313	
A1C293	281-0153-00	CAP.,VAR,AIR DI:1.7-10PF,250V	74970	187-0106-005	
A1C349	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A1C369	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A1C371	281-0661-00	CAP.,FXD,CER DI:0.8PF,+/-0.1PF,500V	72982	301-000C0K0808B	
A1C379	283-0341-00	CAP.,FXD,CER DI:0.047UF,10%,100V	72982	8121N153X7R0473K	
A1C396	290-0536-00	CAP.,FXD,ELCTLT:10UF,20%,25V	90201	TDC106M025FL	
A1C397	290-0536-00	CAP.,FXD,ELCTLT:10UF,20%,25V	90201	TDC106M025FL	
A1C398	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A1C402	290-0536-00	CAP.,FXD,ELCTLT:10UF,20%,25V	90201	TDC106M025FL	
A1C403	290-0534-00	CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1	
A1C404	283-0178-00	CAP.,FXD,CER DI:0.1UF,+80-20%,100V	72982	8131N145651104Z	
A1CR122	152-0246-00	SEMICOND DEVICE:SILICON,400PIV,200MA	80009	152-0246-00	
A1CR142	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	80009	152-0242-00	
A1CR175	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR176	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR177	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR178	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR192	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	80009	152-0242-00	
A1CR222	152-0246-00	SEMICOND DEVICE:SILICON,400PIV,200MA	80009	152-0246-00	
A1CR242	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	80009	152-0242-00	
A1CR275	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR276	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR277	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR278	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR292	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	80009	152-0242-00	
A1CR327	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR334	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR351	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR354	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR361	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR362	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR363	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR364	152-0141-02	SEMICOND DEVICE:SILICON,30V,150MA	80009	152-0141-02	
A1CR381	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	80009	152-0242-00	
A1CR382	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	80009	152-0242-00	
A1Q123	151-1054-00	TRANSISTOR:SILICON,JFE,N-CHANNEL,DUAL	80009	151-1054-00	2000-76
A1Q136	151-0192-00	TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	80009	151-0192-00	2000-75
A1Q141	151-0453-00	TRANSISTOR:SILICON,PNP	80009	151-0453-00	2000-74
A1Q186	151-0192-00	TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	80009	151-0192-00	2000-75
A1Q191	151-0453-00	TRANSISTOR:SILICON,PNP	80009	151-0453-00	2000-74
A1Q223	151-1054-00	TRANSISTOR:SILICON,JFE,N-CHANNEL,DUAL	80009	151-1054-00	2000-76
A1Q236	151-0192-00	TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	80009	151-0192-00	2000-75
A1Q241	151-0453-00	TRANSISTOR:SILICON,PNP	80009	151-0453-00	2000-74
A1Q286	151-0192-00	TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	80009	151-0192-00	2000-75
A1Q291	151-0453-00	TRANSISTOR:SILICON,PNP	80009	151-0453-00	2000-74
A1Q327	151-0341-00	TRANSISTOR:SILICON,NPN	80009	151-0341-00	
A1Q334	151-0342-00	TRANSISTOR:SILICON,PNP	80009	151-0342-00	
A1Q353	151-1054-00	TRANSISTOR:SILICON,JFE,N-CHANNEL,DUAL	80009	151-1054-00	2000-76
A1Q354	151-0342-00	TRANSISTOR:SILICON,PNP	80009	151-0342-00	
A1Q367	151-0341-00	TRANSISTOR:SILICON,NPN	80009	151-0341-00	
A1Q369	151-0406-00	TRANSISTOR:SILICON,PNP	80009	151-0406-00	2000-73

Table 6-10. Replaceable Electrical Parts - CRT Mainframe (Continued)

Comp. No.	Tektronix Part No.	Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
A1Q379	151-0407-01	TRANSISTOR:SILICON,NPN	80009	151-0407-01	20-15
A1R113	322-0481-00	RES.,FXD,FILM:1M OHM,1%,0.25W	75042	CEBT0-1004F	
A1R121	315-0104-00	RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045	
A1R122	315-0102-00	RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025	
A1R123	321-0286-00	RES.,FXD,FILM:9.31K OHM,1%,0.125W	91637	MFF1816G93100F	
A1R125	311-1563-00	RES.,VAR,NONWIR:1K OHM,20%,0.50W	73138	91-85-0	
A1R126	321-0197-00	RES.,FXD,FILM:1.1K OHM,1%,0.125W	91637	MFF1816G11000F	
A1R129	315-0222-00	RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225	
A1R133	321-0344-00	RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F	
A1R136	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R137	315-0272-00	RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725	
A1R139	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R141	323-0608-00	RES.,FXD,FILM:6K OHM,1%,0.5W	91637	MFF1226G060000F	
A1R142	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A1R147	315-0220-00	RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205	
A1R148	321-0174-00	RES.,FXD,FILM:634 OHM,1%,0.125W	91637	MFF1816G634R0F	
A1R149	315-0220-00	RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205	
A1R164	321-0225-00	RES.,FXD,FILM:2.15K OHM,1%,0.125W	91637	MFF1816G21500F	
A1R165	321-0256-00	RES.,FXD,FILM:4.53K OHM,1%,0.125W	91637	MFF1816G45300F	
A1R166	321-0225-00	RES.,FXD,FILM:2.15K OHM,1%,0.125W	91637	MFF1816G21500F	
A1R171	321-0204-00	RES.,FXD,FILM:1.3K OHM,1%,0.125W	91637	MFF1816G13000F	
A1R173	321-0286-00	RES.,FXD,FILM:9.31K OHM,1%,0.125W	91637	MFF1816G93100F	
A1R178	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R183	321-0344-00	RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F	
A1R186	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R187	315-0272-00	RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725	
A1R189	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R191	323-0608-00	RES.,FXD,FILM:6K OHM,1%,0.5W	91637	MFF1226G060000F	
A1R192	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A1R213	322-0481-00	RES.,FXD,FILM:1M OHM,1%,0.25W	75042	CEBT0-1004F	
A1R221	315-0104-00	RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045	
A1R222	315-0102-00	RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025	
A1R223	321-0286-00	RES.,FXD,FILM:9.31K OHM,1%,0.125W	91637	MFF1816G93100F	
A1R225	311-1563-00	RES.,VAR,NONWIR:1K OHM,20%,0.50W	73138	91-85-0	
A1R226	321-0206-00	RES.,FXD,FILM:1.37K OHM,1%,0.125W	91637	MFF1816G13700F	
A1R229	315-0222-00	RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225	
A1R233	321-0344-00	RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF18.6G37401F	
A1R236	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R237	315-0272-00	RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725	
A1R239	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R241	323-0608-00	RES.,FXD,FILM:6K OHM,1%,0.5W	91637	MFF1226G060000F	
A1R242	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A1R247	315-0220-00	RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205	
A1R248	321-0174-00	RES.,FXD,FILM:634 OHM,1%,0.125W	91637	MFF1816G634R0F	
A1R249	315-0220-00	RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205	
A1R264	321-0225-00	RES.,FXD,FILM:2.15K OHM,1%,0.125W	91637	MFF1816G21500F	
A1R265	321-0256-00	RES.,FXD,FILM:4.53K OHM,1%,0.125W	91637	MFF1816G45300F	
A1R266	321-0225-00	RES.,FXD,FILM:2.15K OHM,1%,0.125W	91637	MFF1816G21500F	
A1R271	321-0204-00	RES.,FXD,FILM:1.3K OHM,1%,0.125W	91637	MFF1816G13000F	110-1.3K-1
A1R273	321-0286-00	RES.,FXD,FILM:9.31K OHM,1%,0.125W	91637	MFF1816G93100F	
A1R278	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R283	321-0344-00	RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F	
A1R286	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R287	315-0272-00	RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725	
A1R289	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R291	323-0608-00	RES.,FXD,FILM:6K OHM,1%,0.5W	91637	MFF1226G060000F	
A1R292	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	

Table 6-10. Replaceable Electrical Parts - CRT Mainframe (Continued)

Comp. No.	Tektronix Part No.	Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
A1R326	315-0222-00	RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225	
A1R329	321-0323-00	RES.,FXD,FILM:22.6K OHM,1%,0.125W	91637	MFF1816G22601F	
A1R331	315-0302-00	RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025	
A1R334	321-0264-00	RES.,FXD,FILM:5.49K OHM,1%,0.125W	91637	MFF1816G54900F	
A1R336	321-0183-00	RES.,FXD,FILM:787 OHM,1%,0.125W	91637	MFF1816G787R0F	
A1R343	322-0481-00	RES.,FXD,FILM:1M OHM,1%,0.25W	75042	CEBT0-1004F	
A1R349	315-0104-00	RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045	
A1R351	315-0102-00	RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025	
A1R353	315-0240-00	RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405	
A1R354	321-0264-00	RES.,FXD,FILM:5.49K OHM,1%,0.125W	91637	MFF1816G54900F	
A1R355	315-0240-00	RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405	
A1R357	321-0249-00	RES.,FXD,FILM:3.83K OHM,1%,0.125W	91637	MFF1816G38300F	
A1R363	321-0289-00	RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F	
A1R364	321-0396-00	RES.,FXD,FILM:130K OHM,1%,0.125W	91637	MFF1816G13002F	
A1R366	315-0201-00	RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015	
A1R367	315-0152-00	RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525	
A1R371	321-0320-00	RES.,FXD,FILM:21K OHM,1%,0.125W	91637	MFF1816G21001F	
A1R372	321-0320-00	RES.,FXD,FILM:21K OHM,1%,0.125W	91637	MFF1816G21001F	
A1R376	315-0203-00	RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035	
A1R377	315-0222-00	RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225	
A1R379	315-0301-00	RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015	
A1R382	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1R396	315-0100-00	RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005	
A1R397	315-0100-00	RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005	
A1R398	315-0100-00	RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005	
A1R402	315-0100-00	RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005	
A1R403	315-0100-00	RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005	
A1R404	315-0101-00	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015	
A1VR326	152-0227-00	SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ13903	

Table 6-10. Replaceable Electrical Parts - CRT Mainframe (Continued)

Comp. No.	Tektronix Part No.	Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
A2	670-5731-00	CKT BOARD ASSY:POWER SUPPLY	80009	670-5731-00	
A2C107	290-0719-00	CAP.,FXD,ELCTLT:47UF,20%,25V	56289	196D476X0025TE3	
A2C108	290-0719-00	CAP.,FXD,ELCTLT:47UF,20%,25V	56289	196D476X0025TE3	
A2C116	283-0351-00	CAP.,FXD,CER DI:5000PF,20%,3000V	72982	848-023Z5U0502M	2000-81
A2C121	285-1184-00	CAP.,FXD,MTLZD:0.01UF,20%,4000V	84411	TEK-183103040	2000-82
A2C123	285-1184-00	CAP.,FXD,MTLZD:0.01UF,20%,4000V	84411	TEK-183103040	2000-82
A2C127	281-0513-00	CAP.,FXD,CER DI:27PF,+/-5.4PF,500V	72982	301-000P2G0270M	
A2C131	290-0758-00	CAP.,FXD,ELCTLT:2.2UF,+50-10%,160V	56289	502D227	
A2C133	283-0279-00	CAP.,FXD,CER DI:0.001UF,20%,3000V	56289	55C153	2000-83
A2C139	285-1082-00	CAP.,FXD,CER PLASTIC:0.47UF,20%,200V	14752	230B1C474	
A2C140	290-0758-00	CAP.,FXD,ELCTLT:2.2UF,+50-10%,160V	56289	502D227	
A2C142	283-0177-00	CAP.,FXD,CER DI:1UF,+80-20%,25V	72982	8131N039 E 105Z	
A2C143	290-0536-00	CAP.,FXD,ELCTLT:10UF,20%,25V	90201	TDC106M025FL	
A2C151	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A2C156	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A2C161	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A2C167	285-1184-00	CAP.,FXD,CER MTLZD:0.01UF,20%,4000V	84411	TEK-183103040	2000-82
A2C171	283-0198-00	CAP.,FXD,CER DI:0.22UF,20%,50V	72982	8121N083Z5U0224M	
A2C173	290-0534-00	CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1	
A2C177	283-0067-00	CAP.,FXD,CER DI:0.001UF,10%,200V	72982	835-515B102K	
A2C183	283-0198-00	CAP.,FXD,CER DI:0.22UF,20%,50V	72982	8121N083Z5U0224M	
A2C186	283-0279-00	CAP.,FXD,CER DI:0.001UF,20%,3000V	56289	55C153	2000-83
A2C221	290-0571-00	CAP.,FXD,ELCTLT:5000UF,+100-0%,25V	90201	PFP20-36043	
A2C243	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A2C247	290-0527-00	CAP.,FXD,ELCTLT:15UF,20%,20V	90201	TDC156M020FL	
A2C256	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A2C257	290-0527-00	CAP.,FXD,ELCTLT:15UF,20%,20V	90201	TDC156M020FL	
A2C276	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K	
A2C277	290-0758-00	CAP.,FXD,ELCTLT:2.2UF,+50-10%,160V	56289	502D227	
A2CR116	152-0429-00	SEMICOND DEVICE:SILICON,5000V,10MA	14099	SA3282	2000-84
A2CR117	152-0429-00	SEMICOND DEVICE:SILICON,5000V,10MA	14099	SA3282	2000-84
A2CR131	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004	
A2CR133	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004	
A2CR134	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004	
A2CR136	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004	
A2CR139	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004	
A2CR140	152-0242-00	SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004	
A2CR142	152-0333-00	SEMICOND DEVICE:SILICON,55V,200MA	80009	152-0333-00	
A2CR143	152-0333-00	SEMICOND DEVICE:SILICON,55V,200MA	80009	152-0333-00	
A2CR171	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR172	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR173	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR174	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR181	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR182	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR220	152-0556-00	SEMICOND DEVICE:BRIDGE,50V,2.5A	04713	SDA10271K	
A2CR236	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR237	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR238	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR262	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR263	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR282	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	
A2CR283	152-0141-02	SEMICOND DEVICE:SILICON,30V,50NA	80009	152-0141-02	

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Table 6-10. Replaceable Electrical Parts - CRT Mainframe (Continued)

Comp. No.	Tektronix Part No.	Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
A2DS122	150-0050-00	LAMP,GLOW:135V MAX,1.9MA	74276	LT2-24-2(NE2H)	
A2DS191	150-0050-00	LAMP,GLOW:135V MAX,1.9MA	74276	LT2-24-2(NE2H)	
A2DS192	150-0050-00	LAMP,GLOW:135V MAX,1.9MA	74276	LT2-24-2(NE2H)	
A2E136	119-0181-00	ARSR,ELEC SURGE:230V,GAS FILLED	80009	119-0181-00	
A2F225	159-0160-00	FUSE,CARTRIDGE:3AG,1.5A, 250V,SLOW-BLOW	71400	MDX 1 25/100	631-13
A2F226	159-0016-00	FUSE,CARTRIDGE:3AG,1.5A,250V,FAST-BLOW	71400	AGC 1 1/2	631-34
A2F227	159-0029-00	FUSE,CARTRIDGE:3AG,0.3A,250V,SLOW-BLOW	71400	MDL3/10	631-7
A2Q173	151-0192-00	TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801	2000-75
A2Q241	151-0462-00	TRANSISTOR:SILICON,PNP	04713	TIP30C	
A2Q265	151-0464-00	TRANSISTOR:SILICON,NPN	04713	SJE412	2000-71
A2Q280	151-0453-00	TRANSISTOR:SILICON,PNP	80009	151-0453-00	2000-74
A2Q285	151-0464-00	TRANSISTOR:SILICON,NPN	04713	SJE412	2000-71
A2R107	308-0685-00	RES.,FXD,WW:1.5 OHM,5%,1W	75042	BW20-1R500J	
A2R121	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A2R122	315-0153-00	RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535	
A2R123	315-0391-00	RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915	
A2R127	315-0474-00	RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745	
A2R130	311-1915-00	RES.,VAR,NONWIR:20K OHM,10%,0.50W	73138	72-196-0	
A2R131	316-0471-00	RES.,FXD,CMPSN:470 OHM,10%,0.25W	01121	CB4711	
A2R133	315-0472-00	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725	
A2R134	316-0471-00	RES.,FXD,CMPSN:470 OHM,10%,0.25W	01121	CB4711	
A2R136	315-0226-00	RES.,FXD,CMPSN:22M OHM,5%,0.25W	01121	CB2265	
A2R145	311-1373-00	RES.,VAR,NONWIR:TRMR,5K OHM,10%,0.5W	73138	72-198-0	
A2R150	315-0333-00	RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335	
A2R151	316-0471-00	RES.,FXD,CMPSN:470 OHM,10%,0.25W	01121	CB4711	
A2R155	311-1914-00	RES.,VAR,NONWIR:TRMR,50K OHM,10%,0.50W	73138	72-202-0	
A2R156	317-0471-00	RES.,FXD,CMPSN:470 OHM,5%,0.125W	01121	BB4715	
A2R160	311-1914-00	RES.,VAR,NONWIR:TRMR,50K OHM,10%,0.50W	73138	72-202-0	
A2R161	316-0471-00	RES.,FXD,CMPSN:470 OHM,10%,0.25W	01121	CB4711	
A2R163	307-0572-00	RES NTWK,FXD FI:HIGH VOLTAGE DIVIDER	80009	307-0572-00	2000-69
A2R165	311-1312-00	RES.,VAR,NONWIR:5M OHM,20%,1W	01121	73M4G048L505M	
A2R167	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A2R169	307-0103-00	RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5	
A2R171	315-0100-00	RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005	
A2R174	315-0472-00	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725	
A2R176	315-0155-00	RES.,FXD,CMPSN:1.5M OHM,5%,0.25W	01121	CB1555	
A2R177	315-0562-00	RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625	
A2R178	315-0473-00	RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735	
A2R182	315-0473-00	RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735	
A2R183	321-0366-00	RES.,FXD,FILM:63.4K OHM,1%,0.125W	91637	MFF1816G63401F	
A2R191	316-0270-00	RES.,FXD,CMPSN:27 OHM,10%,0.25W	01121	CB2701	
A2R231	321-0200-00	RES.,FXD,FILM:1.18K OHM,1%,0.125W	91637	MFF1816G11800F	
A2R232	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A2R233	315-0391-00	RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915	
A2R241	307-0057-00	RES.,FXD,CMPSN:5.1 OHM,5%,0.50W	01121	EB51G5	
A2R242	308-0248-00	RES.,FXD,WW:150 OHM,1%,5W	91637	RS2A-B150R0F	
A2R244	321-0265-00	RES.,FXD,FILM:5.62K OHM,1%,0.125W	91637	MFF1816G56200F	
A2R245	311-1563-00	RES.,VAR,NONWIR:1K OHM,20%,0.50W	73138	91A R1K	
A2R246	321-0249-00	RES.,FXD,FILM:3.83K OHM,1%,0.125W	91637	MFF1816G38300F	

Table 6-10. Replaceable Electrical Parts - CRT Mainframe (Continued)

Comp. No.	Tektronix Part No.	Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
A2R254	321-0335-00	RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	MFF1816G30101F	
A2R256	321-0335-00	RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	MFF1816G30101F	
A2R260	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A2R261	315-0391-00	RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915	
A2R266	307-0107-00	RES.,FXD,CMPSN:5.6 OHM,5%,0.25W	01121	CB56G5	
A2R274	321-0335-00	RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	MFF1816G30101F	
A2R276	321-0399-00	RES.,FXD,FILM:140K OHM,1%,0.125W	91637	MFF1816G14002F	
A2R279	315-0471-00	RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715	
A2R280	315-0472-00	RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725	
A2R281	315-0271-00	RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715	
A2R286	307-0057-00	RES.,FXD,CMPSN:5.1 OHM,5%,0.50W	01121	EB51G5	
A2R287	315-0100-00	RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005	
A2R291	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A2R292	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A2R293	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A2R294	315-0221-00	RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215	
A2R305	311-1313-00	RES.,VAR,NONWIR:2K OHM,20%,1W	01121	73M4G048L202M	
A2R315	311-1313-00	RES.,VAR,NONWIR:2K OHM,20%,1W	01121	73M4G048L202M	
A2R325	311-1710-00	RES.,VAR,NONWIR:20K OHM,20%,1W	01121	16M148	
A2T110	120-1202-00	XFMR,PWR,SDN & SU:HIGH VOLTAGE	80009	120-1202-00	2000-86
A2U110	152-0637-02	SEMICOND DVC,DI:HV MULTR,CHECKED	80009	152-0637-02	2000-85
A2U175	156-0158-00	MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	80009	156-0158-00	
A2U232	156-0158-00	MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	80009	156-0158-00	
A2VR130	152-0268-00	SEMICOND DEVICE:ZENER,0.4W,56V,5%	80009	152-0268-00	
A2VR150	152-0241-00	SEMICOND DEVICE:ZENER,0.4W,33V,5%	80009	152-0241-00	10-1
A2VR231	152-0461-00	SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	80009	152-0461-00	10-1N823
A2VR232	152-0149-00	SEMICOND DEVICE:ZENER,0.4W,10V,5%	80009	152-0149-00	10-1N758A
A2VR260	152-0149-00	SEMICOND DEVICE:ZENER,0.4W,10V,5%	80009	152-0149-00	10-1N758A

Table 6-10. Replaceable Electrical Parts - CRT Mainframe (Continued)

Comp. No.	Tektronix Part No.	Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
		CHASSIS PARTS			
F42	159-0029-00	FUSE,CARTRIDGE:3AG,0.3A,250V,SLOW-BLOW	71400	MDL3/10	
F42	159-0054-00	FUSE,CARTRIDGE:3AG,0.15A,250V,SLOW-BLOW	71400	MDL 15/100	
	----- -----	(ALTERNATE - 220V OPERATION)			
J12	131-0955-00	CONNECTOR,RCPT,:BNC,FEMALE,W/HARDWARE	13511	31-279	
J17	131-0955-00	CONNECTOR,RCPT,:BNC,FEMALE,W/HARDWARE	13511	31-279	
J21	131-0955-00	CONNECTOR,RCPT,:BNC,FEMALE,W/HARDWARE	13511	31-279	
J25	131-0955-00	CONNECTOR,RCPT,:BNC,FEMALE,W/HARDWARE	13511	31-279	
Q35	151-0349-05	TRANSISTOR:SILICON,NPN,SCREENED	80009	151-0349-05	2000-114
T210	120-1201-00	XFMR,PWR,STPDN:	80009	120-1201-00	
V39	154-0798-00	ELECTRON TUBE:CRT,P31,T6200	80009	154-0798-00	2000-87

6-6 REPLACEABLE MECHANICAL PARTS - CRT MAINFRAME

The CRT mainframe is purchased from Tektronix, Inc. The replaceable mechanical parts list, which is extracted from the Tektronix Model 620 Instruction Manual and reprinted here with their permission, is contained in Table 6-12.

6-6.1 Parts Ordering Information

Replacement parts that have a WILTRON part number assigned (Table 6-12) may be ordered directly from WILTRON; all other parts are available from Tektronix, Inc.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type of number, serial number, and modification number if applicable.

6-6.2 Figure and Index Numbers

Items in this section are referenced by figure and index numbers to the illustrations.

6-6.3 Indentation System

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                    Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
                  - - - ' - - -
  Detail Part of Assembly and/or Component
  Attaching parts for Detail Part
                  - - - ' - - -
    Parts of Detail Part
    Attaching parts for Parts of Detail Part
                  - - - ' - - -
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol--- ---indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

An Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

6-6.4 Abbreviations

"	In
#	Number Size
ACTR	Actuator
ADPTR	Adapter
ALIGN	Alignment
AL	Aluminum
ASSEM	Assembled
ASSY	Assembly
ATTEN	Attenuator
AWG	American Wire Gage
BD	Board
BRKT	Bracket
BRS	Brass
BRZ	Bronze
BSHG	Bushing
CAB	Cabinet
CAP	Capacitor
CER	Ceramic
CHAS	Chassis
CKT	Circuit
COMP	Composition
CONN	Connector
COV	Cover
CPLG	Coupling
CRT	Cathode Ray Tube
DEG	Degree
DWR	Drawer
ELCTRN	Electron
ELEC	Electrical
ELCTLT	Electrolytic
ELEM	Element
EPL	Electrical Parts List
EQPT	Equipment
EXT	External
FIL	Fillister Head
FLEX	Flexible
FLH	Flat Head
FLTR	Filter
FR	Frame or Front
FSTNR	Fastener
FT	Foot
FXD	Fixed
GSKT	Gasket
HDL	Handle
HEX	Hexagon
HEX HD	Hexagonal Head
HEX SOC	Hexagonal Socket
HLCPS	Helical Compression
HLEXT	Helical Extension
HV	High Voltage
IC	Integrated Circuit
ID	Inside Diameter
IDENT	Identification
IMPLR	Impeller
IN	INCH
INCAND	Incandescent
INSUL	Insulator
INTL	Internal
LPHLDR	Lampholder
MACH	Machine
MECH	Mechanical
MTG	Mounting
NIP	Nipple
NON WIRE	Not Wire Wound
OBD	Order by Description
OD	Outside Diameter
OVH	Oval Head
PH BRZ	Phosphor Bronze
PL	Plain or Plate
PLSTC	Plastic
PN	Part Number
PNH	Pan Head
PWR	Power
RCPT	Receptacle
RES	Resistor
RGD	Rigid
RLF	Relief
RTNR	Retainer
SCH	Socket Head
SCOPE	Oscilloscope
SCR	Screw
SE	Single End
SECT	Section
SEMICON	Semiconductor
SHLD	Shield
SHLDR	Shouldered
SKT	Socket
SL	Slide
SLFLKG	Self-Locking
SLVG	Sleeving
SPR	Spring
SQ	Square
SST	Stainless Steel
STL	Steel
SW	Switch
T	Tube
TERM	Terminal
THD	Thread
THK	Thick
TNSN	Tension
TPG	Tapping
TRH	Truss Head
V	Voltage
VAR	Variable
W/	With
WSHR	Washer
XFMR	Transformer
XSTR	Transistor

6-6.5 Cross-Index - Mfr. Code Number to Manufacturer

The Mfr. Code Number-to-Manufacturer Index for the mechanical parts list is located in Table 6-11. The cross-index provides codes, names and addresses of manufacturers of the components listed in Table 6-12.

The Mfr. Code Number-to-Manufacturer Index for the mechanical parts list is located in Table 6-11. The cross-index provides codes, names and addresses of manufacturers of the components listed in Table 6-12.

Table 6-11. Cross-Index - Mfr. Code Number to Manufacturer

Mfr. Code	Manufacturer	Address	City, State, Zip
000EA	ALLEGHENY LUDLUM STEEL	501 FORBES BLVD., SUITE 106	SAN FRANCISCO, CA 94080
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
05091	TRI-ORDINATE CORPORATION	343 SNYDER AVENUE	BERKELEY HEIGHTS, NJ 07922
05820	WAKEFIELD ENGINEERING, INC.	AUDUBON ROAD	WAKEFIELD, MA 01880
07111	PNEUMO DYNAMICS CORPORATION	4800 PRUDENTIAL TOWER	BOSTON, MA 02199
08261	SPECTRA-STRIP CORP.	7100 LAMPSON AVE.	GARDEN GROVE, CA 92642
11897	PLASTIGLIDE MFG. CORPORATION	P O BOX 867, 1757 STANFORD ST.	SANTA MONICA, CA 90406
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27264	MOLEX PRODUCTS CO.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
28520	HEYMAN MFG. CO.	147 N. MICHIGAN AVE.	KENILWORTH, NJ 07033
55210	GETTIG ENG. AND MFG. COMPANY	PO BOX 85, OFF ROUTE 45	SPRING MILLS, PA 16875
59730	THOMAS AND BETTS COMPANY	36 BUTLER ST.	ELIZABETH, NJ 07207
70485	ATLANTIC INDIA RUBBER WORKS, INC.	571 W. POLK ST.	CHICAGO, IL 60607
71159	BRISTOL SOCKET SCREW, DIV. OF AMERICAN CHAIN AND CABLE CO., INC.	P O BOX 2244, 40 BRISTOL ST.	WATERBURY, CT 06720
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
74445	HOLO-KROME CO.	31 BROOK ST. WEST	HARTFORD, CT 06110
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
77250	PHEOLL MANUFACTURING CO., DIVISION OF ALLIED PRODUCTS CORP.	5700 W. ROOSEVELT RD.	CHICAGO, IL 60650
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
82647	TEXAS INSTRUMENTS, INC., CONTROL PRODUCTS DIV.	34 FOREST ST.	ATTLEBORO, MA 02703
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
85471	BOYD, A. B., CO.	2527 GRANT AVENUE	SAN LEANDRO, CA 94579
86445	PENN FIBRE AND SPECIALTY CO., INC.	2032 E. WESTMORELAND ST.	PHILADELPHIA, PA 19134
93907	CAMCAR SCREW AND MFG. CO.	600 18TH AVE.	ROCKFORD, IL 61101
96904	NATVAR CORP.	211 RANDOLPH AVE.	WOODBRIDGE, NJ 07095

Table 6-12. Replaceable Mechanical Parts - CRT Mainframe

Comp. No.	Tektronix Part No.		Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
1-1	426-1468-00	1	FRAME,MASK:PLASTIC	80009	426-1468-00	
-2	200-2193-00	1	COVER,OPENING:LEFT,CRT RETAINER	80009	200-2193-00	2000-103
	200-2192-00	1	COVER,OPENING:RIGHT,CRT RETAINER	80009	200-2192-00	2000-102
-3	200-2143-01	1	RTNR,CRT SCALE:6.0 CRT,ALUM	80009	200-2143-01	
			(ATTACHING PARTS)			
-4	213-0808-00	4	SCREW,TPG,TR:8-32 X 0.625 L,TAPTITE,FILM	93907	OBD	
			- - - * - - -			
-5	337-2537-00	1	SHLD,IMPLOSION:5.854 X 4.714X 0.09,CLEAR	80009	337-2537-00	
-6	343-0751-00	4	CLAMP,CRT:6.0 INCH CRT	80009	343-0751-00	
			(ATTACHING PARTS FOR EACH)			
-7	211-0669-00	1	SCREW,MACHINE:6-32 X 0.75,FLH,90 DEG,SST	93907	OBD	
			- - - * - - -			
-8	366-1189-00	4	KNOB:GRAY	80009	366-1189-00	
	----- -----	-	. EACH KNOB INCLUDES:			
	213-0246-00	1	. SETSCREW:5-40 X 0.093 INCH L,HEX SOC	71159	OBD	
-9	333-2490-00	1	PANEL,FRONT:	80009	333-2490-00	
			(ATTACHING PARTS)			
-10	210-0586-00	2	NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00	
			- - - * - - -			
-11	384-0341-00	4	EXTENSION SHAFT:0.125 OD X 3.6 INCH LONG	80009	384-0341-00	860-A-7017-1 (Long) 560-A-7017-2 (Short)
-12	376-0051-01	4	CPLG,SHAFT,FLEX:FOR 0.125 INCH DIA SHAFTS	80009	376-0051-01	
	----- -----	-	. EACH COUPLER INCLUDES:			
	213-0048-00	4	. SETSCREW:4-40 X 0.125 INCH,HEX SOC STL	74445	OBD	
-13	426-1517-01	1	FRAME,CABINET:FRONT	80009	426-1517-01	
			(ATTACHING PARTS)			
-14	213-0760-00	4	SCREW,TPG,TF:8-32 X 0.875,SPCL TAPTITE	93907	OBD	
			- - - * - - -			
-15	----- -----	1	TRANSISTOR:(SEE Q35 EPL)			
			(ATTACHING PARTS)			
-16	211-0198-00	1	SCREW,MACHINE:4-40 X 0.438 PNH,STL,POZ	77250	OBD	

Table 6-12. Replaceable Mechanical Parts - CRT Mainframe (continued)

Comp. No.	Tektronix Part No.		Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
-17	210-0586-00	1	NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00	
-18	210-1122-00	1	WASHER,LOCK:0.228 ID X 0.375 INCH OD,STL	04713	B52200F006	
			- - - * - - -			
-19	342-0163-00	1	INSULATOR,PLATE:XSTR,0.675 X 0.625 X 0.001"	80009	342-0163-00	
-20	108-0918-00	1	COIL,TUBE DEFL:TRACE ROTATOR	80009	108-0918-00	
-21	348-0233-00	1	GROMMET,PLASTIC:GRAY,OVAL SHAPE,0.927 ID	80009	348-0233-00	
-22	348-0145-00	1	GROMMET,PLASTIC:U-SHP,1.0 X 0.42 INCH	80009	348-0145-00	
-23	348-0090-00	3	CUSHION,CRT:	85471	OBD	
-24	337-2521-00	1	SHIELD,CRT:	000EA	OBD	
			(ATTACHING PARTS)			
-25	210-0586-00	3	NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00	
-26	211-0008-00	3	SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD	
			- - - * - - -			
-27	136-0706-00	1	SKT,PL-IN ELEK:ELKTRN TUBE,11 CONT,W/LEADS	80009	136-0706-00	
-28	136-0301-01	1	. SKT,PL-IN ELEK:ELCTN TUBE,14CONTACT	80009	136-0301-01	
-29	131-0707-00	6	. CONNECTOR,TERM.:22-26 AWG,BRS& CU BE GOLD	22526	47439	
	131-0621-00	5	. CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	46231	
-30	352-0164-00	1	. CONN BODY,PL,EL:6 WIRE BLACK	80009	352-0164-00	
-31	162-0009-00	1	. INS SLV,ELEC:0.234 ID,VINYL,BLK,105 DEG	96904	TYPE 400SIZE3BLK	
-32	204-0640-00	1	BODY,CONN,RCPT:FOR 3 FEM CONT,NYLON	00779	1-480304-0	
-33	343-0786-01	1	CLAMP,CRT SHLD:	80009	343-0786-01	
			(ATTACHING PARTS)			
-34	211-0542-00	2	SCREW,MACHINE:6-32 X 0.312 INCH,TRH STL	83385	OBD	
-35	210-1124-00	2	WASHER,SPR TNSN:0.171 ID X 0.15 THK	78189	3502-08-15	
	220-0419-00	2	NUT,PLAIN,SQ:6-32 X 0.312 INCH,STL	83385	OBD	
			- - - * - - -			
-36	346-0133-00	3	STRAP,TIE DOWN:0.091 W X 14.0 L,PLASTIC	59730	TY-234M	
	334-3457-00	1	MARKER,IDENT:MARKED DANGER	80009	334-3457-00	
-37	348-0005-00	2	GROMMET,RUBBER:0.50 INCH DIA	70485	230	
-38	337-2582-00	1	SHIELD,ELECTRIC:CIRCUIT BOARD	80009	337-2582-00	
			(ATTACHING PARTS)			
-39	211-0019-00	4	SCREW,MACHINE:4-40 X 1.0 INCH,PNH STL	83385	OBD	
-40	361-0396-00	4	SPACER,SLEEVE:0.125 ID X 0.250 OD X 0.56 L	80009	361-0396-00	
			- - - * - - -			
1-41	----- -----	1	CKT BOARD ASSY:DEFLECTION Z-AXIS(SEE A1 EPL)			
	----- -----	-	. CKT BOARD ASSY INCLUDES:			
-42	131-2225-00	1	. CONNECTOR,TERM:22-24 AWG,BRASS	27264	09-52-3153	
-43	131-0608-00	8	. TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL	22526	47357	
-44	214-1291-00	2	. HEAT SINK,ELEC:XSTR,0.72 OD X 0.375"H	05820	207-AB	
-45	348-0566-00	2	. PAD,MOUNTING:TO-5 TRANSISTOR	80009	348-0566-00	
-46	131-0566-00	7	. LINK,TERM.CONNE:0.086 DIA X 2.375 INCH L	55210	L-2007-1	
-47	214-0579-00	1	. TERM.,TEST PT:BRS CD PL	80009	214-0579-00	
-48	337-1995-00	2	. SHLD,ELECTRICAL:DEFLECTION CIRCUIT CARD	80009	337-1995-00	
	198-4091-00	1	. WIRE SET,ELEC:	80009	198-4091-00	
-49	131-1109-01	4	. . CONNECTOR,TERM.:20-26 AWG,U/00.04 OD PIN	80009	131-1109-01	
-50	337-2596-00	1	SHIELD,ELEC:HIGH VOLTAGE	80009	337-2596-00	
			(ATTACHING PARTS)			
-51	211-0020-00	2	SCREW,MACHINE:4-40 X 1.125 INCH,PNH STL	83385	OBD	
			- - - * - - -			
-52	----- -----	1	SW,THRMSTC:(SEE S43 EPL)			
			(ATTACHING PARTS)			
-53	211-0008-00	2	SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD	
			- - - * - - -			
-54	255-0334-00	FT	PLASTIC CHANNEL:12.75 X 0.175X 0.155,NYL	11897	122-37-2500	
-55	407-2235-00	1	BRACKET,SUPPORT:TRANSFORMER	80009	407-2235-00	
			(ATTACHING PARTS)			
-56	212-0515-00	2	SCREW,MACHINE:10-32 X 2.250" HEX.HD STL	83385	OBD	
-57	212-0520-00	2	SCREW,MACHINE:10 X 32 X 1.25,HEX HD,STL	07111	OBD	
-58	220-0410-00	4	NUT,EXTENDED WA:10-32 X 0.375 INCH,STL	83385	OBD	
-59	210-0812-00	4	WASHER,NONMETAL:#10,FIBER	86445	OBD	
-60	361-0943-00	2	SPACER,SLEEVE:0.75 L X 0.196 ID	80009	361-0943-00	
			- - - * - - -			
-61	166-0226-00	4	INS SLV,ELEC:1.125 INCHES LONG	80009	166-0226-00	
-62	----- -----	1	TRANSFORMER:(SEE T210 EPL)			
			(ATTACHING PARTS)			
-63	129-0388-00	1	POST,ELEC-MECH:1.673 INCH LONG	80009	129-0388-00	
-64	211-0507-00	1	SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD	
			- - - * - - -			
-65	----- -----	1	CKT BOARD ASSY:HV(SEE A2 EPL)			
			(ATTACHING PARTS)			

Table 6-12. Replaceable Mechanical Parts - CRT Mainframe (continued)

Comp. No.	Tektronix Part No.		Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
-66	213-0789-00	4	SCREW,TPG,TF:6-32 X 0.375,TAPTITE,PNH	93907	OBD	
			- - - * - - -			
	----- -----	-	. CKT BOARD ASSY INCLUDES:			
-67	131-0608-00	24	. TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL	22526	47357	
-68	131-0589-00	8	. TERM,PIN:0.46 L X 0.025 SQ.PH BRZ GL	22526	47350	
-69	131-1895-00	1	. LINK,TERM. CONN:8,22 AWG,1.5 L	80009	131-1895-00	
	131-1896-00	1	. LINK,TERM. CONN:8,22 AWG,1.5 L	80009	131-1896-00	
-70	131-2233-00	1	. TERM,FEEDTHRU:0.75 L X 0.045 SQ	80009	131-2233-00	
-71	136-0514-00	2	. SOCKET,PLUG IN:MICROCIRCUIT,8 CONTACT	73803	CS9002-8	
-72	214-0579-00	4	. TERM.,TEST PT:BRS CD PL	80009	214-0579-00	
-73	131-0566-00	8	. LINK,TERM.CONNE:0.086 DIA X 2.375 INCH L	55210	L-2007-1	
-74	----- -----	2	. RES.,VAR NONWW:(SEE R305 AND R315 EPL)			
	----- -----	1	. RES.,VAR NONWW:(SEE R245 EPL)			
	----- -----	1	. RES.,VAR NONWW:(SEE R165 EPL)			
-75	344-0154-00	8	. CLIP,ELECTRICAL:FOR 0.25 INCH DIA FUSE	80009	344-0154-00	
	129-0368-00	3	. SPACER,POST:0.25 L TO MT SEAT,W/4-40 THD	80009	129-0368-00	
-76	407-2157-00	4	. BRACKET,CMPNT:UPPER EXTENSION	80009	407-2157-00	
			(ATTACHING PARTS FOR EACH)			
-77	213-0789-00	1	SCREW,TPG,TF:6-32 X 0.375,TAPTITE,PNH	93907	OBD	
			- - - * - - -			
-78	407-2158-00	1	BRACKET,CMPNT:UPPER EXTENSION	80009	407-2158-00	
			(ATTACHING PARTS)			
-79	213-0789-00	1	SCREW,TPG,TF:6-32 X 0.375,TAPTITE,PNH	93907	OBD	
			- - - * - - -			
1-80	407-2204-00	2	BRACKET,CMPNT:ALUMINUM	80009	407-2204-00	
			(ATTACHING PARTS FOR EACH)			
-81	213-0789-00	1	SCREW,TPG,TF:6-32 X 0.375,TAPTITE,PNH	93907	OBD	
			- - - * - - -			
-82	407-2250-00	4	BRACKET,CMPNT:ALUMINUM	80009	407-2250-00	
			(ATTACHING PARTS FOR EACH)			
-83	213-0789-00	1	SCREW,TPG,TF:6-32 X 0.375,TAPTITE,PNH	93907	OBD	
			- - - * - - -			
-84	200-0865-00	1	COVER,MTG HOLE:2.164 X 0.53,AL	80009	200-0865-00	
			(ATTACHING PARTS)			
-85	211-0097-00	1	SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD	
-86	210-0586-00	2	NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00	
			- - - * - - -			
	334-1379-00	1	LABEL:CRT,ADHESIVE BACK	80009	334-1379-00	
	334-3457-00	1	MARKER,IDENT:MARKED DANGER	80009	334-3457-00	
-87	200-0237-03	1	COVER,FUHLR:	80009	200-0237-03	
-88	352-0362-01	1	FUSEHOLDER:W/HARDWARE	75915	345002	
	200-2264-00	1	CAP.,FUSEHOLDER:3AG FUSES	S3629	031.1666(MDLFEU)	
	204-0837-00	1	BODY FUSEHOLDER:3AG,6.3A,250V,PNL MT	S3629	031.1681(MDLFEU)	
-89	161-0017-12	1	CABLE ASSY,PWR:3,18 AWG,125V	80009	161-0017-12	
-90	358-0529-00	1	BSHG,STRAIN RLF:FOR 0.3-0.36 OD CABLE,STR	28520	SR-63P-4	
-91	134-0159-00	1	BUTTON,PLUG:0.38 DIA,PLASTIC	80009	134-0159-00	
-92	----- -----	3	CONNECTOR,RCPT:(SEE J12,J17,J25 EPL)			
-93	407-2203-00	1	BRACKET,CMPNT:BRASS	80009	407-2203-00	
			(ATTACHING PARTS)			
	407-2203-01	1	BRACKET,CMPNT:ALUMINUM	80009	407-2203-01	
-94	211-0008-00	2	SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD	
			- - - * - - -			
-95	407-2201-00	1	BRACKET,CMPNT:BRASS	80009	407-2201-00	
			(ATTACHING PARTS)			
-96	211-0008-00	1	SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD	
			- - - * - - -			
-97	366-1402-93	1	PUSH BUTTON:GRAY--POWER	80009	366-1402-93	
-98	384-1059-00	1	EXTENSION SHAFT:6.58 INCH LONG	80009	384-1059-00	
-99	----- -----	1	SWITCH,PUSH(SEE S205 EPL)			
	334-3379-00	1	MARKER,IDENT:MARKED GROUNDSYMBOL	80009	334-3379-00	
-100	386-4004-01	1	PLATE,CAB,FRAME:REAR ALUMINUM	80009	386-4004-01	
			(ATTACHING PARTS)			
-101	213-0801-00	4	SCREW,TPG,TF:8-32 X 0.312,TAPTITE,PNH	93907	OBD	
			- - - * - - -			
-102	210-0202-00	1	TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N	
			(ATTACHING PARTS)			
-103	210-0457-00	1	NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD	
			- - - * - - -			
-104	426-1449-01	1	FRAME,CABINET:REAR,5.25 X 0.5 RACK	80009	426-1449-01	
-105	426-1541-00	4	FRAME SECT,CAB.:17.41 L,AL	80009	426-1541-00	
			(ATTACHING PARTS FOR EACH)			
-106	213-0760-00	1	SCREW,TPG,TF:8-32 X 0.875,SPCL TAPTITE	93907	OBD	
			- - - * - - -			

△See Title Page

Table 6-12. Replaceable Mechanical Parts - CRT Mainframe (continued)

Comp. No.	Tektronix Part No.		Name & Description	Mfr. Code	Mfr. Part Number	WILTRON Part No.
	198-4088-00	1	WIRE SET,ELEC:	80009	198-4088-00	
-107	131-0621-00	1	. CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	46231	
-108	352-0199-00	1	. CONN BODY,PL,EL:3 WIRE BLACK	80009	352-0199-00	
-109	175-0862-00	FT	. WIRE,ELECTRICAL:3 WIRE RIBBON	08261	SS-0322-1910610C	
	198-4089-00	1	WIRE SET,ELEC:	80009	198-4089-00	
-110	131-1055-00	2	. CONTACT,ELEC:CONN PIN,BRASS TIN	00779	60620-1	

SECTION VII
SERVICE

7-1 INTRODUCTION

This section provides general information, troubleshooting flow charts, and integrated service instructions for the 560A and its associated microwave components (RF detector and SWR Autotester).

7-2 GENERAL INFORMATION

Information regarding the WILTRON printed circuit board (PCB) exchange program and recommended test equipment for troubleshooting the 560A is contained in the following paragraphs.

7-2.1 Printed Circuit Board Exchange Program

WILTRON has a PCB exchange program that includes five of the six 560A PCBs: A1, A2, A3, A6, and A8. Upon request, and for a cost of approximately $250-$350 (exact cost available from Customer Service), WILTRON will immediately supply a replacement for any of the five PCBs covered by this program; the customer has 30 days to return the defective PCB. To obtain a replacement PCB, contact WILTRON Customer Service at 415-969-6500 and supply them with the serial number of the malfunctioning 560A.

7-2.2 Recommmended Test Equipment

To troubleshoot the 560A to a faulty PCB, only two items of test equipment are required: an oscilloscope and a digital multimeter. Any oscilloscope that contains a calibrated time base and a triggered sweep is suitable; any digital multimeter that will provide at least a 2-1/2 digit readout is suitable.

7-3 TROUBLESHOOTING

Troubleshooting in this manual is generally divided into assembly (PCB) and integrated or functional circuit maintenance levels. Troubleshooting to a PCB is accomplished through an analysis of front panel control operation, and through the use of logical troubleshooting flow charts. These troubleshooting flow charts are explained in a later paragraph. To use the troubleshooting flow charts requires access to the network analyzer section and CRT mainframe PCBs; how to gain access is explained in the following paragraph. Troubleshooting to an integrated or functional circuit is aided by the maintenance data contained in the service instructions. The service instructions are explained in paragraph 7-4.

7-3.1 Gaining Access to Network Analyzer and CRT Mainframe Printed Circuit Boards

The 560A network analyzer section and CRT mainframe PCBs are readily accessible on either the horizontal or the vertical (Option 2) chassis. To gain access, remove the four corner and two straight brackets on the rear of the 560A and slide the top, bottom, and side panels to the rear. On both the horizontal and vertical chassis, the CRT mainframe PCB adjustments are accessed from the top and right-hand side; the network analyzer section PCB components and adjustments are accessed from the bottom. Figure 7-1 shows a vertical chassis with the network analyzer section PCBs exposed.

7-3.2 Troubleshooting Flow Charts

Troubleshooting to a PCB assembly is accomplished using front panel controls, and

where necessary, logical troubleshooting flow charts. Table 3-5, provides the format for using front panel controls to troubleshoot to a malfunctioning PCB. In many cases the malfunctioning PCB is identified in the table's "If Indication Abnormal" column. In cases where further troubleshooting is necessary, however, the troubleshooting flow charts in Figures 7-2 thru 7-17 are provided. Each of these charts relates to a particular step in Table 3-5; the start symbol (top) in each chart indentifies the step number.

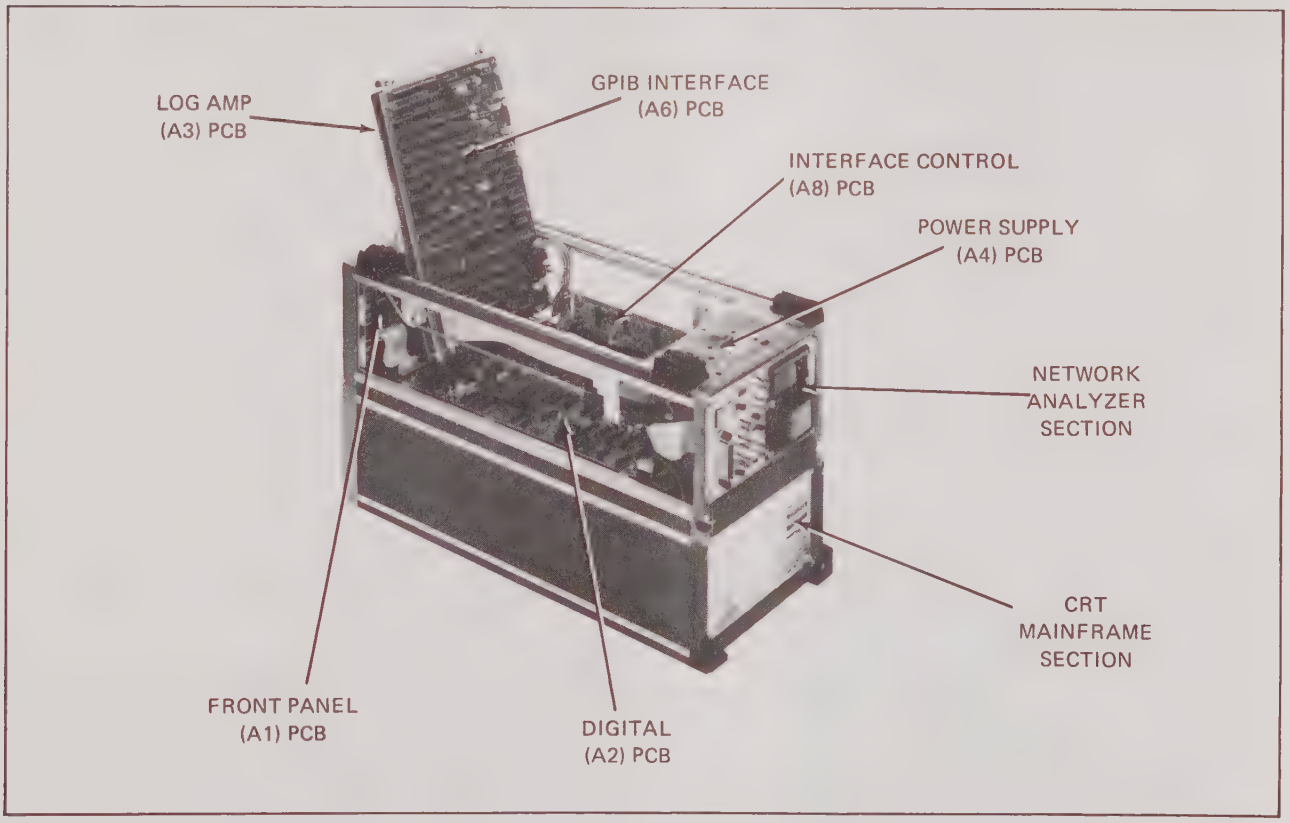


Figure 7-1. Vertical Chassis With Network Analyzer Exposed

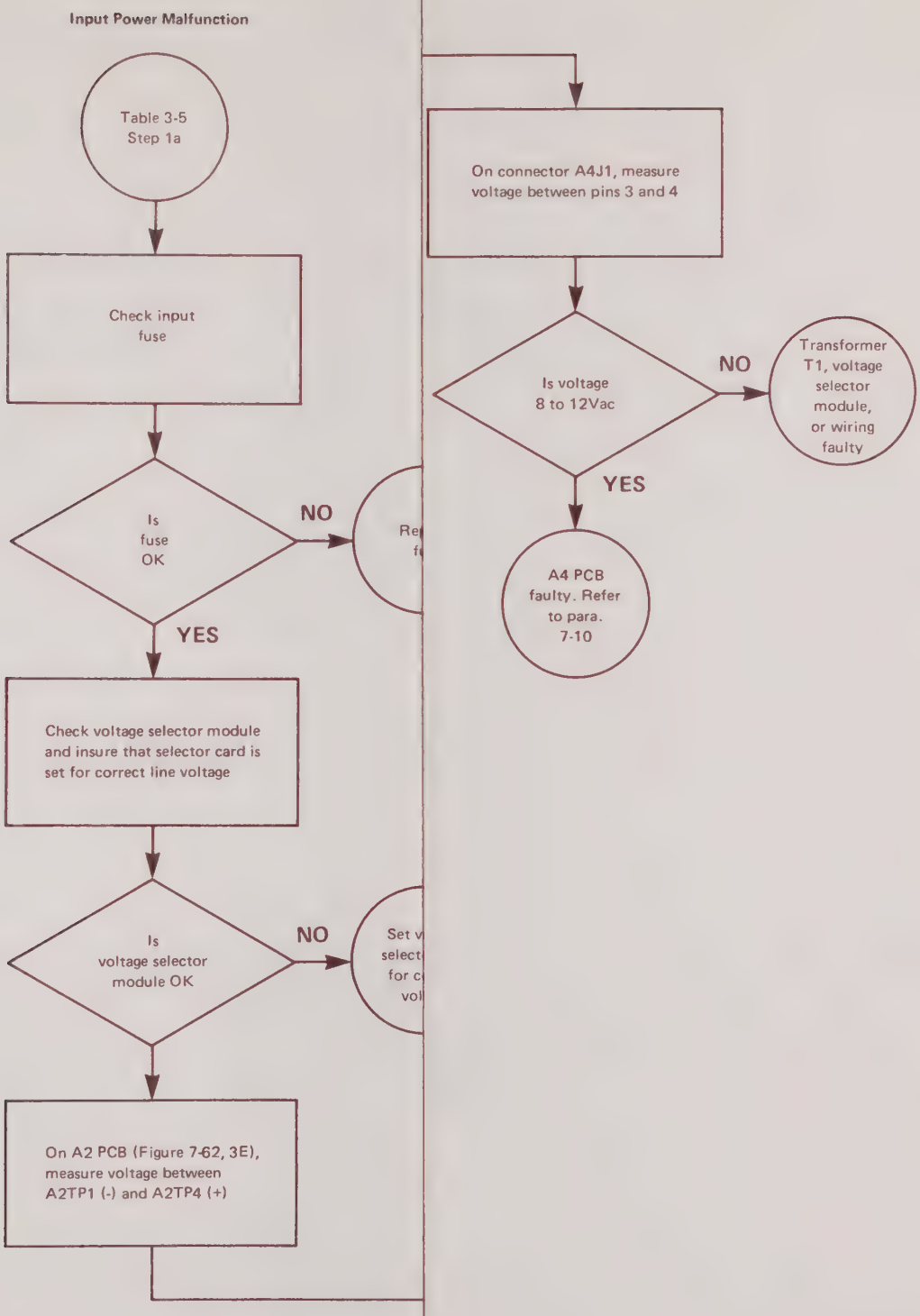


Figure 7-2. Troubleshooting Chart, Input Power Malfunction

where necessary, logical troubleshooting flow charts. Table 3-5, provides the format for using front panel controls to troubleshoot to a malfunctioning PCB. In many cases the malfunctioning PCB is identified in the table's "If Indication Abnormal" column. In cases where further troubleshooting is necessary, however, the troubleshooting flow charts in Figures 7-2 thru 7-17 are provided. Each of these charts relates to a particular step in Table 3-5; the start symbol (top) in each chart indentifies the step number.

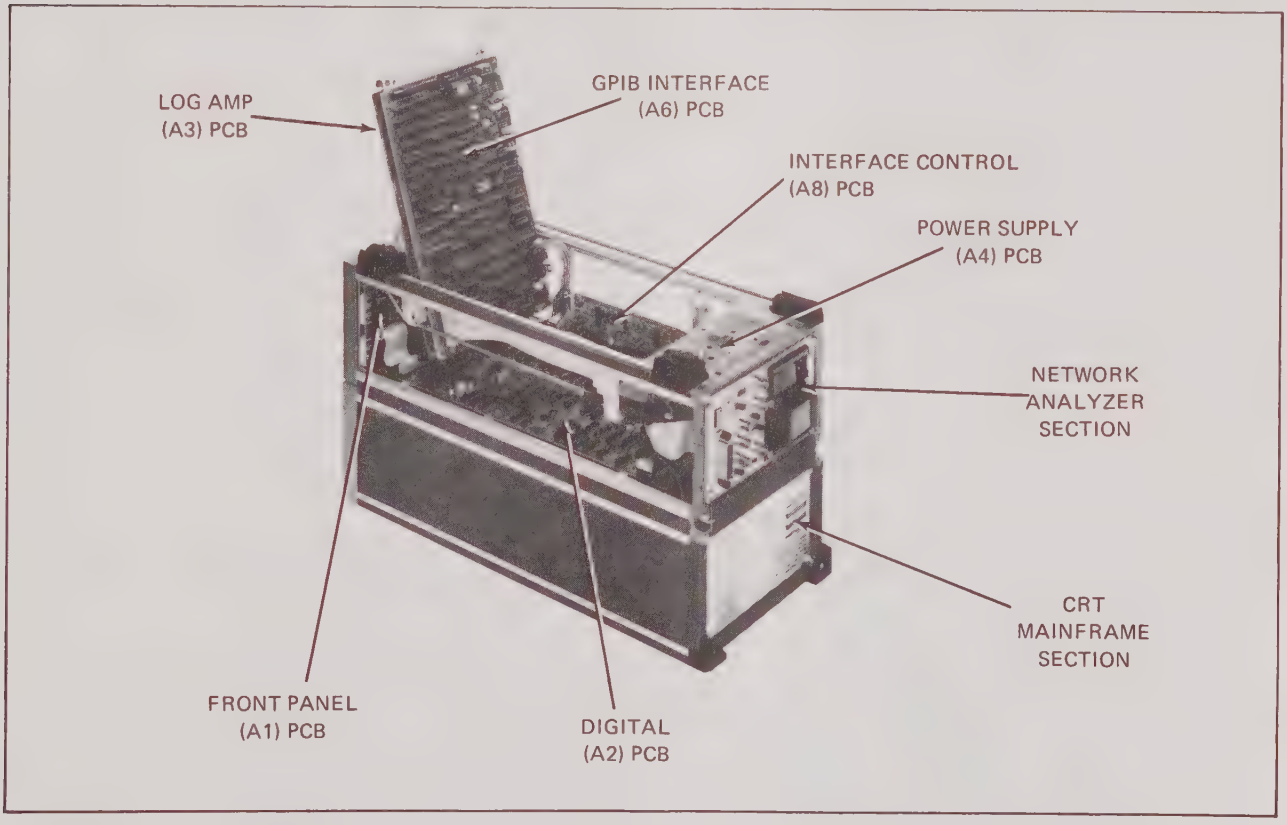
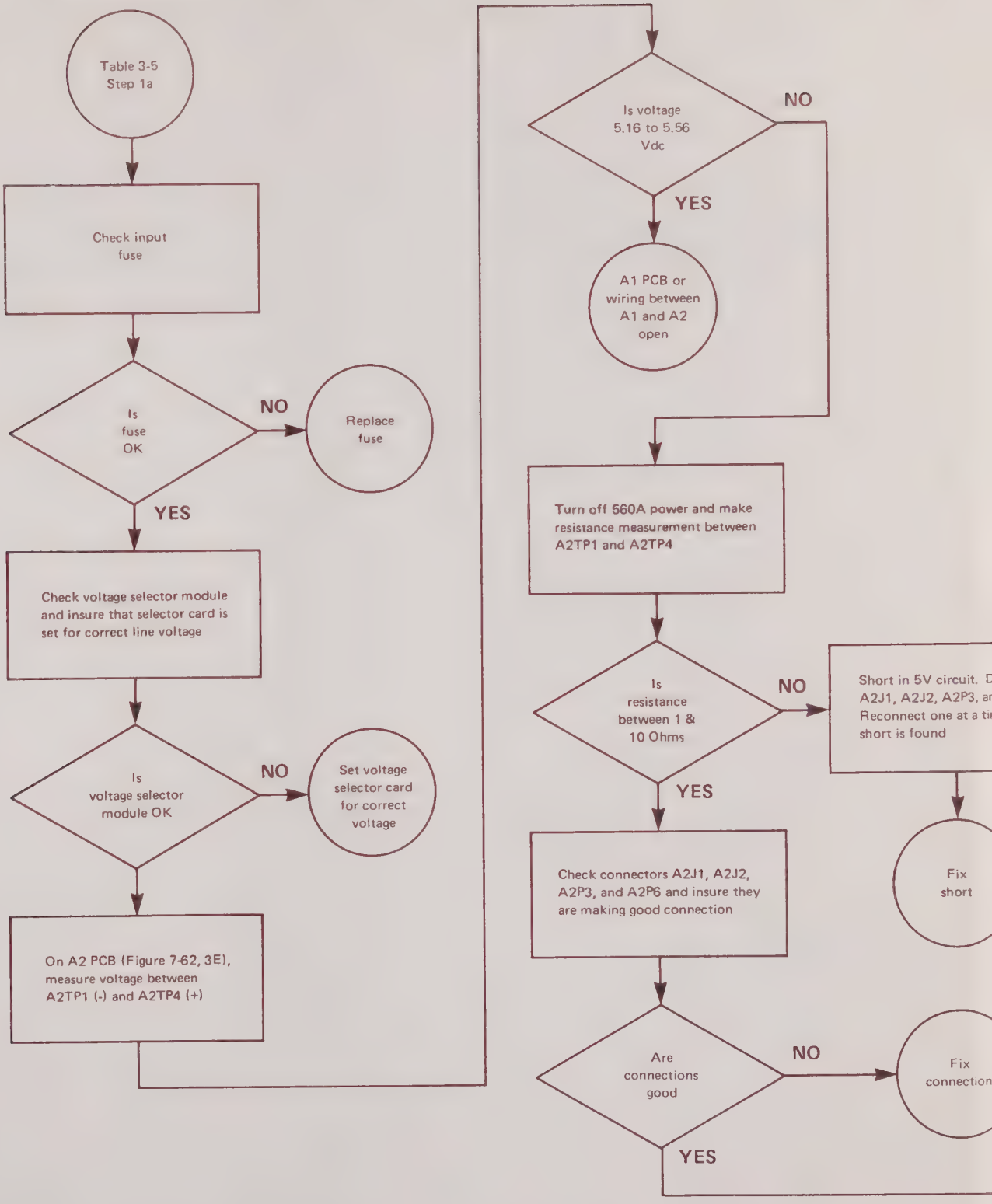


Figure 7-1. Vertical Chassis With Network Analyzer Exposed

Input Power Malfunction



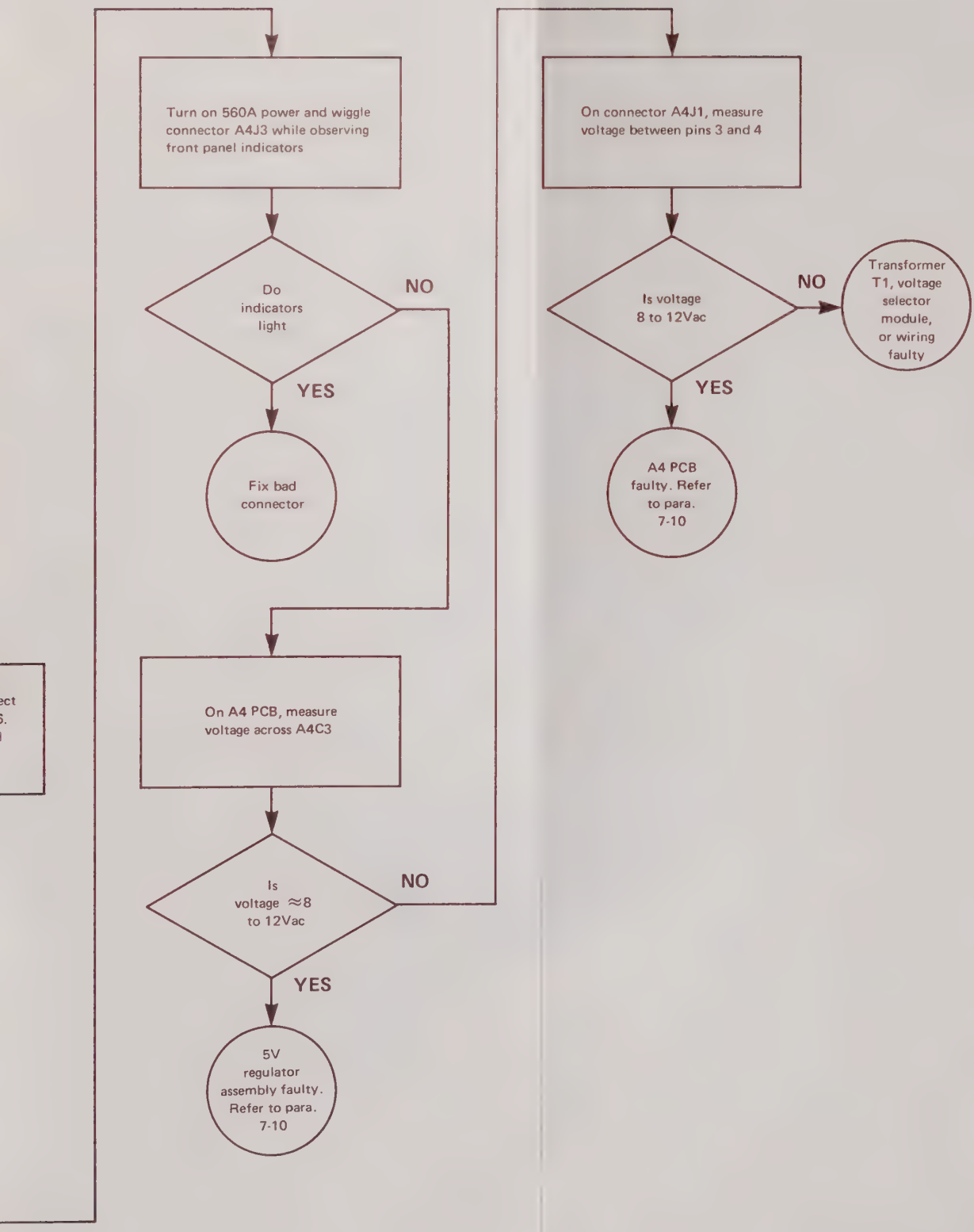

Turn on 560A power and wiggle connector A4J3 while observing front panel indicators
Do indicators light
NO
YES
Fix bad connector
On A4 PCB, measure voltage across A4C3
Is voltage ≈8 to 12Vac
NO
YES
5V regulator assembly faulty. Refer to para. 7-10
On connector A4J1, measure voltage between pins 3 and 4
Is voltage 8 to 12Vac
NO
YES
Transformer T1, voltage selector module, or wiring faulty
A4 PCB faulty. Refer to para. 7-10

Figure 7-2. Troubleshooting Chart, Input Power Malfunction

Channel A Horizontal Trace Malfunction

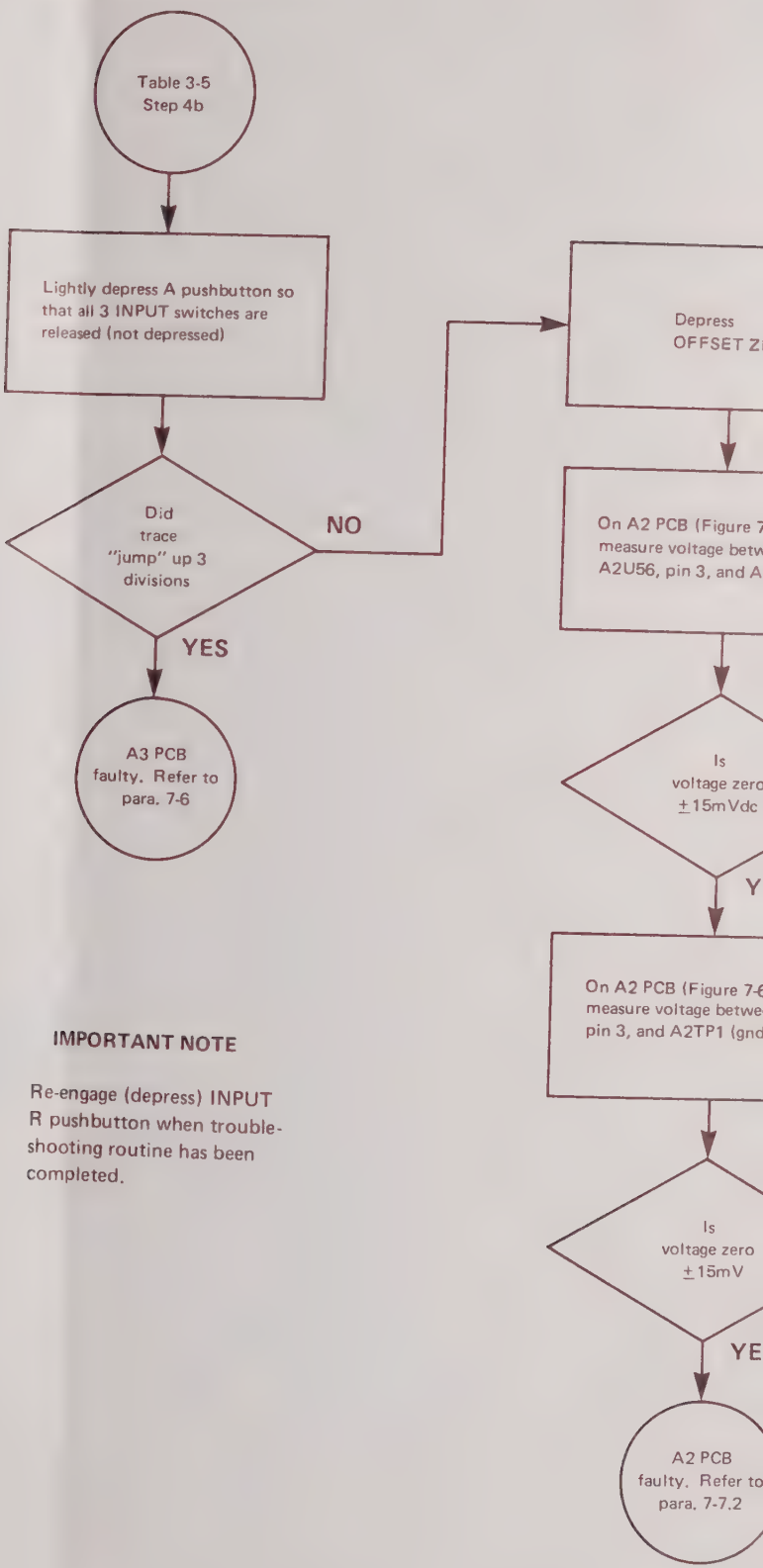


Table 3-5
Step 4b
Lightly depress A pushbutton so that all 3 INPUT switches are released (not depressed)
Did trace "jump" up 3 divisions
NO
YES
A3 PCB faulty. Refer to para. 7-6
Depress OFFSET Z
On A2 PCB (Figure 7
measure voltage betw
A2U56, pin 3, and A
Is voltage zero ±15mVdc
Y
On A2 PCB (Figure 7-6
measure voltage betwe
pin 3, and A2TP1 (gnd
Is voltage zero ±15mV
YE
A2 PCB faulty. Refer to
para. 7-7.2

IMPORTANT NOTE

Re-engage (depress) INPUT R pushbutton when trouble-shooting routine has been completed.

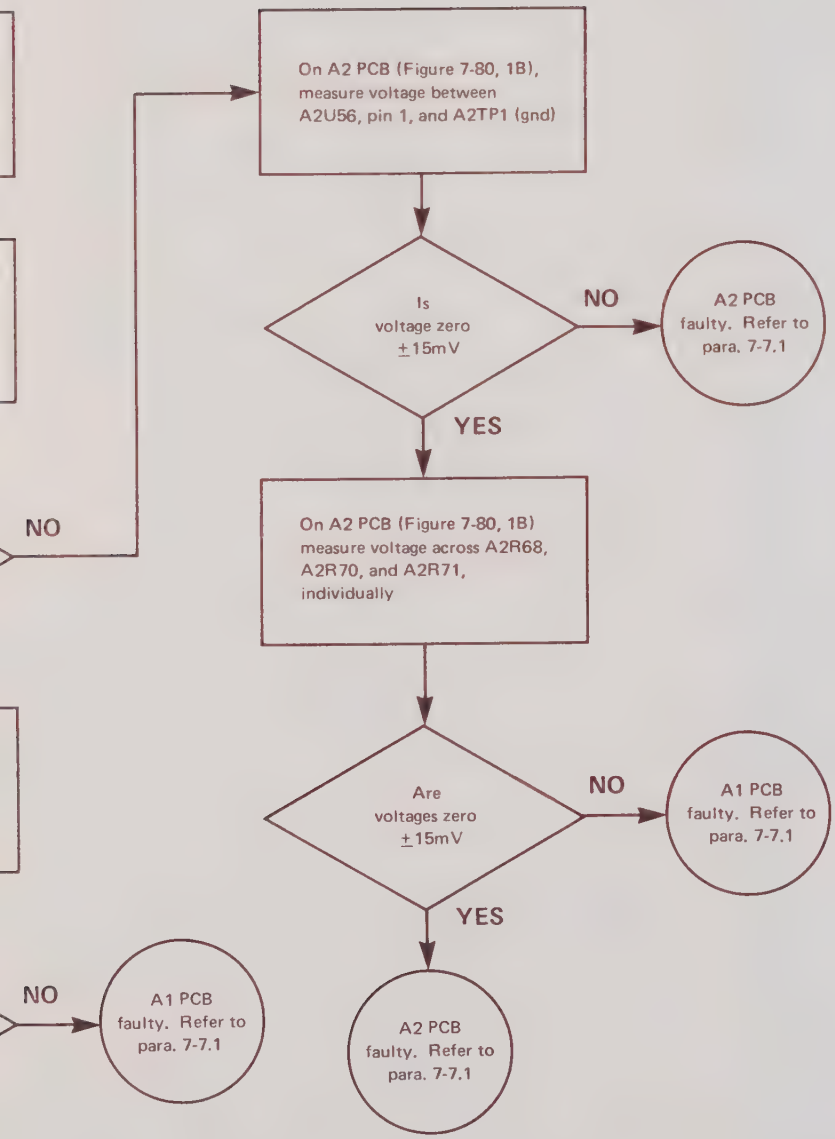

On A2 PCB (Figure 7-80, 1B), measure voltage between A2U56, pin 1, and A2TP1 (gnd)
Is voltage zero ±15mV
NO
A2 PCB faulty. Refer to para. 7-7.1
YES
On A2 PCB (Figure 7-80, 1B) measure voltage across A2R68, A2R70, and A2R71, individually
Are voltages zero ±15mV
NO
A1 PCB faulty. Refer to para. 7-7.1
YES
A2 PCB faulty. Refer to para. 7-7.1
NO
A1 PCB faulty. Refer to para. 7-7.1
NO

Figure 7-3. Troubleshooting Chart, Channel A Horizontal Trace Malfunction

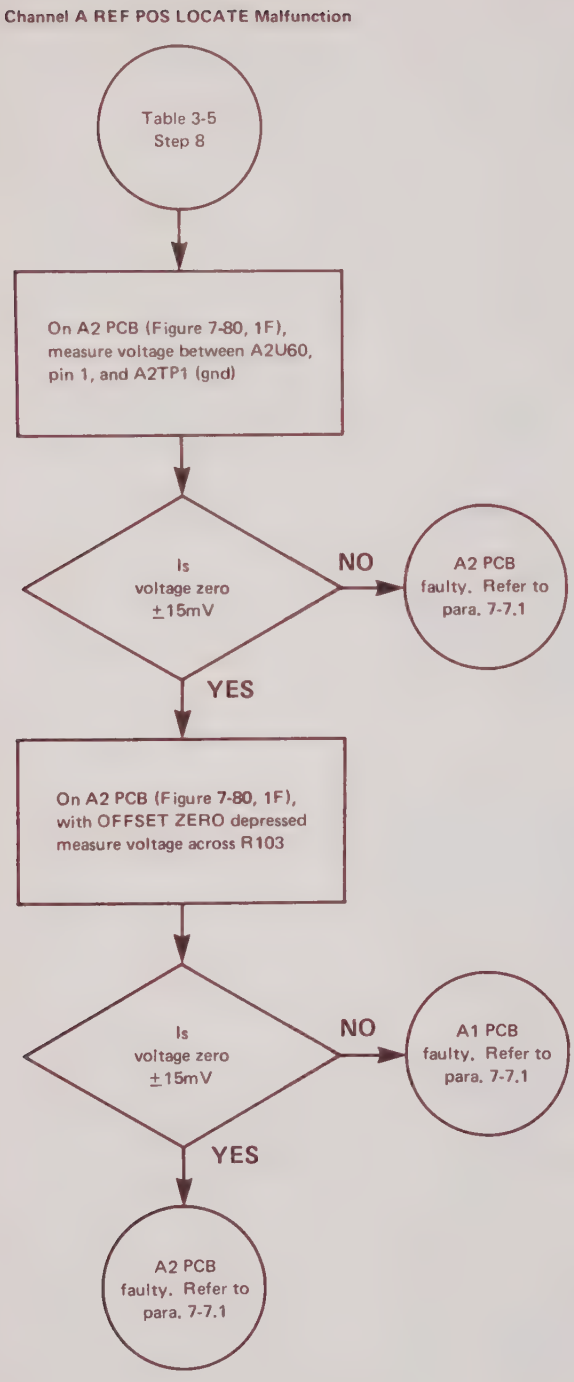


Figure 7-4. Troubleshooting Chart, Channel A REF POS LOCATE Malfunction

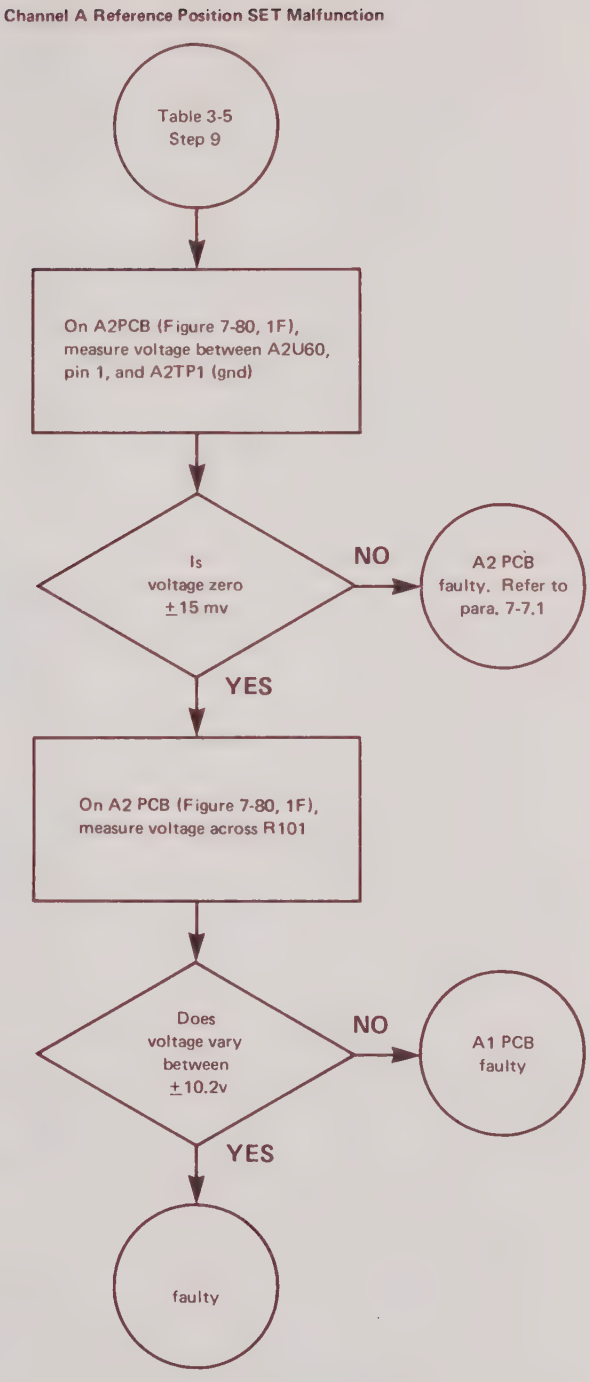


Figure 7-5. Troubleshooting Chart, Channel A Reference Position SET Malfunction

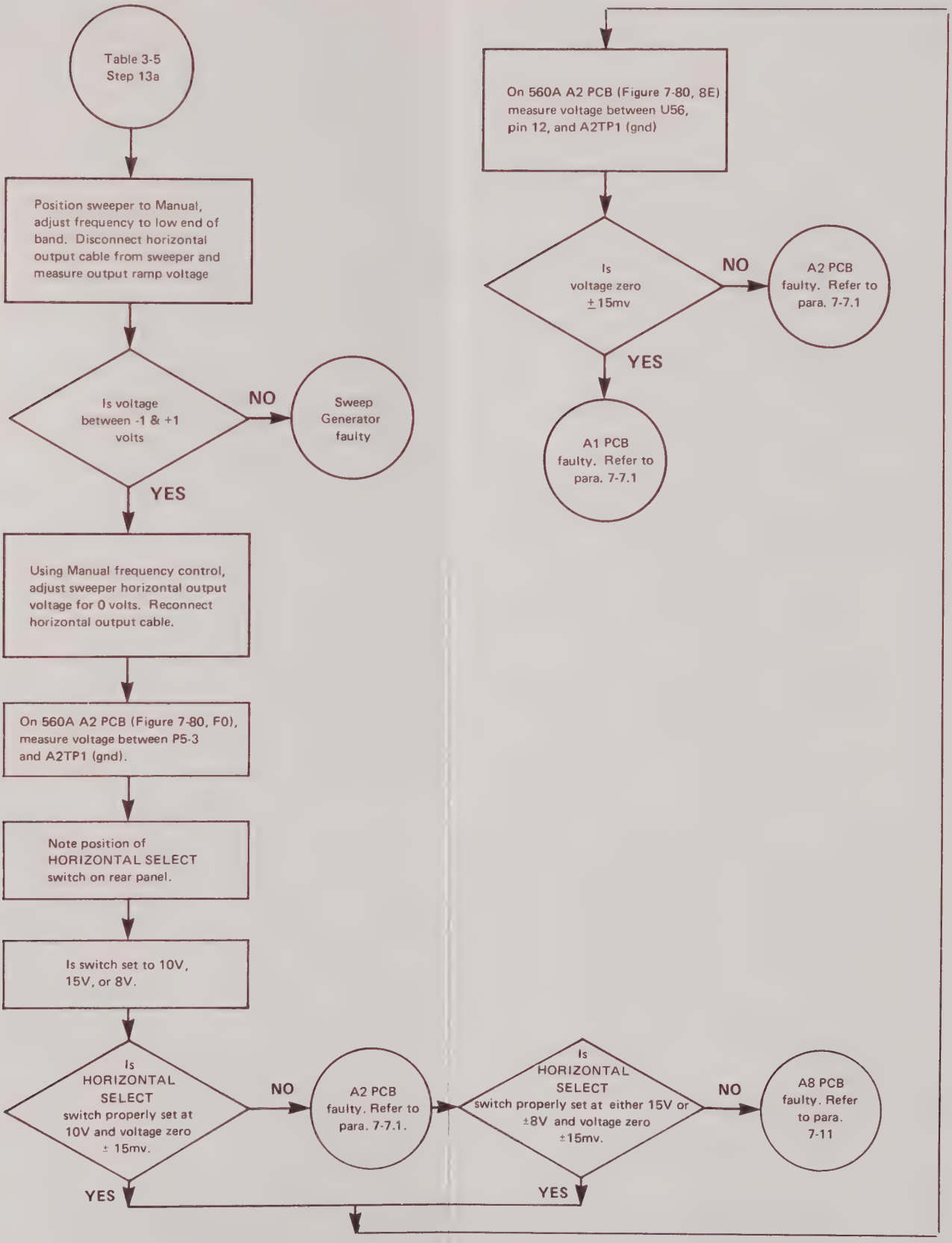


Table 3-5
Step 13a
Position sweeper to Manual, adjust frequency to low end of band. Disconnect horizontal output cable from sweeper and measure output ramp voltage
Is voltage between -1 & +1 volts
NO
Sweep Generator faulty
YES
Using Manual frequency control, adjust sweeper horizontal output voltage for 0 volts. Reconnect horizontal output cable.
On 560A A2 PCB (Figure 7-80, F0), measure voltage between P5-3 and A2TP1 (gnd).
Note position of HORIZONTAL SELECT switch on rear panel.
Is switch set to 10V, 15V, or 8V.
Is HORIZONTAL SELECT switch properly set at 10V and voltage zero ± 15mv.
NO
A2 PCB faulty. Refer to para. 7-7.1.
YES
On 560A A2 PCB (Figure 7-80, 8E) measure voltage between U56, pin 12, and A2TP1 (gnd)
Is voltage zero ±15mv
NO
A2 PCB faulty. Refer to para. 7-7.1
YES
A1 PCB faulty. Refer to para. 7-7.1
Is HORIZONTAL SELECT switch properly set at either 15V or ±8V and voltage zero ±15mv.
NO
A8 PCB faulty. Refer to para. 7-11
YES

Figure 7-6. Troubleshooting Chart, HORIZ START Malfunction

Figure 7-4.
Figure 7-5.

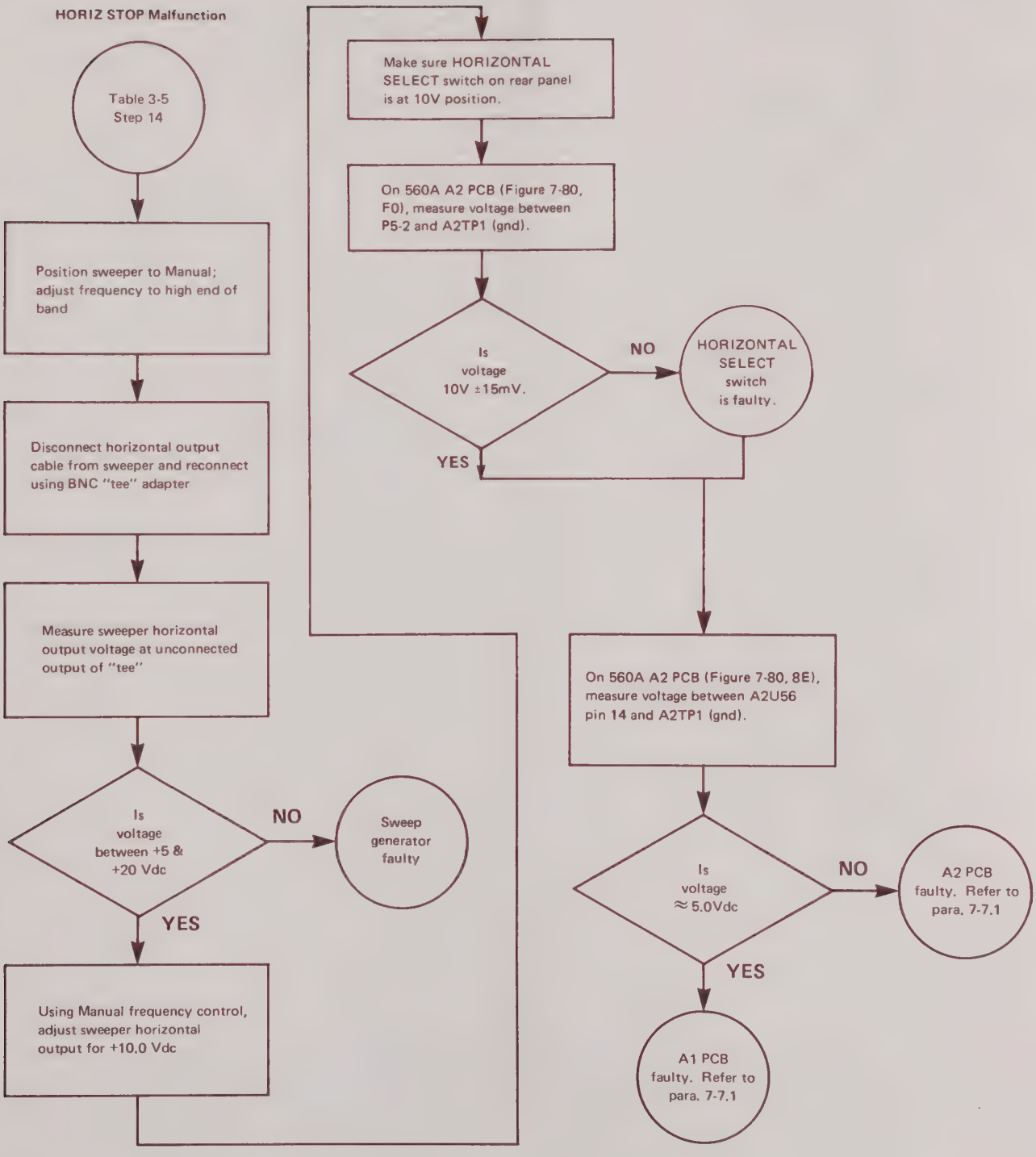

HORIZ STOP Malfunction
Table 3-5 Step 14
Position sweeper to Manual; adjust frequency to high end of band
Disconnect horizontal output cable from sweeper and reconnect using BNC "tee" adapter
Measure sweeper horizontal output voltage at unconnected output of "tee"
Is voltage between +5 & +20 Vdc
NO
Sweep generator faulty
YES
Using Manual frequency control, adjust sweeper horizontal output for +10.0 Vdc
Make sure HORIZONTAL SELECT switch on rear panel is at 10V position.
On 560A A2 PCB (Figure 7-80, F0), measure voltage between P5-2 and A2TP1 (gnd).
Is voltage 10V ±15mV.
NO
HORIZONTAL SELECT switch is faulty.
YES
On 560A A2 PCB (Figure 7-80, 8E), measure voltage between A2U56 pin 14 and A2TP1 (gnd).
Is voltage ≈ 5.0Vdc
NO
A2 PCB faulty. Refer to para. 7-7.1
YES
A1 PCB faulty. Refer to para. 7-7.1

Figure 7-7. Troubleshooting Chart, HORIZ STOP Malfunction

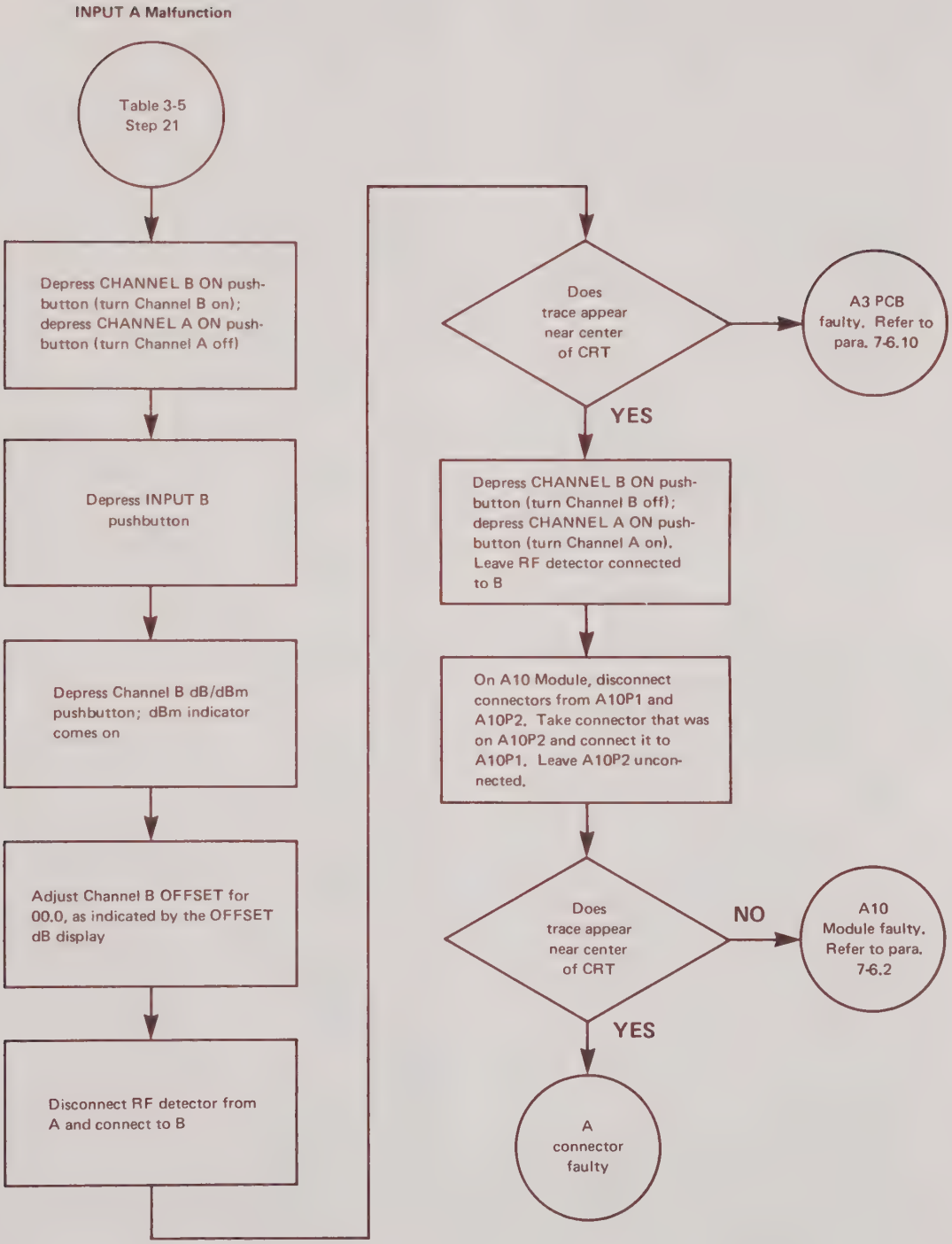

INPUT A Malfunction
Table 3-5 Step 21
Depress CHANNEL B ON push-button (turn Channel B on); depress CHANNEL A ON push-button (turn Channel A off)
Depress INPUT B pushbutton
Depress Channel B dB/dBm pushbutton; dBm indicator comes on
Adjust Channel B OFFSET for 00.0, as indicated by the OFFSET dB display
Disconnect RF detector from A and connect to B
Does trace appear near center of CRT
A3 PCB faulty. Refer to para. 7-6.10
YES
Depress CHANNEL B ON push-button (turn Channel B off); depress CHANNEL A ON push-button (turn Channel A on). Leave RF detector connected to B
On A10 Module, disconnect connectors from A10P1 and A10P2. Take connector that was on A10P2 and connect it to A10P1. Leave A10P2 unconnected.
Does trace appear near center of CRT
NO
A10 Module faulty. Refer to para. 7-6.2
YES
A connector faulty

Figure 7-8. Troubleshooting Chart, INPUT A Malfunction

Figure 7-7.

Channel B Horizontal Trace Malfunction

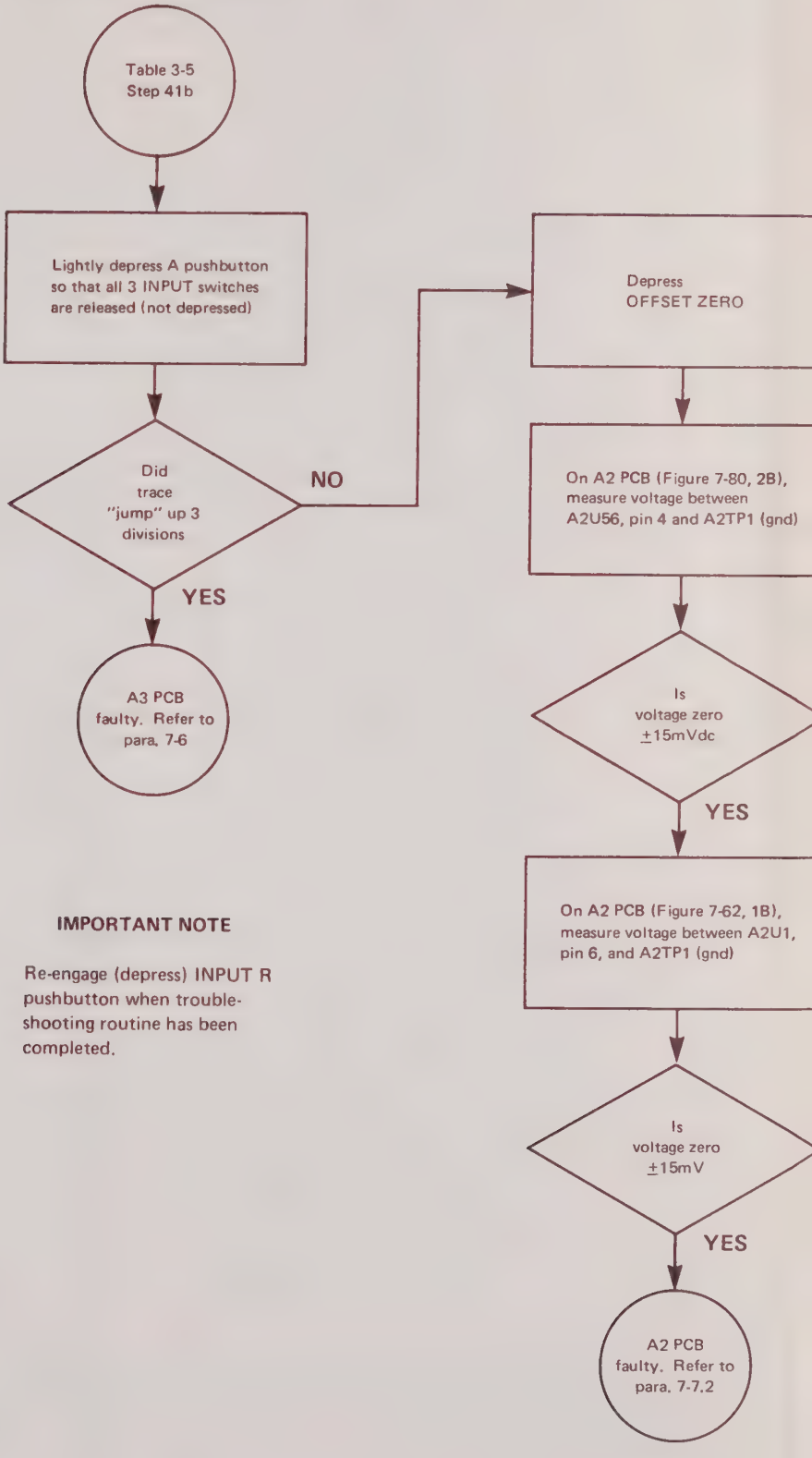


Table 3-5
Step 41b
Lightly depress A pushbutton so that all 3 INPUT switches are released (not depressed)
Did trace "jump" up 3 divisions
NO
YES
A3 PCB faulty. Refer to para. 7-6
Depress OFFSET ZERO
On A2 PCB (Figure 7-80, 2B), measure voltage between A2U56, pin 4 and A2TP1 (gnd)
Is voltage zero ±15mVdc
YES
On A2 PCB (Figure 7-62, 1B), measure voltage between A2U1, pin 6, and A2TP1 (gnd)
Is voltage zero ±15mV
YES
A2 PCB faulty. Refer to para. 7-7.2

IMPORTANT NOTE

Re-engage (depress) INPUT R pushbutton when trouble-shooting routine has been completed.

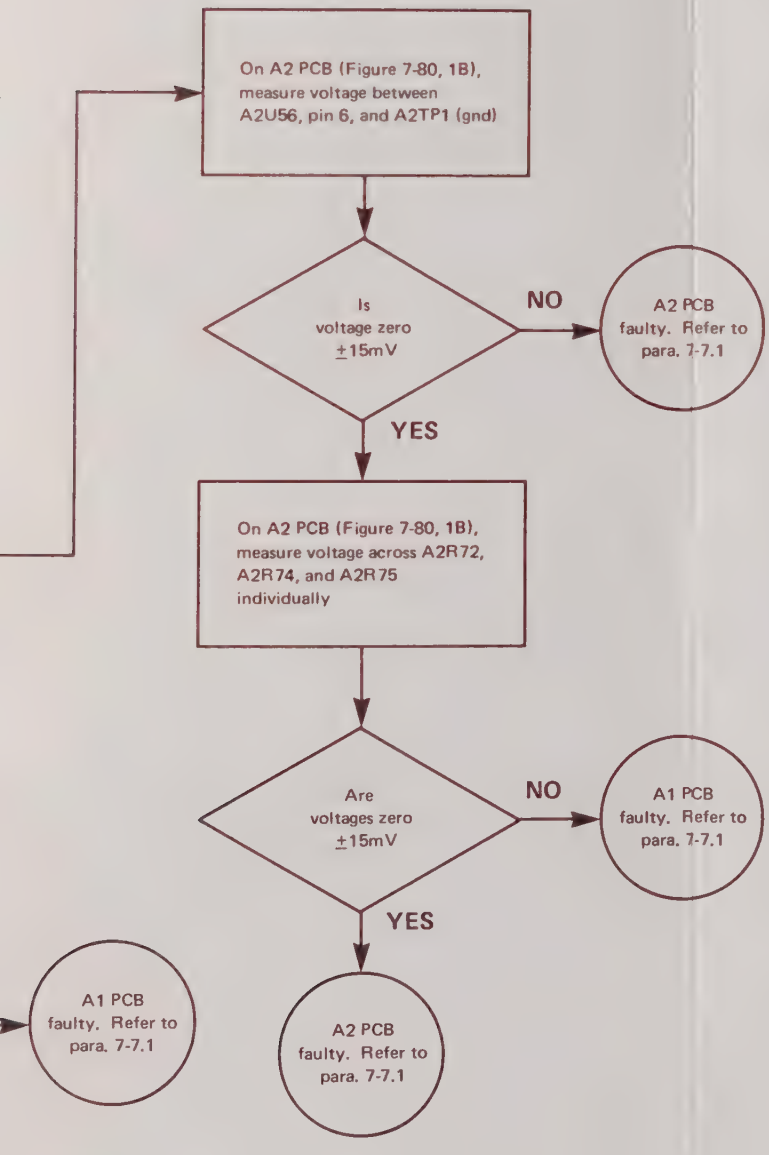

On A2 PCB (Figure 7-80, 1B), measure voltage between A2U56, pin 6, and A2TP1 (gnd)
Is voltage zero ±15mV
NO
A2 PCB faulty. Refer to para. 7-7.1
YES
On A2 PCB (Figure 7-80, 1B), measure voltage across A2R72, A2R74, and A2R75 individually
Are voltages zero ±15mV
NO
A1 PCB faulty. Refer to para. 7-7.1
YES
A2 PCB faulty. Refer to para. 7-7.1
A1 PCB faulty. Refer to para. 7-7.1

Figure 7-9. Troubleshooting Chart, Channel B Horizontal Trace Malfunction

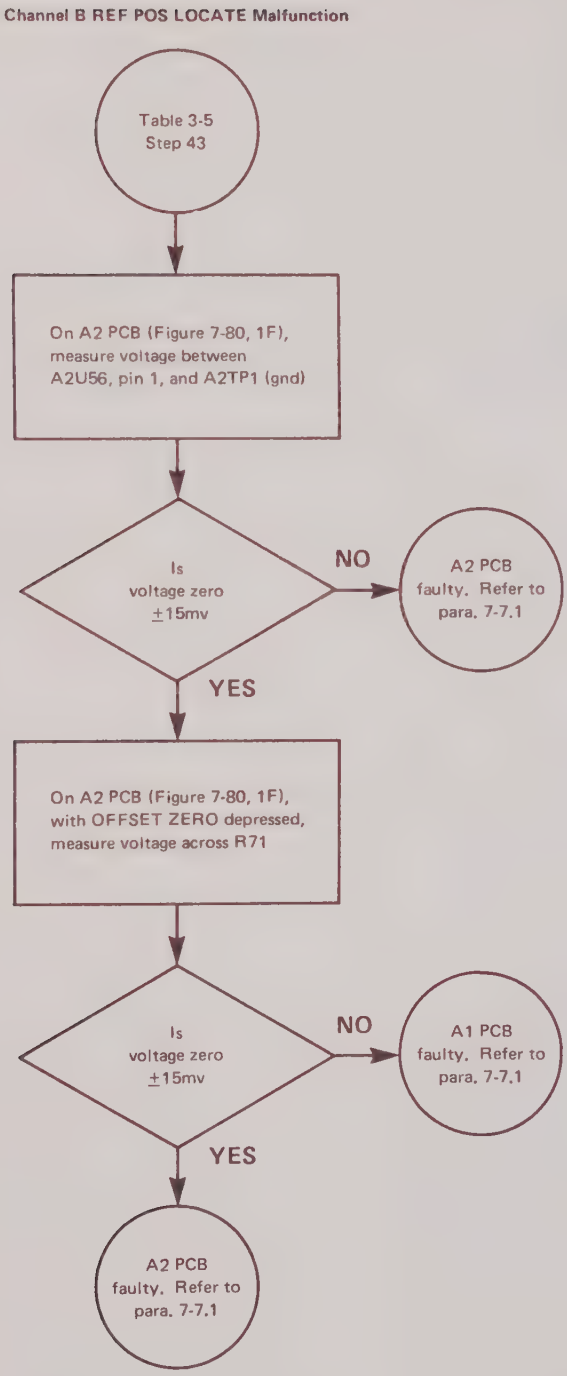


Figure 7-10. Troubleshooting Chart, Channel B REF POS LOCATE Malfunction

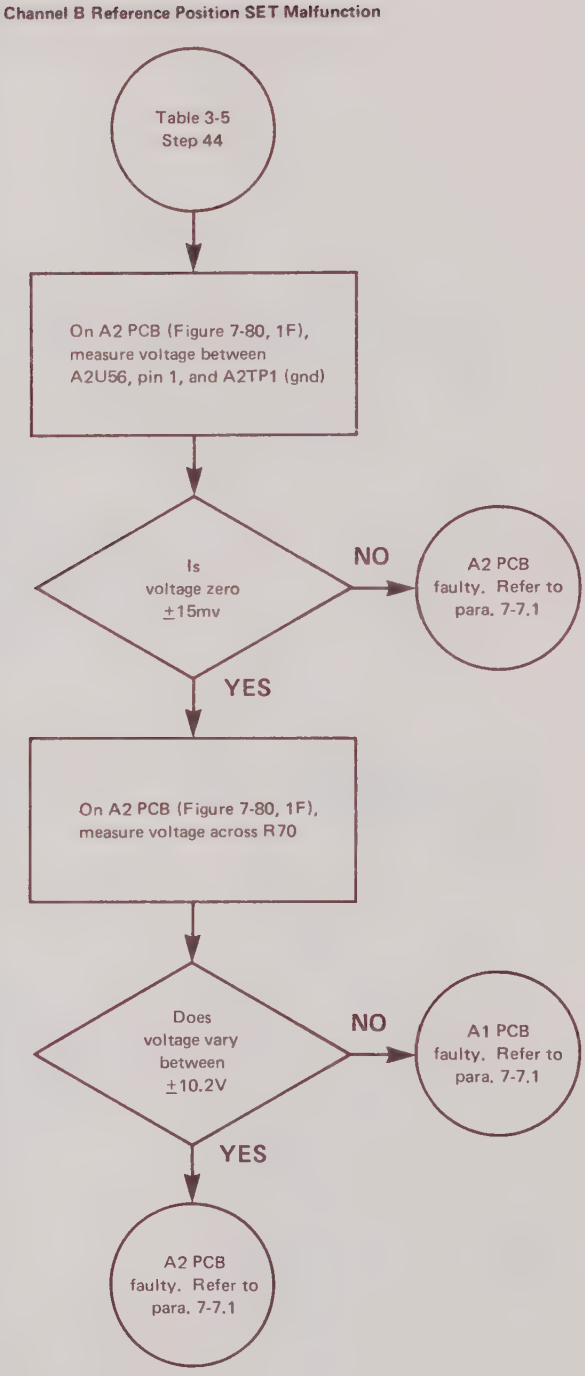


Figure 7-11. Troubleshooting Chart, Channel B Reference Position SET Malfunction

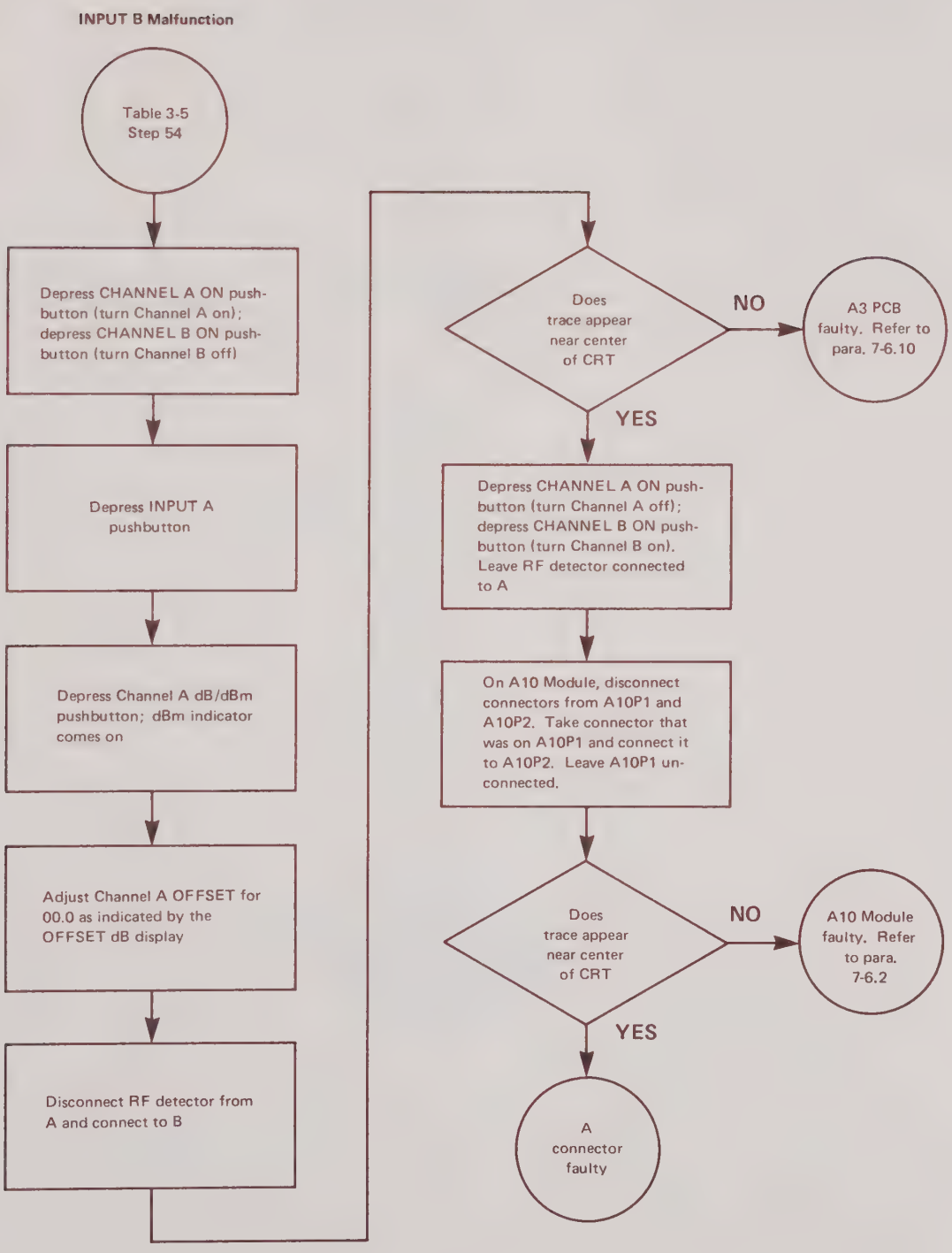

INPUT B Malfunction
Table 3-5 Step 54
Depress CHANNEL A ON push-button (turn Channel A on); depress CHANNEL B ON push-button (turn Channel B off)
Depress INPUT A pushbutton
Depress Channel A dB/dBm pushbutton; dBm indicator comes on
Adjust Channel A OFFSET for 00.0 as indicated by the OFFSET dB display
Disconnect RF detector from A and connect to B
Does trace appear near center of CRT
NO
A3 PCB faulty. Refer to para. 7-6.10
YES
Depress CHANNEL A ON push-button (turn Channel A off); depress CHANNEL B ON push-button (turn Channel B on). Leave RF detector connected to A
On A10 Module, disconnect connectors from A10P1 and A10P2. Take connector that was on A10P1 and connect it to A10P2. Leave A10P1 un-connected.
Does trace appear near center of CRT
NO
A10 Module faulty. Refer to para. 7-6.2
YES
A connector faulty

Figure 7-12. Troubleshooting Chart, INPUT B Malfunction

Figure 7-10.
Figure 7-11.

Marker Malfunction WILTRON 6600 Series

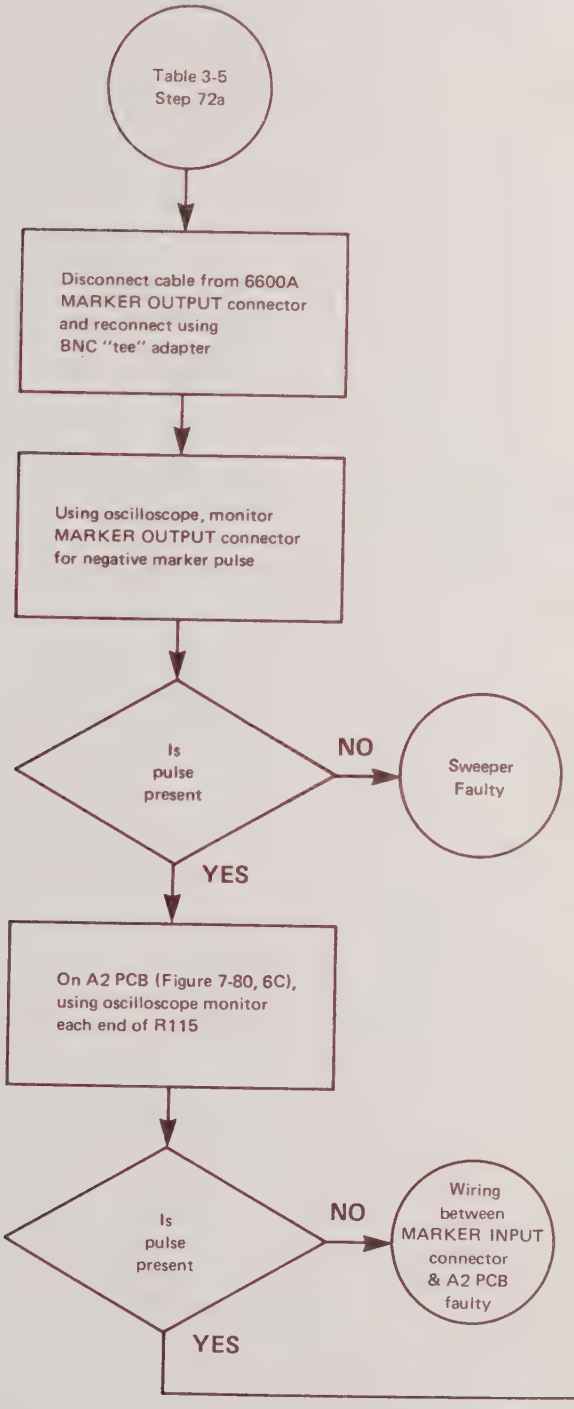


Table 3-5
Step 72a
Disconnect cable from 6600A MARKER OUTPUT connector and reconnect using BNC "tee" adapter
Using oscilloscope, monitor MARKER OUTPUT connector for negative marker pulse
Is pulse present
NO
Sweeper Faulty
YES
On A2 PCB (Figure 7-80, 6C), using oscilloscope monitor each end of R115
Is pulse present
NO
Wiring between MARKER INPUT connector & A2 PCB faulty
YES

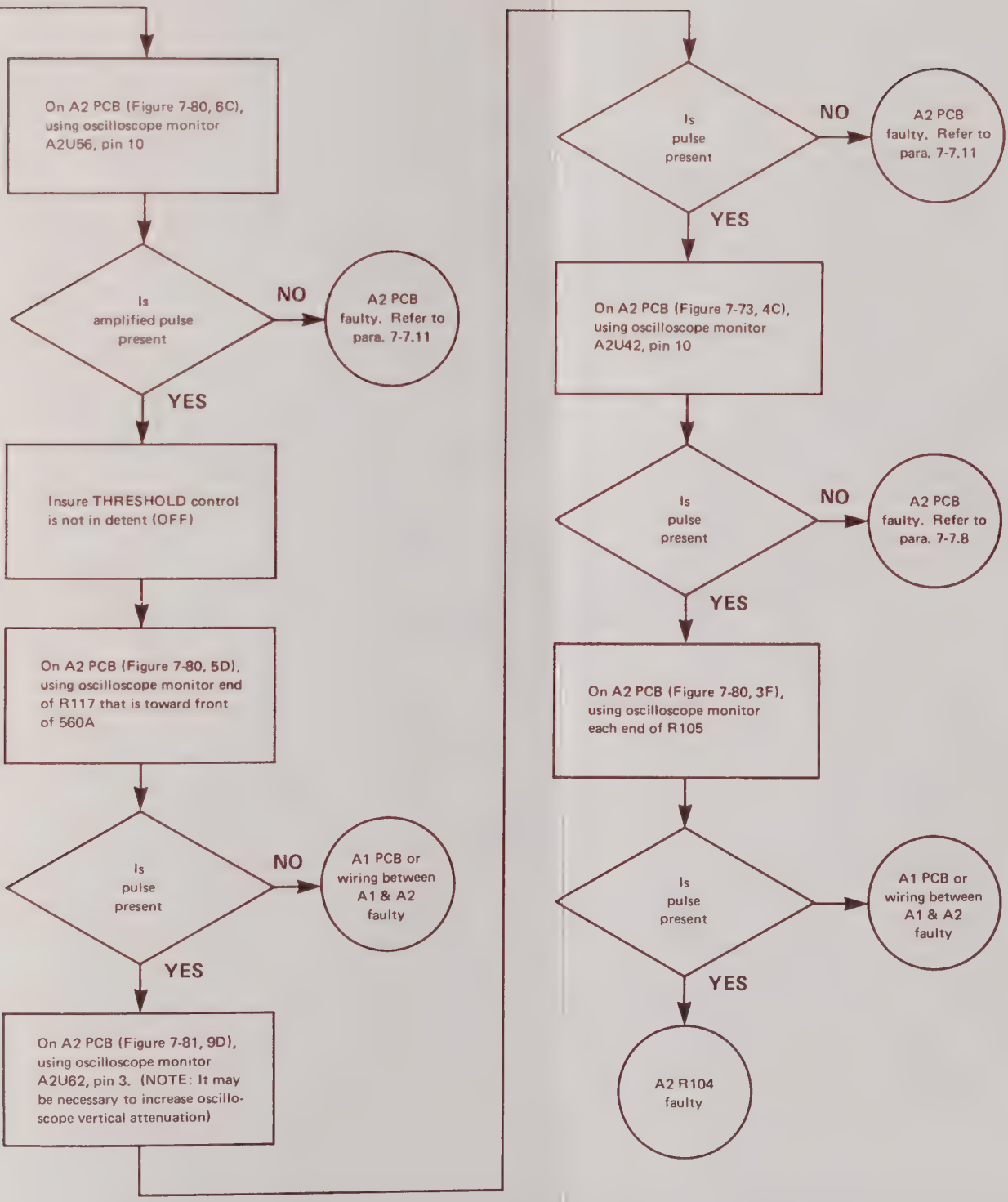

On A2 PCB (Figure 7-80, 6C), using oscilloscope monitor A2U56, pin 10
Is amplified pulse present
NO
A2 PCB faulty. Refer to para. 7-7.11
YES
Insure THRESHOLD control is not in detent (OFF)
On A2 PCB (Figure 7-80, 5D), using oscilloscope monitor end of R117 that is toward front of 560A
Is pulse present
NO
A1 PCB or wiring between A1 & A2 faulty
YES
On A2 PCB (Figure 7-81, 9D), using oscilloscope monitor A2U62, pin 3. (NOTE: It may be necessary to increase oscilloscope vertical attenuation)
Is pulse present
NO
A2 PCB faulty. Refer to para. 7-7.11
YES
On A2 PCB (Figure 7-73, 4C), using oscilloscope monitor A2U42, pin 10
Is pulse present
NO
A2 PCB faulty. Refer to para. 7-7.8
YES
On A2 PCB (Figure 7-80, 3F), using oscilloscope monitor each end of R105
Is pulse present
A1 PCB or wiring between A1 & A2 faulty
YES
A2 R104 faulty

Figure 7-13. Troubleshooting Chart, Marker Malfunction (WILTRON Model 6647 used as sweep generator)

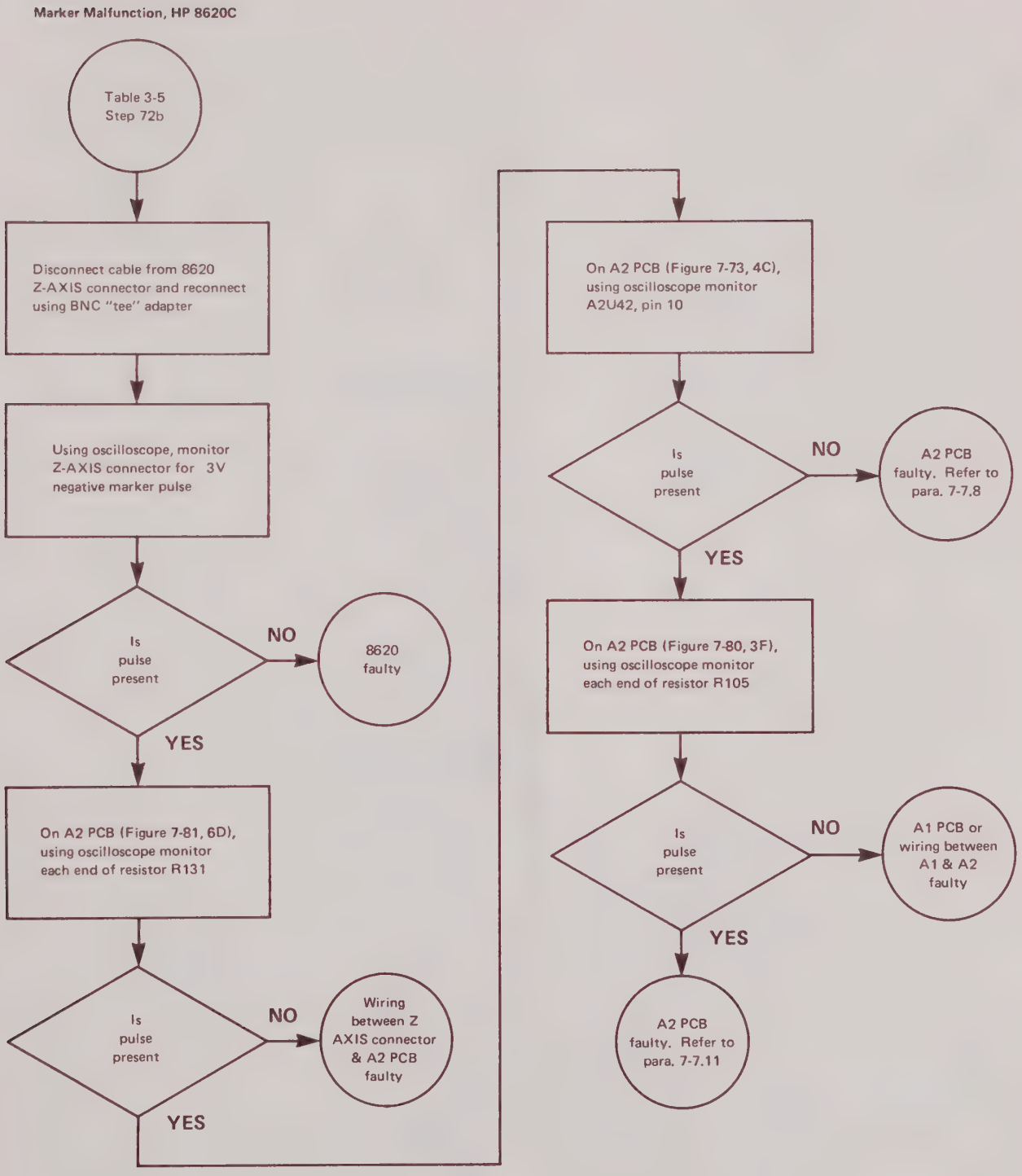


Figure 7-14. Troubleshooting Chart, Marker Malfunction (Hewlett-Packard Model 8620C used as sweep generator)

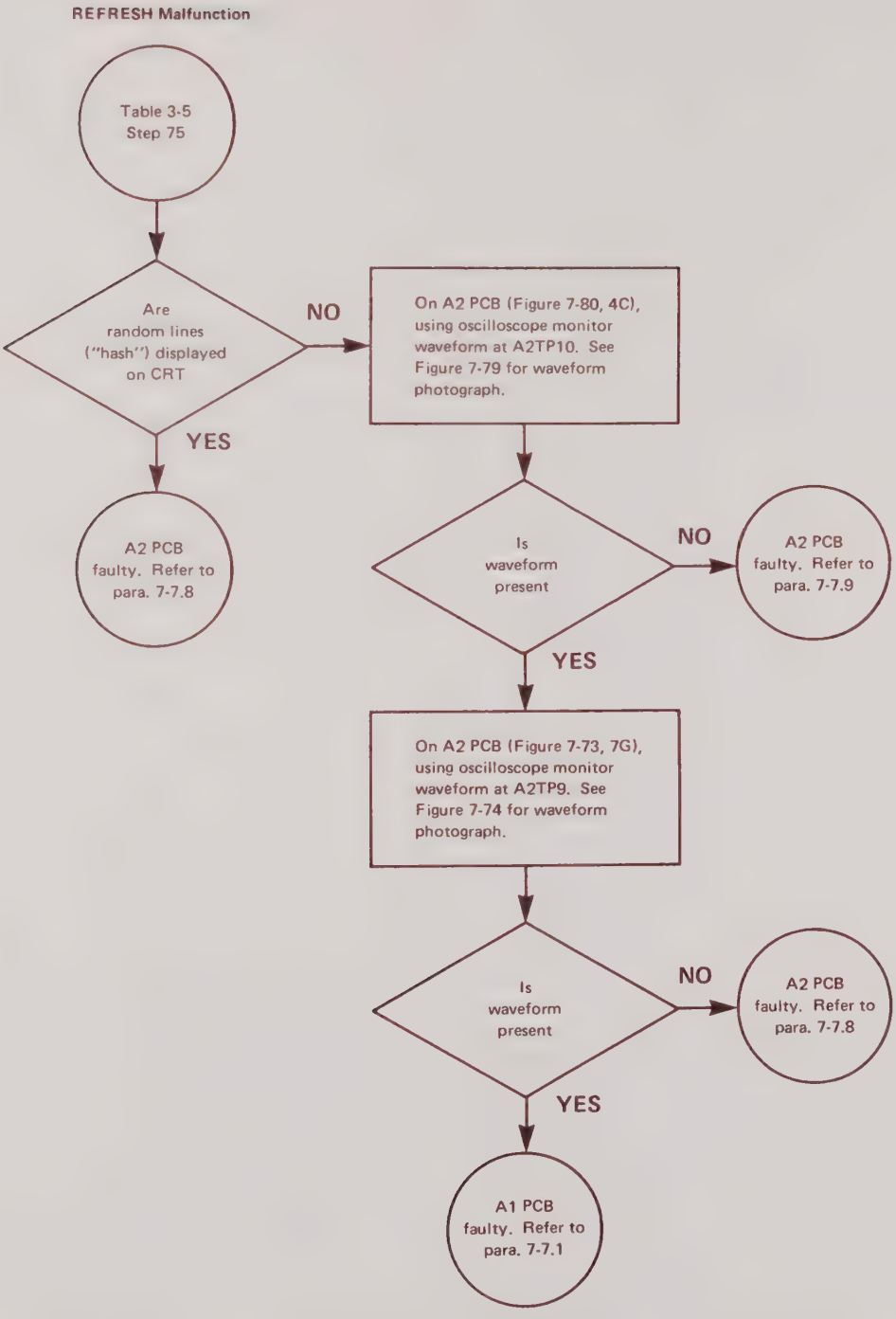


Figure 7-15. Troubleshooting Chart, REFRESH Malfunction

Figure 7-14.

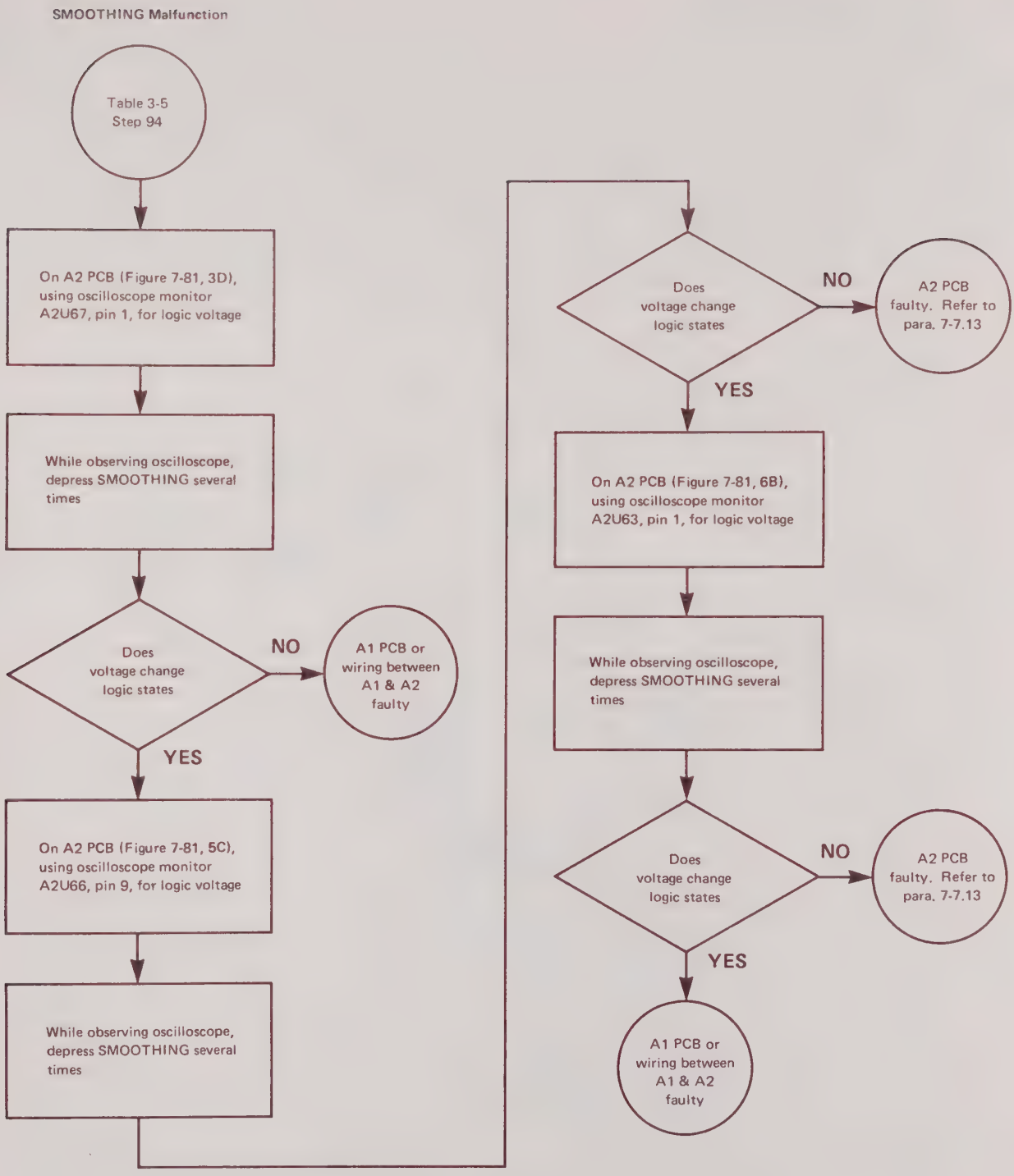

SMOOTHING Malfunction
Table 3-5
Step 94
On A2 PCB (Figure 7-81, 3D), using oscilloscope monitor A2U67, pin 1, for logic voltage
While observing oscilloscope, depress SMOOTHING several times
Does voltage change logic states
NO
A1 PCB or wiring between A1 & A2 faulty
YES
On A2 PCB (Figure 7-81, 5C), using oscilloscope monitor A2U66, pin 9, for logic voltage
While observing oscilloscope, depress SMOOTHING several times
Does voltage change logic states
NO
A2 PCB faulty. Refer to para. 7-7.13
YES
On A2 PCB (Figure 7-81, 6B), using oscilloscope monitor A2U63, pin 1, for logic voltage
While observing oscilloscope, depress SMOOTHING several times
Does voltage change logic states
NO
A2 PCB faulty. Refer to para. 7-7.13
YES
A1 PCB or wiring between A1 & A2 faulty

Figure 7-16. Troubleshooting Chart, SMOOTHING Malfunction

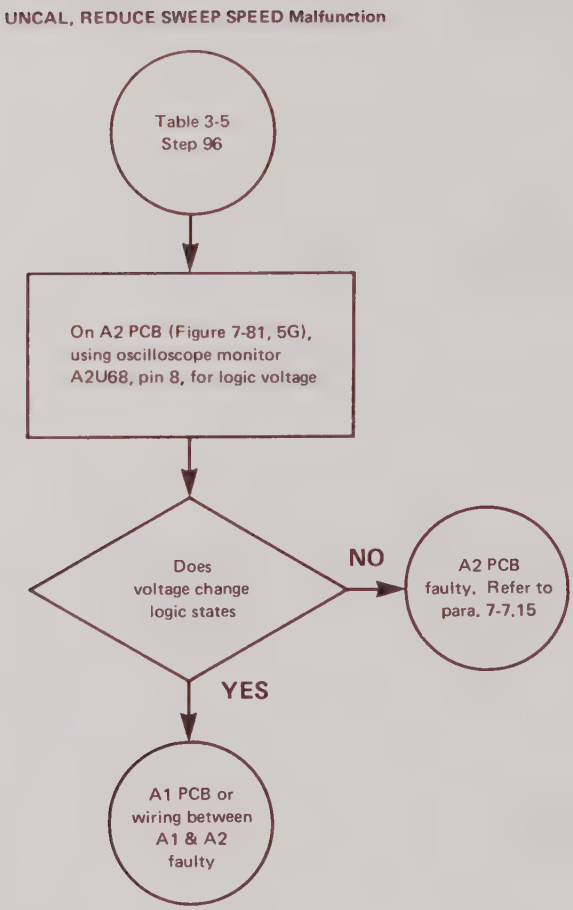


Figure 7-17. Troubleshooting Chart, UNCAL REDUCE SWEEP SPEED Malfunction

7-4 SERVICE INSTRUCTIONS

The service instructions in the following paragraphs contain all of the necessary information - e.g., theory of operation, schematic and block diagrams, parts locator diagrams, and test point voltages and waveforms - to permit troubleshooting to the defective integrated or functional circuit. In its basic configuration the 560A contains four printed circuit boards (PCBs): Front Panel (A1), Digital (A2), Log Amplifier (A3), Power Supply (A4), and Interface Control (A8). In its Option 3 (GPIB) configuration, the 560A contains the GPIB Interface (A6) PCB, in addition to the four PCBs mentioned above. The 560A Option 3 also contains a rear panel GPIB interface connector with its associated PCB. Figure 7-18 provides a block diagram, Figure 7-19 provides an interconnect diagram, and Figure 7-20 provides a power supply voltage distribution diagram of the 560A PCBs.

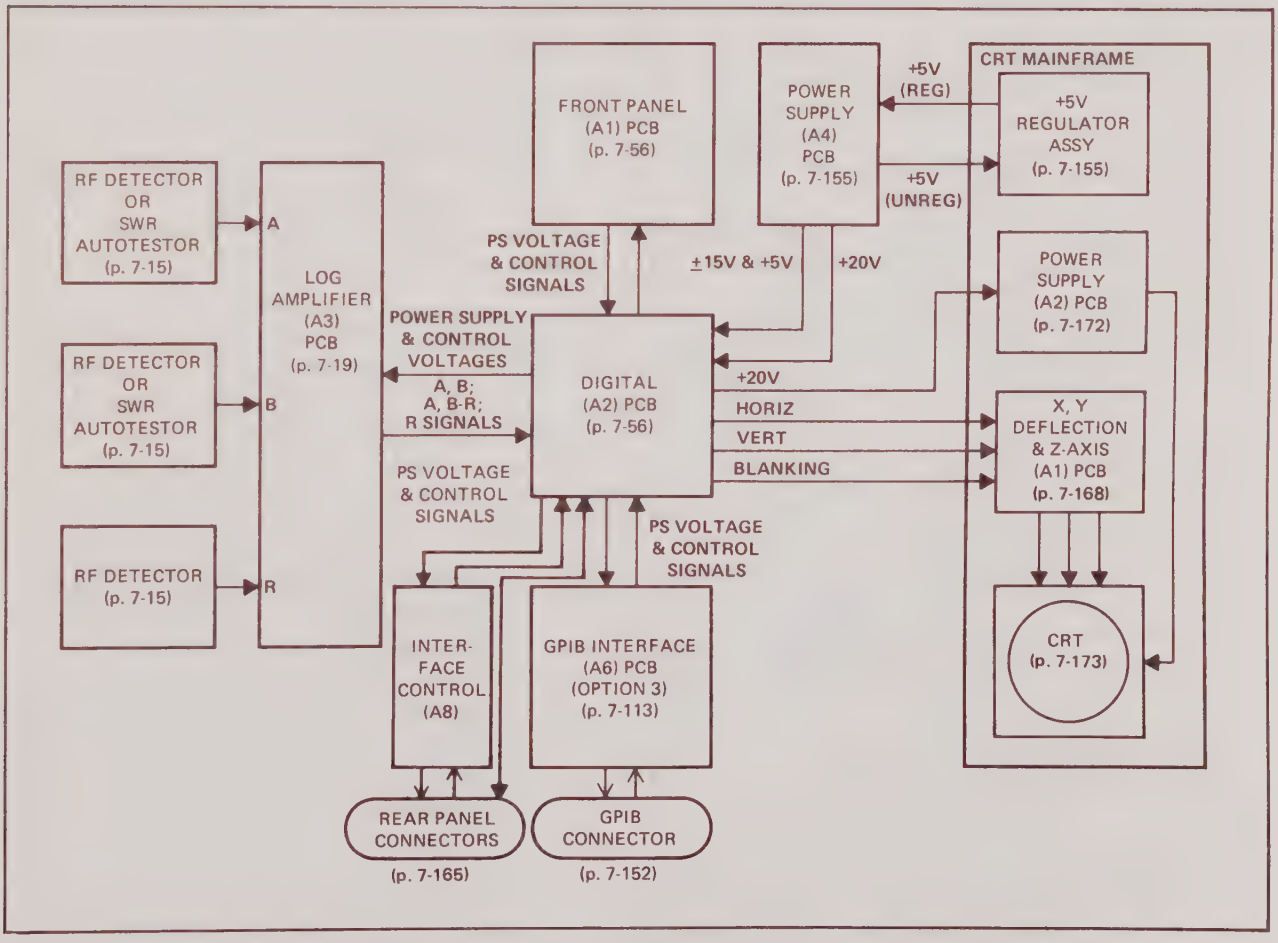
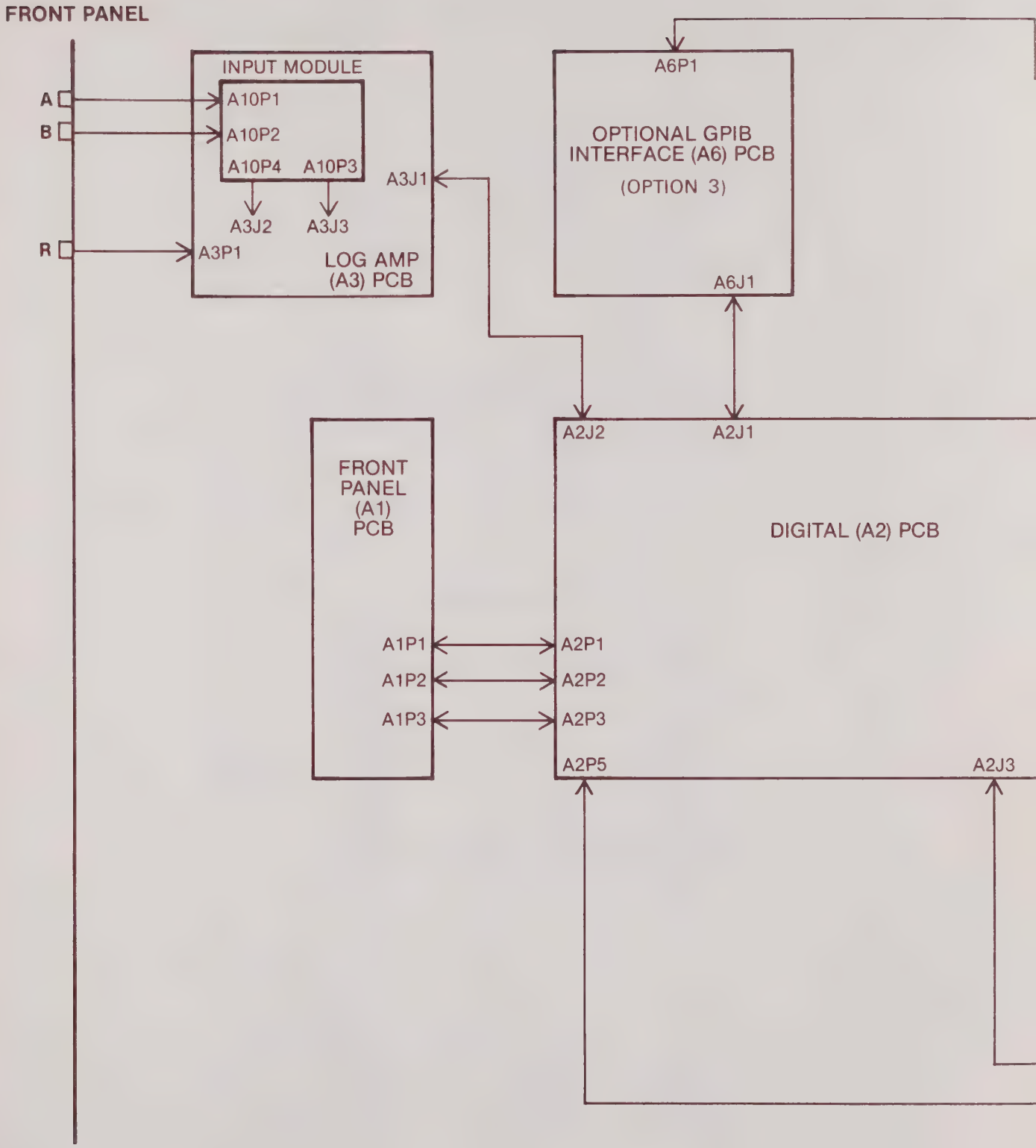


Figure 7-18. 560A Overall Block Diagram


FRONT PANEL
A
B
R
INPUT MODULE
A10P1
A10P2
A10P4
A10P3
A3J2
A3J3
A3P1
A3J1
LOG AMP
(A3) PCB
A6P1
OPTIONAL GPIB
INTERFACE (A6) PCB
(OPTION 3)
A6J1
FRONT
PANEL
(A1)
PCB
A2J2
A2J1
DIGITAL (A2) PCB
A1P1
A1P2
A1P3
A2P1
A2P2
A2P3
A2P5
A2J3

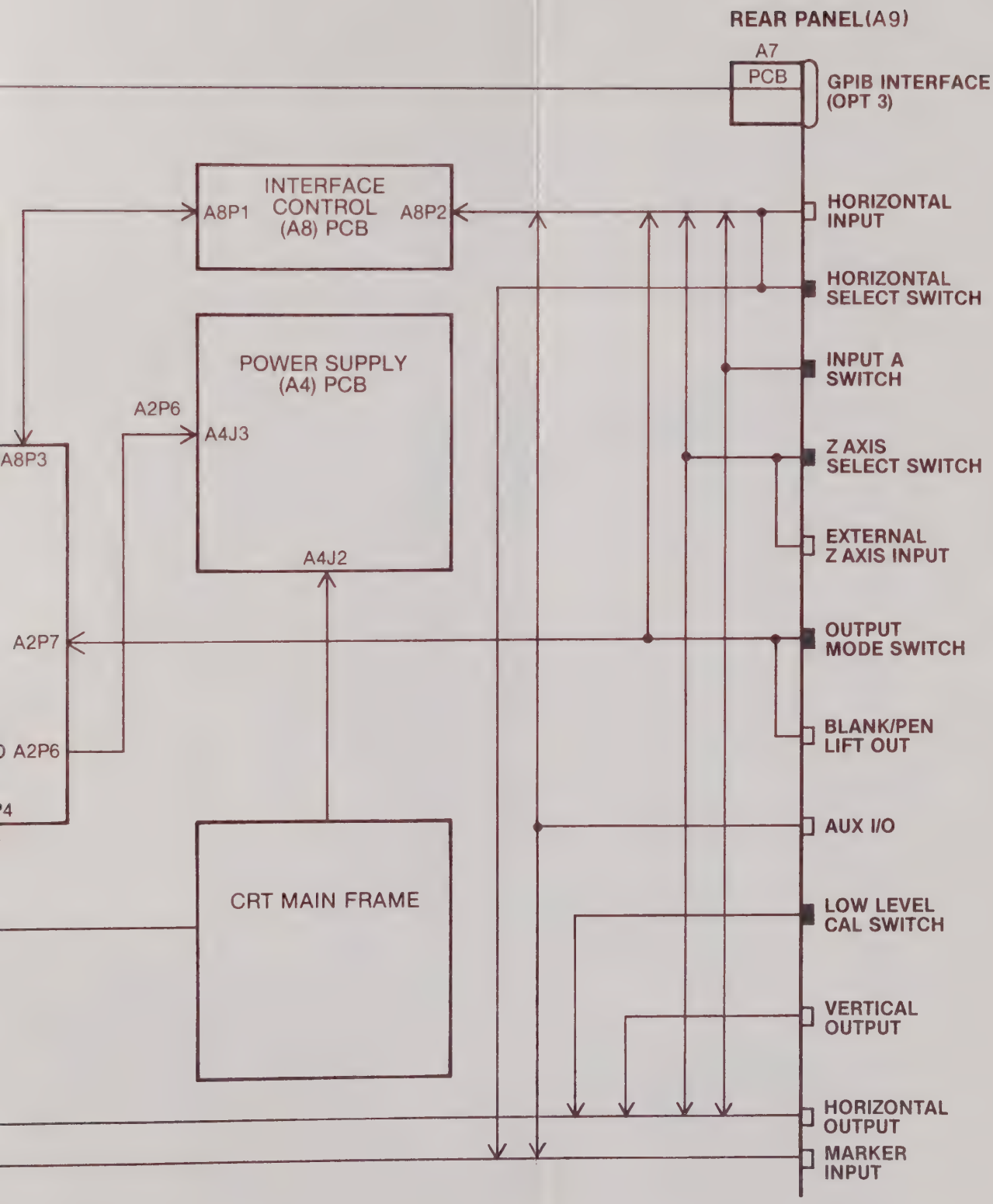
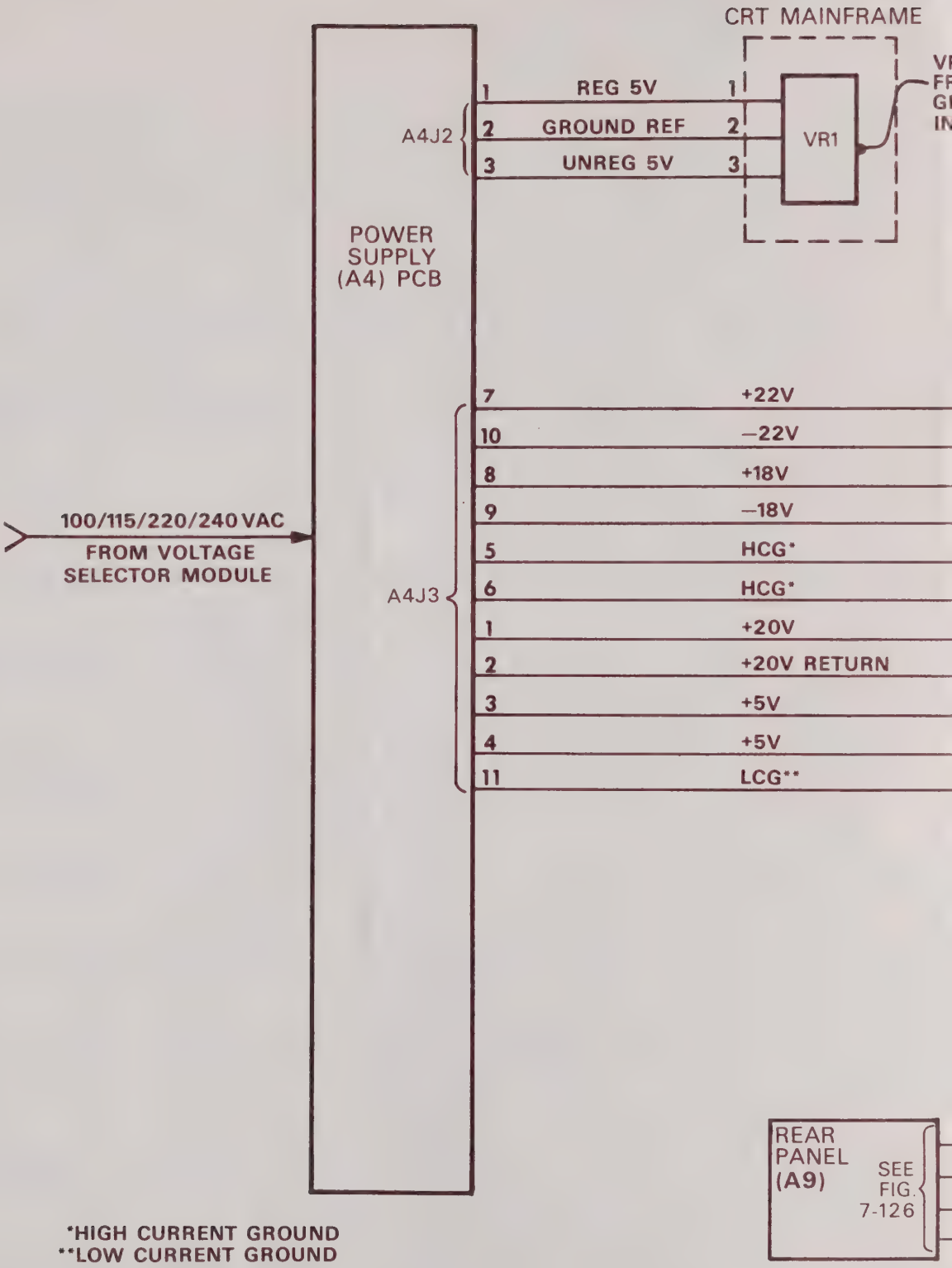


Figure 7-19. 560A Interconnect Diagram


CRT MAINFRAME
VR1
A4J2
1 REG 5V
2 GROUND REF
3 UNREG 5V
POWER SUPPLY (A4) PCB
A4J3
7 +22V
10 −22V
8 +18V
9 −18V
5 HCG*
6 HCG*
1 +20V
2 +20V RETURN
3 +5V
4 +5V
11 LCG**
100/115/220/240 VAC
FROM VOLTAGE SELECTOR MODULE
REAR PANEL (A9)
SEE FIG. 7-126
*HIGH CURRENT GROUND
**LOW CURRENT GROUND

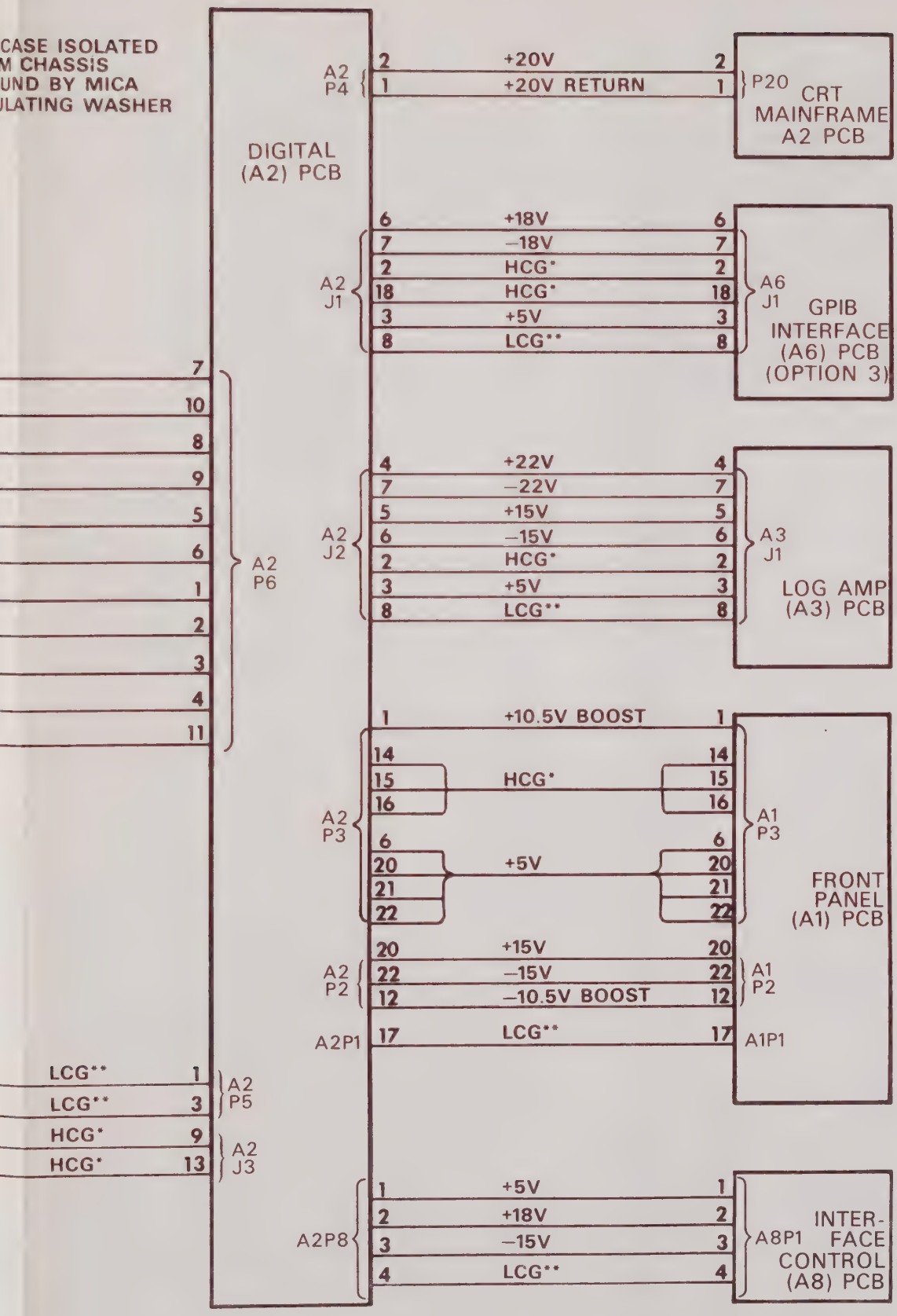


Figure 7-20. 560A Power Supply Voltages, Distribution Diagram

7-5 MICROWAVE COMPONENTS

The microwave components consist of of Model 560-97, -98, and -6 series SWR Autotesters and the Model 560-7 and 560-71 series RF Detectors. Functional descriptions of these components, along with instructions for replacing the detector diode in the two models of RF detectors and in the Model 560-6 series SWR Autotesters are provided in the following paragraphs. General information pertaining to center-pin replacement on WSMA connectors, and to care and cleaning of installed RF connectors is also included.

7-5.1 SWR Autotesters

The 560-97, -98, and -6 series SWR Autotesters are highly accurate devices for making reflection measurements. The components consist of a broadband microwave bridge, a precision termination, a zero-bias Schottky diode, and a low-reflection test port connector. The SWR Autotesters are precision manufactured microwave components. There are o internal adjustments, and repair is limited to:

a. Center pin replacement on the 560-97 and -98S50 and SF50 SWR Autotesters' WSMA male and female connectors (paragraph 7-5.7).

b. Diode replacement on the 560-6 series SWR Autotesters (paragraph 7-5.4).

7-5.2 Model 560A-7 Series RF Detectors

The 560-7 series RF detectors are sensitive, frequency-accurate, broadband, microwave RF detectors; they use a zero-bias Schottky diode for RF detection and have a frequency range, depending upon Option number of .01 to 18.5 GHz, .01 to 26.5 GHz, .01 to 34 GHz, or .01-40 GHz. The detector consists of the 560-A-7219 field-replaceable diode module assembly and the A1 printed circuit board (PCB) assembly.
The Model 560-7 RF Detector is a precision manufactured microwave component. The only repair that is recommended is replacement of the diode module assembly (paragraph 7-5.5).

7-5.3 • Model 560-71 Series RF Detectors

The 560-71 series RF detectors provide the 560A with a 1.0 MHz to 2.0 GHz frequency capability. The detectors are manufactured in 50 and 75-ohm types. The 560-71N50 type offers an input impedance of 50 ohms; the 560-71N75 type offers an input impedance of 75 ohms. Both detector types offer exceptionally flat transmission and return loss characteristics, and both have field-replaceable zero-bias Schottky detector diodes.

The Model 560-71 RF Detector is a precision manufactured microwave component. The only repair recommended is replacement of the detector diode (paragraph 7-5.6).

7-5.4 Diode Replacement, 560-6 Series SWR Autotesters

The 560-6 series SWR Autotesters are equipped with a field-replaceable detector diode. To replace this diode, proceed as follows:

a. Remove the two screws from the top cover of the SWR Autotester (top cover contains the model number), and remove cover.

b. Unplug and remove diode (Figure 7-21) from SWR Autotester circuit board.

Figure 7-21. 560-6 SWR Autotester With Detector Diode Shown

c. Install replacement diode with cathode (black ring or red dot) positioned toward the test port connector.

d. Replace top cover and reinstall the two screws.

7-5.5 Diode Replacement, 560-7 Series RF Detectors

The 560-7 series RF detectors are equipwith a field-replaceable diode module that contains - in addition to the detector diode - a thermistor, a resistor, and two capacitors. An exploded view of this detector is shown in Figure 7-22. Replacement of this diode module requires realignment of two potentiometers, located within the detector housing. The realignment of these potentiometers is accomplished after the defective diode module is removed but before the replacement diode module is installed. To set the resistance of these two potentiometers, use a digital multimeter that has at least a 3-1/2 digit display resolution. To replace the diode module, proceed as follows:

a. Remove four retaining screws and lift top cover away from detector housing.

b. Remove two retaining screws from A1 PCB.

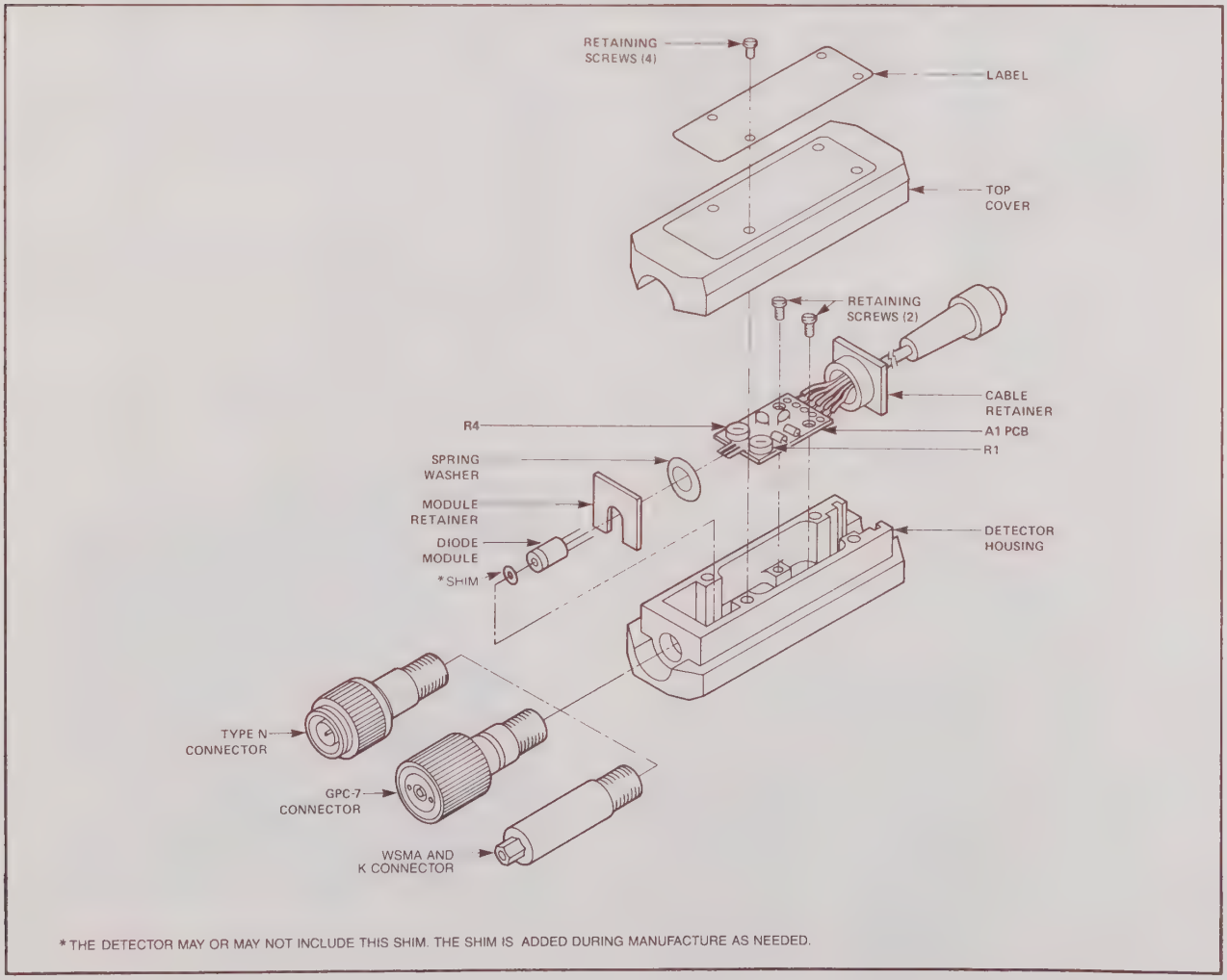


Figure 7-22. Model 560-7 Series RF Detector, Exploded View

c. Slide cable retainer out of detector housing assembly. When cable retainer clears housing, disconnect A1 PCB from diode module.

d. Remove fiberglass module retainer from housing. This retainer can be removed by prying it out using a small screwdriver or by pulling it out using a pair of short, round-nose pliers.

e. Remove diode module from its housing in rear of connector. The module can be removed by pulling it straight out.

f. Adjust potentiometer R1 fully clockwise (maximum resistance).

g. Connect digital multimeter between pins 1 and 2 of detector connector (Figure 7-23) and measure the resistance value of R1 (typical value is 40.5kΩ). This resistance value is hereafter known as R_T; record this value.

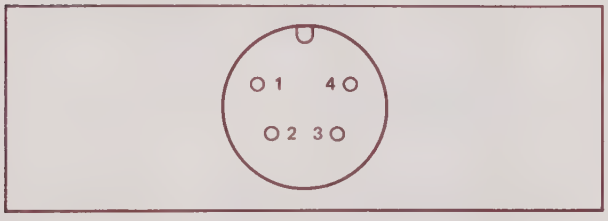


Figure 7-23. Pin Orientation on RF Detector Connector

h. Obtain "K" value from label (Figure 7-24) on replacement module's plastic container.

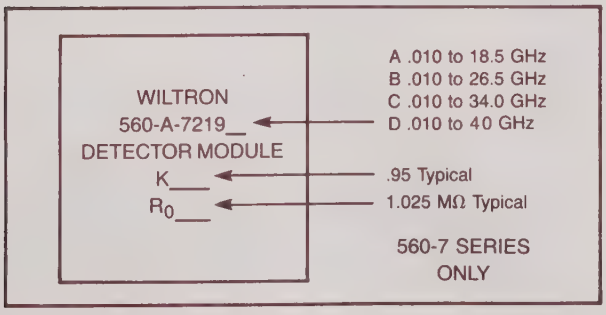


Figure 7-24. Label from Replacement Module Container

i. Multiply "K" times R_T ($K \times R_T$) and record this value.

j. Adjust R1 counterclockwise until the digital multimeter indicates resistance value calculated in step i.

k. Disconnect multimeter leads from between pins 1 and 2 and connect between pin 3 and connector shield.

l. Obtain the value for R_O from label; adjust R4 until multimeter indicates "R_O" value.

m. Disconnect multimeter leads from detector connector.

n. Orient replacement module so that center lead is on top; slide module into its housing at rear of connector (Figure 7-22).

o. Orient washer so that two curved flanges point toward A1 PCB and are positioned at 3 o'clock and 9 o'clock.

p. Insert fiberglass module retainer between module and washer; push down on retainer until firmly seated.

q. Orient A1 PCB so that center pin on three-pin-module connector is on top; insert A1 PCB into detector housing so that module connector mates with leads coming from diode module.

NOTE

It may be easier to mate diode module with A1 connector if module leads are bent to about a 45° angle.

r. Insert cable retainer into its slot in detector housing.

s. Align retaining screw holes in A1 PCB with those in detector.

t. Diode module replacement is complete; reinstall top cover and four retaining screws.

7-5.6 Diode Replacement, 560 71 Series RF Detectors

The 560-71 series RF detectors are equipped with a field-replaceable detector diode. Replacement of this diode requires readjustment of two potentiometers located within the detector housing. The readjustment of these potentiometers is accomplished after the defective diode is removed, but before the replacement diode is installed. To set the resistance of these two potentiometers, use a digital multimeter that has at least a 3-1/2 digit display resolution. To replace the diode, proceed as follows:

a. Remove the four retaining screws and lift top cover away from detector housing.

b. Unplug diode (Figure 7-25) from circuit board and remove from detector.

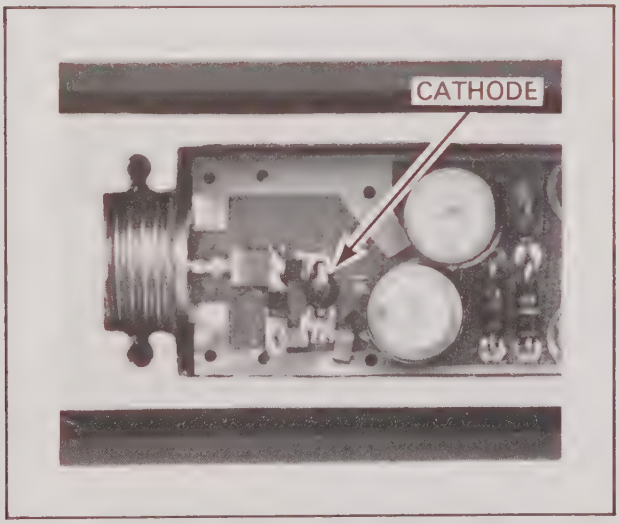


Figure 7-25. Model 560-71N75 With Detector Diode Shown

c. Adjust potentiometer R1 fully clockwise (maximum resistance).

d. Connect digital multimeter between pins 1 and 2 of detector connector (Figure 7-26) and measure the resistance of R1 (typical value is 40.5kΩ). This resistance value is hereafter known as R_T; record this value.

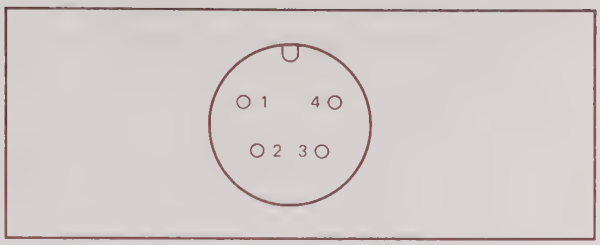


Figure 7-26. Pin Orientation on RF Detector Connector

e. Obtain "K" value from label (Figure 7-27) on replacement module's plastic container.

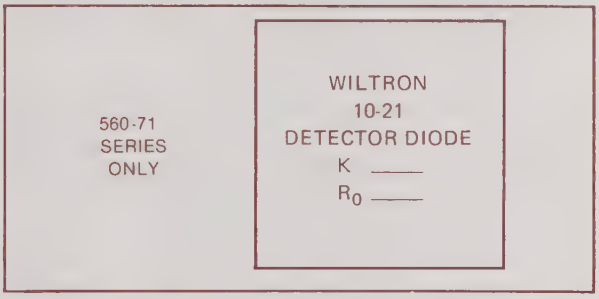


Figure 7-27. Label from Replacement Module Container

f. Multiply "K" times R_T ($K \times R_T$) and record this value.

g. Adjust R1 counterclockwise until the digital multimeter indicates the resistance value calculated in step f.

h. Disconnect multimeter leads from between pins 1 and 2 and connect between pin 3 and connector shield.

i. Obtain value for R_O from label; adjust R4 until multimeter indicates "R_O" value.

j. Disconnect multimeter from detector connector.

k. Orient replacement diode so that white dot (cathode) is positioned as shown in Figure 7-25. Insert diode into socket on A1 PCB.

l. Diode replacement is complete; reinstall top cover and four retaining screws.

7-5.7 WSMA Connector Center-Pin Replacement

The WSMA connector center-pin on the 560-97 and -98 S50 and SF50 SWR Autotester test ports are field-replaceable. The replacement procedure requires use of the WILTRON Model 01-160 Gauging Set. Instructions for center-pin replacement are included with the gauging set.

7-5.8 Connector Cleaning

Connector interfaces, especially the outer conductors on the GPC-7 and WSMA connectors, should be kept clean and free of dirt and other debris. Alcohol is the recommended cleaning agent, and a clean, damp cotton swab is the recommended applicator.

CAUTION

On all models of the 560-97 and -98 SWR Autotesters, the test port connector may have small teflon rings located on the center conductor. These rings are compensating washers and their position on the center conductor must not be disturbed. Any movement of these washers will degrade the directivity of the component.

7-6 LOG AMPLIFIER (A3) PRINTED CIRCUIT BOARD

This printed circuit board (PCB), in conjunction with the A10 Input Module Assembly, amplifies and logarithmically shapes the A, B, and R input signals. The A3 PCB contains 15 major circuits and is diagramed on 8 sheets of schematics. To provide continuity between schematics, a system of descriptive mnenonics identifies the control and signal lines used. Table 7-1 provides an alphabetical listing of these mnemonic symbols. The listing also includes "Definition, " "To, " and "From" columns for each symbol.

To interconnect the A3 PCB with the front panel and the digital (A2) PCB, four connectors are used. Connector J1 connects the A3 PCB with the A2 PCB. Connectors J2 and J3, via the A10 Assembly, connect the A3 PCB with the front panel A and B connectors. Connector P1 connects the A3 PCB with the front panel R connector. Figure 7-28 provides a pinout chart for each of these connectors.

To provide maintenance instructions, technical information for the A3 PCB is organized into blocks of data. Each schematic is presented on a foldout page. With the schematic is a parts locator diagram showing the physical location of applicable components and, where applicable, a chart showing the voltage present at circuit test points. The description for each circuit shown on any particular schematic is contained on an adjacent, facing page.

To test certain A3 PCB circuits, a detector simulator must be used. This detector simulator simulates the resistance of the RF detector thermistor and offset potentiometer circuits. Figure 7-29 provides a parts list and instructions for fabricating the simulated detector.

To begin the circuit description, an overall block diagram is presented in Figure 7-30. This diagram shows the A3 PCB and its major circuits, as well as the signal and control lines (each identified by a mnemonic symbol) that connect these circuits together. Each of the circuits shown on this block diagram is described in a separate, numbered paragraph under this major heading. For example, the R Channel Log Amplifier is described in paragraph 7-6.1, the A10 Input Module in paragraph 7-6.2, and the Channel A Local Isolated-Ground Driver and ±15 Volt Regulator Circuits in paragraph 7-6.3.

Table 7-1. Listing of Mnemonic Symbols used with A3 PCB Circuits

MNEMONIC	DEFINITION	FROM*	TO*
AUTO BAL	Automatic Balancing Signal	Fig. 7-43/9D	Input Module via J2-11
BIAS A, B	Channel A&B Log Shaper Bias Voltage	Fig. 7-51/9F	Fig. 7-44/0D
CMA	Common-Mode A Signal	Fig. 7-39/8F	Fig. 7-39/0B
CMB	Common-Mode B Signal	Fig. 7-39/8B	Fig. 7-38/0F
CM DRV A	Common-Mode Drive A Signal	Fig. 7-38/8E	Input Module via J3-12
CM DRV B	Common-Mode Drive B Signal	Fig. 7-39/8C	Input Module via J2-6
DET BAL A	Detector Balance A Signal	Fig. 7-38/8F	Input Module via J2-14
DET BAL B	Detector Balance B Signal	Fig. 7-39/8C	Input Module via J2-5
DET R IN	Detector R Input Signal	Front Panel via P1-1	Fig. 7-33, Sh. 1/1C
DET R RTN	Detector R Return Signal	Front Panel via P1-2	Fig. 7-33, Sh. 1/1D
DET RTN A	Detector Return A Signal	Input Module via J2-8	Fig. 7-38/0F
DET RTN B	Detector Return B Signal	Input Module via J2-4	Fig. 7-39/0C
GUARD	Guard Shield	Fig. 7-52/7D	Input Module via J3-7
HIGH QUAL GROUND	High-Quality Ground (Detector A or B switched return line.)	Input Module via J2-13	Fig. 7-43/0D
-L A, B	Negative-Polarity Log A or B Signal	Fig. 7-44/9F	Fig. 7-51/0B
LAZ	Low active-state, Autozero Signal	A2 PCB	Fig. 7-51/0H

*The numeric/alpha characters (e.g., 0F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-1. Listing of Mnemonic Symbols used with A3 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
LDETA	Low active-state, Detector A Signal	A2 PCB via J1-11	Fig. 7-51/0G
$LFILT_1$	Low active-state, Filter 1 (SMOOTHING MIN) signal	A2 PCB via J1-12	Fig. 7-51/0G
$LFILT_2$	Low active-state, Filter 2 (SMOOTHING (MAX) Signal	A2 PCB via J1-13	Fig. 7-51/0G
LOG A, B	Log Amplifier A or B Signal	Fig. 7-51/9A	A2 PCB via J1-16
LOG A, B-R	Log Amplifier A or B minus R Signal	Fig. 7-51/9G	A2 PCB via J1-15
LOG R	Log Amplifier R Signal	Fig. 7-51/9A	A2 PCB via J1-14
-LOG R	Negative-Polarity Log Amplifier R Signal	Fig. 7-33, Sh. 2/9B	Fig. 7-51/0D
LOG 1 A, B	Log Amplifier A or B Sensitivity Level 1 Signal	Fig. 7-43/9A	Fig. 7-44/0B & Fig. 7-52/0G
LOG 2 A, B	Log Amplifier A or B Sensitivity Level 2 Signal	Fig. 7-43/9B	Fig. 7-44/0B
LOG 3 A, B	Log Amplifier A or B Sensitivity Level 3 Signal	Fig. 7-43/9B	Fig. 7-44/0B
LOG 1 R	Log Amplifier R Sensitivity Level 1 Signal	Fig. 7-33, Sh. 1/9A	Fig. 7-33, Sh. 2/0B
LOG 2 R	Log Amplifier R Sensitivity Level 2 Signal	Fig. 7-33, Sh. 1/9B	Fig. 7-33, Sh. 2/0B
LOW LEVEL TRACK A	Low Level Tracking A Signal	Fig. 7-38/8B	Input Module via J3-16
LOW LEVEL TRACK B	Low Level Tracking B Signal	Fig. 7-39/8E	Input Module via J3-13

* The numeric/alpha characters (e.g., 0F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-1. Listing of Mnemonic Symbols used with A3 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
LSWR	Low active-state, Switch-Reference Signal	A2 PCB via J1-10	Fig. 7-51/0A
OFFSET POT A	Offset Potentiometer A Signal	Input Module via J3-5	Fig. 7-39/0B
OFFSET POT B	Offset Potentiometer B Signal	Input Module via J2-1	Fig. 7-39/0F
OP AMP FB	Operational Amplifier Feedback Signal	Fig. 7-43/9A	Input Module via J3-14
OP AMP OUT	Operational Amplifier Output Signal	Input Module via J2-16	Fig. 7-43/0C
OP AMP V+	Operational Amplifier V+ Voltage	Fig. 7-43/9E	Input Module via J2-15
OP AMP V-	Operational Amplifier V- Voltage	Fig. 7-43/9G	Input Module via J3-15
OSA	Offset A Voltage	Fig. 7-38/8C	Fig. 7-51/0E
OSB	Offset B Voltage	Fig. 7-39/8D	Fig. 7-51/0E
OSR	Offset R Voltage	Front Panel via P1-4	Fig. 7-33, Sh. 2/0F
SHIELD A	Shield A Signal	Input Module via J3-4	Fig. 7-38/0C
SHIELD B	Shield B Signal	Input Module via J2-3	Fig. 7-39/0E
SHIELD R	Shield R Signal	Front Panel via P1-3	Fig. 7-33, Sh. 1/1E
TEST IN	Test Signal For Factory Log Conformity Tests	A2 PCB via J1-1	Fig. 7-51/0A
THERMIS-TOR A	Thermistor A Signal	Input Module via J3-6	Fig. 7-38/0A
THERM A	Thermistor A Voltage	Fig. 7-37/8B	Fig. 7-51/0D

* The numeric/alpha characters (e.g., 0F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-1. Listing of Mnemonic Symbols used with A3 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
THERMIS-TOR B	Thermistor B Signal	Input Module via J2-2	Fig. 7-39/0F
THERM B	Thermistor B Voltage	Fig. 7-39/8F	Fig. 7-51/0D
THERM R	Thermistor R Voltage	Front Panel via P1-5	Fig. 7-33, Sh. 2/0F
VCC	Collector Voltage	Fig. 7-51/9B	Fig. 7-52/0H
(1)	Channel A Switch-Reference CMOS Logic Voltage	Fig. 7-51/9A	Fig. 7-52/1B
[1]	Channel A Switch-Reference J-FET Voltage	Fig. 7-52/7A	Input Module via J3-10
(2)	Channel A Switch-Reference CMOS Logic Voltage	Fig. 7-51/9B	Fig. 7-52/1B
[2]	Channel A Switch-Reference J-FET Voltage	Fig. 7-52/7B	Input Module via J3-9
(3)	Channel A Select CMOS Logic Voltage	Fig. 7-51/9B	Fig. 7-38/0F & Fig. 7-43/0G
[3]	Channel A Select J-FET Voltage	Fig. 7-52/7C	Input Module via J3-12
[3']	Channel A Select Stretched J-FET Voltage	Fig. 7-52/7D	Input Module via J3-13
(4)	Channel B Switch-Reference CMOS Logic Voltage	Fig. 7-51/9C	Fig. 7-52/1D
[4]	Channel B Switch-Reference J-FET Voltage	Fig. 7-52/7D	Input Module via J2-7
(5)	Channel B Switch-Reference CMOS Logic Voltage	Fig. 7-51/9C	Fig. 7-52/1E
[5]	Channel B Switch-Reference J-FET Voltage	Fig. 7-52/7E	Input Module via J3-8

* The numeric/alpha characters (e.g., 0F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-1. Listing of Nmemonic Symbols used with A3 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
⑥	Channel B Select CMOS Logic Voltage	Fig. 7-51/9D	Fig. 7-39/0E & Fig. 7-43/0G
[6]	Channel B Select J-FET Voltage	Fig. 7-52/7F	Input Module via J2-10
[6']	Channel B Select Stretched J-FET Voltage	Fig. 7-52/7F	Input Module via J2-9
⑦	Channel A Autozero Voltage	Fig. 7-51/9D	Fig. 7-43/0G
⑧	Channel B Autozero Voltage	Fig. 7-51/9D	Fig. 7-43/0H
⑨	Channel A Filter 1 Voltage	Fig. 7-51/9E	Fig. 7-43/0D
⑩	Channel A Filter 2 Voltage	Fig. 7-51/9E	Fig. 7-43/0B
⑪	Channel B Filter 1 Voltage	Fig. 7-51/9F	Fig. 7-43/0F
⑫	Channel B Filter 2 Voltage	Fig. 7-51/9E	Fig. 7-43/0B

* The numeric/alpha characters (e.g., 0F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

J1
Connects To A2J2
(Digital PCB)

Pin No.	Signal Name	From/To (Figure No.)
1	TEST IN	Figure 7-51
2	HCG*	Figure 7-51
3	+5V	Figure 7-51
4	+22V	Figure 7-33, Sh. 1
5	+15V	Figure 7-51
6	-15V	Figure 7-51
7	-22V	Figure 7-33, Sh. 1
8	LCG**	Figure 7-33, Sh. 1
9	LAZ	Figure 7-51
10	LSWR	Figure 7-51
11	LDETA	Figure 7-51
12	LFILT 2	Figure 7-51
13	LFILT 1	Figure 7-51
14	LOG R	Figure 7-51
15	LOG A, B-R	Figure 7-51
16	LOG A, B	Figure 7-51

J2
Connects to A10P4
(Input Module Assembly)

Pin No.	Signal Name	From/To (Figure No.)
1	OFFSET POT B	Figure 7-39
2	THERMISTOR B	Figure 7-39
3	SHIELD B	Figure 7-39
4	DET RTN B	Figure 7-39
5	DET BAL B	Figure 7-39
6	CM DRV B	Figure 7-39
7	[4]	Figure 7-52
8	DET RTN A	Figure 7-38
9	[6]	Figure 7-52
10	[6']	Figure 7-52
11	AUTO BAL	Figure 7-43
12	CM DRV A	Figure 7-38
13	HI QUAL GND	Figure 7-43
14	DET BAL A	Figure 7-38
15	OP AMP V+	Figure 7-43
16	OP AMP OUT	Figure 7-43

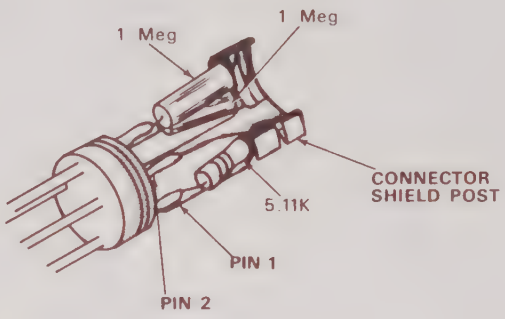
J3
Connects To A10P3
(Input Module Assembly)

Pin No.	Signal Name	From/To (Figure No.)
1	-15V	Figure 7-33, Sh. 1
2	HCG*	Figure 7-51
3	+5V	Figure 7-51
4	SHIELD A	Figure 7-38
5	OFFSET POT A	Figure 7-38
6	THERMISTOR A	Figure 7-38
7	GUARD	Figure 7-52
8	[5]	Figure 7-52
9	[2]	Figure 7-52
10	[1]	Figure 7-52
11	[3']	Figure 7-52
12	[3]	Figure 7-52
13	LOW LEVEL TRACK B	Figure 7-39
14	OP AMP FB	Figure 7-43
15	OP AMP V-	Figure 7-43
16	LOW LEVEL TRACK A	Figure 7-39

P1
Connects To Front Panel R Connector
Via Input Cable Assembly 560-B-7008

Pin No.	Signal Name	From/To (Figure No.)
1	DET R IN	Figure 7-33, Sh. 1
2	DET R RTN	Figure 7-33, Sh. 1
3	SHIELD R	Figure 7-33, Sh. 1
4	OS R	Figure 7-33, Sh. 2
5	THERM R	Figure 7-33, Sh. 2

Figure 7-28. Connector Pinout Charts



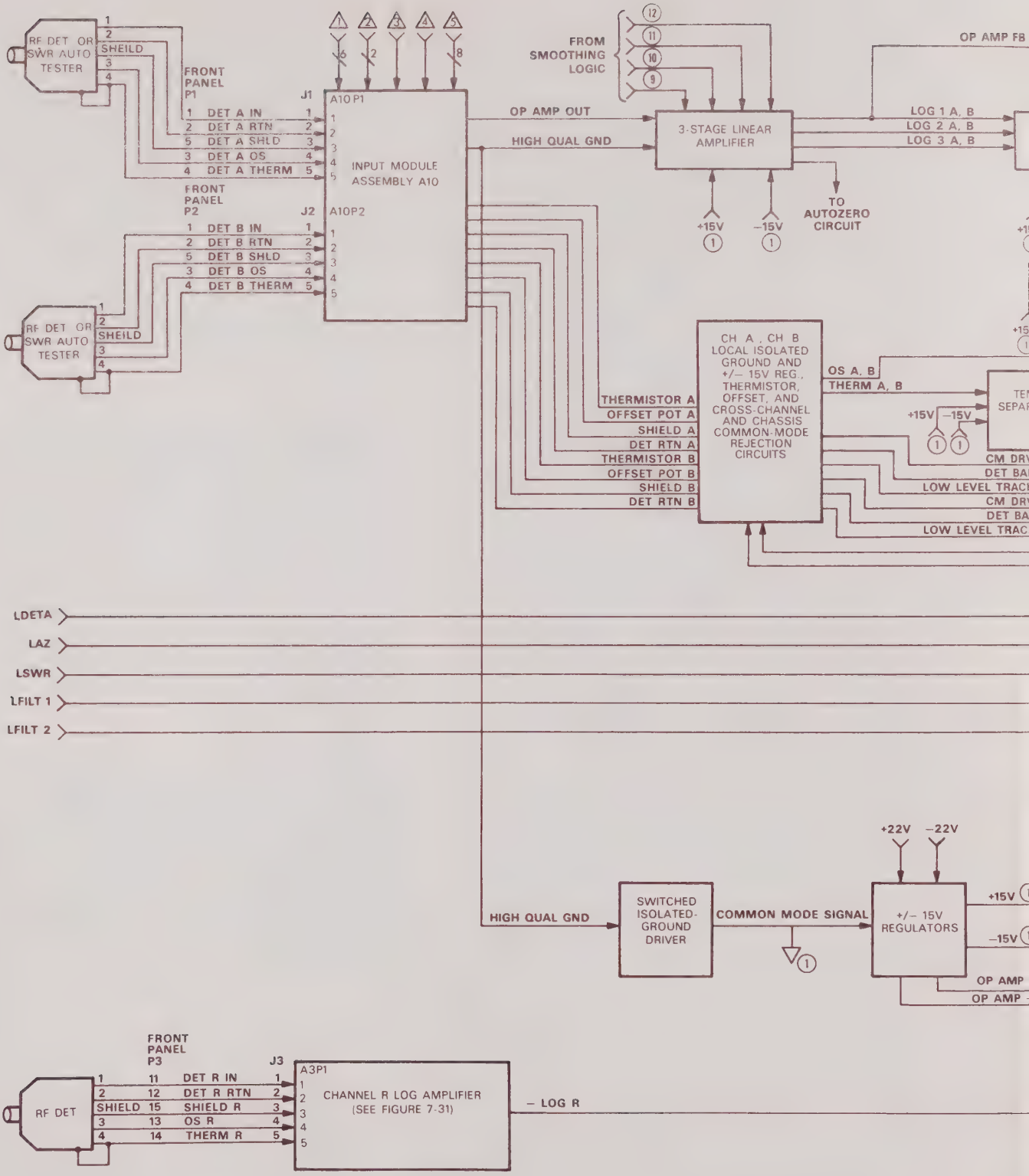
Fabricate simulated detector as follows:

1. Solder one end of 5.11 kΩ resistor to pin 1. Solder the other resistor lead to the connector shieldpost and to pin 2.
2. Solder 1 MΩ resistor to pin 3. Solder the other resistor lead to the shieldpost.
3. Solder 1 MΩ resistor to pin 4. Solder the other resistor lead to shieldpost.

Simulated Detector Parts List

Part Description	Part Number	Vendor
Connector, Plug	09CL4M	Switchcraft, Inc.
Resistor, Metal Film, 5.11 kΩ, 1/8W, 1% (1 each)	EMF55T1-5.11k-1%	Dale Elect.
Resistor, Metal Film, 1 MΩ, 1/8W, 0.1% (2 each)	EMF55T9-1 Meg-0.1% RNC55J1DO4BS	Dale Elect. Mil. Spec.

Figure 7-29. Simulated Detector Fabrication Instructions and Parts List


RF DET OR SWR AUTO TESTER
SHEILD
FRONT PANEL P1
J1
A10 P1
DET A IN
DET A RTN
DET A SHLD
DET A OS
DET A THERM
INPUT MODULE ASSEMBLY A10
FRONT PANEL P2
J2
A10P2
DET B IN
DET B RTN
DET B SHLD
DET B OS
DET B THERM
FROM SMOOTHING LOGIC
OP AMP FB
OP AMP OUT
HIGH QUAL GND
3-STAGE LINEAR AMPLIFIER
LOG 1 A, B
LOG 2 A, B
LOG 3 A, B
TO AUTOZERO CIRCUIT
+15V
−15V
CH A, CH B LOCAL ISOLATED GROUND AND +/− 15V REG., THERMISTOR, OFFSET, AND CROSS-CHANNEL AND CHASSIS COMMON-MODE REJECTION CIRCUITS
OS A, B
THERM A, B
THERMISTOR A
OFFSET POT A
SHIELD A
DET RTN A
THERMISTOR B
OFFSET POT B
SHIELD B
DET RTN B
LDETA
LAZ
LSWR
LFILT 1
LFILT 2
+22V
−22V
HIGH QUAL GND
SWITCHED ISOLATED-GROUND DRIVER
COMMON MODE SIGNAL
+/− 15V REGULATORS
OP AMP
RF DET
FRONT PANEL P3
J3
A3P1
DET R IN
DET R RTN
SHIELD R
OS R
THERM R
CHANNEL R LOG AMPLIFIER (SEE FIGURE 7-31)
− LOG R

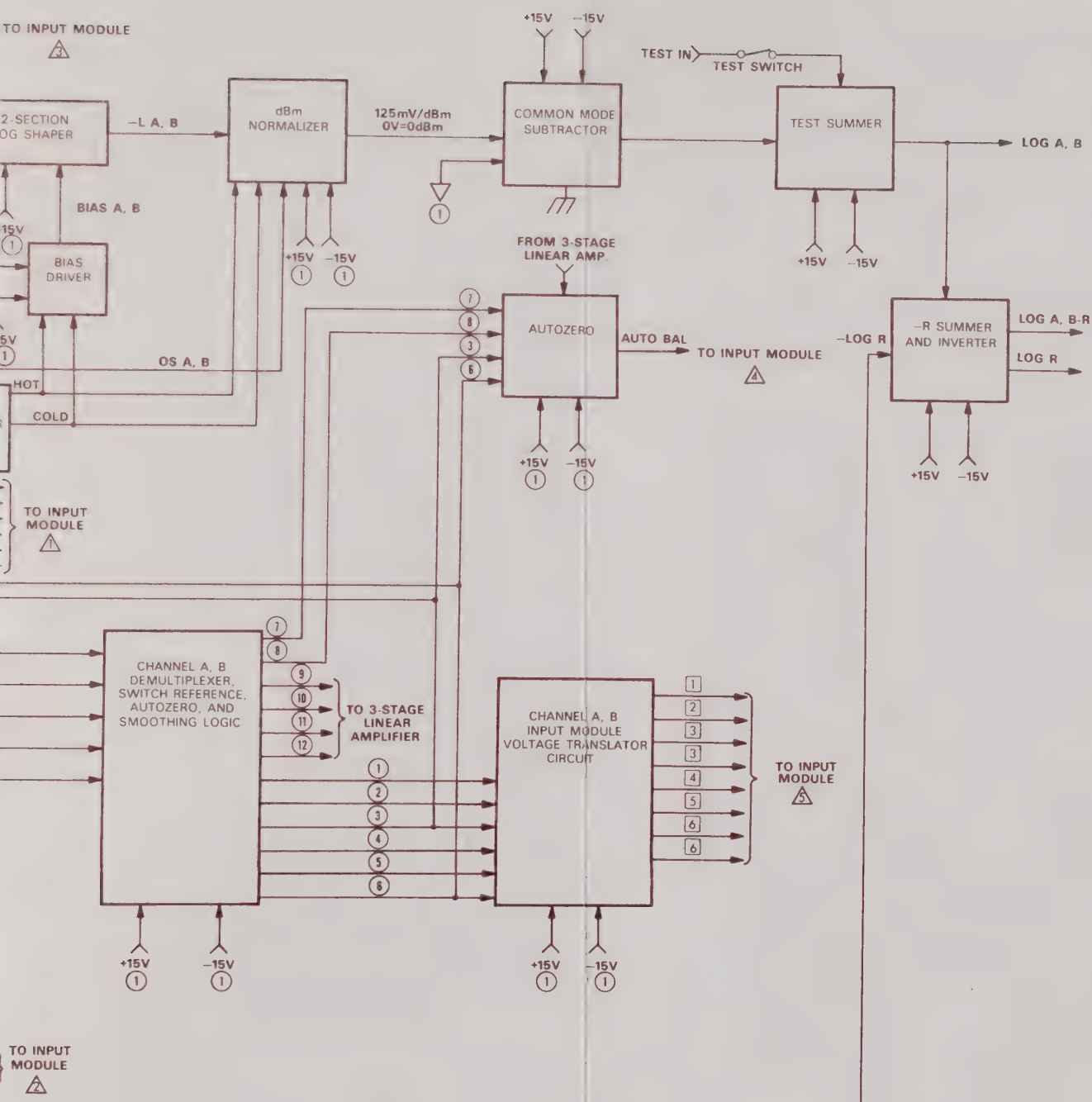


Figure 7-30. Log Amplifier (A3) PCB Overall Block Diagram

7-6.1 R Channel Log Amplifier

This circuit amplifies and logarithmically shapes the sensitivity-input power response curve of the detected input reference (R) signal. The R signal's response curve is shaped to compensate for the difference in detector response at different input power levels (detector response law). The amplifier consists of the following circuits: two-stage linear amplifier, isolated-ground driver, ±15 V regulator, 8-section log shaper, log-shaper bias generator, dBm normalizer, common-mode-signal subtractor, offset bridge, temperature bridge, and separator. A block diagram of the R channel log amplifier is shown in Figure 7-31. A parts locator diagram for the two-stage linear amplifier, the isolated-ground driver, and the ±15 V regulator circuits is shown in Figure 7-32, Sheet 1; their schematic is shown in Figure 7-33, Sheet 1. A parts locator diagram for the 8-section log shaper, the log shaper bias generator, the dBm normalizer, the common-mode-signal subtractor, the offset bridge, and the temperature bridge and separator circuits is shown in Figure 7-32, Sheet 2; their schematic is shown in Figure 7-33, Sheet 2. The R Channel log amplifier circuits are described below.

a. Two-Stage Linear Amplifier Circuit (Figure 7-33, Sh. 1). This circuit provides two stages of linear amplification for the input R signal. The first amplifier stage consists of operational amplifier U40, transistors Q5, Q6, and associated components. This stage has a gain of 11; its output signal, LOG 1 R, goes to the high input-signal-power (+16 to approximately -20 dBm) section of the 8-section log-shaper circuit. The second amplifier stage consists of operational amplifier U41, transistor Q7, and associated components. This stage is a high-gain (A=44) limiter-amplifier; the R195/CR46 thru CR49 resistor-diode circuit limits the stage output to +11.7 volts. The output of this stage, LOG 2 R, goes to the low-signal-power (approximately -20 to -30 dBm) section of the 8-section log-shaper circuit.

b. Isolated-Ground Driver Circuit (Figure 7-33, Sh. 1). This circuit provides the reference input for 15-volt regulators U42 and U43. This U42 and U43 reference input is a voltage from a low-impedance source that is equal to the Channel R RF detector common-mode voltage. The common-mode voltage is the voltage present on the detector case that is common to both the input and the return signals. The isolated-ground driver circuit consists of operational amplifier U44 and associated components.

c. ±15 Volt Regulator Circuit (Figure 7-33, Sh. 1)., The two 15-volt regulators U42 and U43 provide the V_{CC} voltages for all of the Channel R circuits except Common Mode Subtractor. With the R Channel V_{CC} supply referenced as described in subparagraph b above; interference normally attributed to common-mode signals is cancelled.

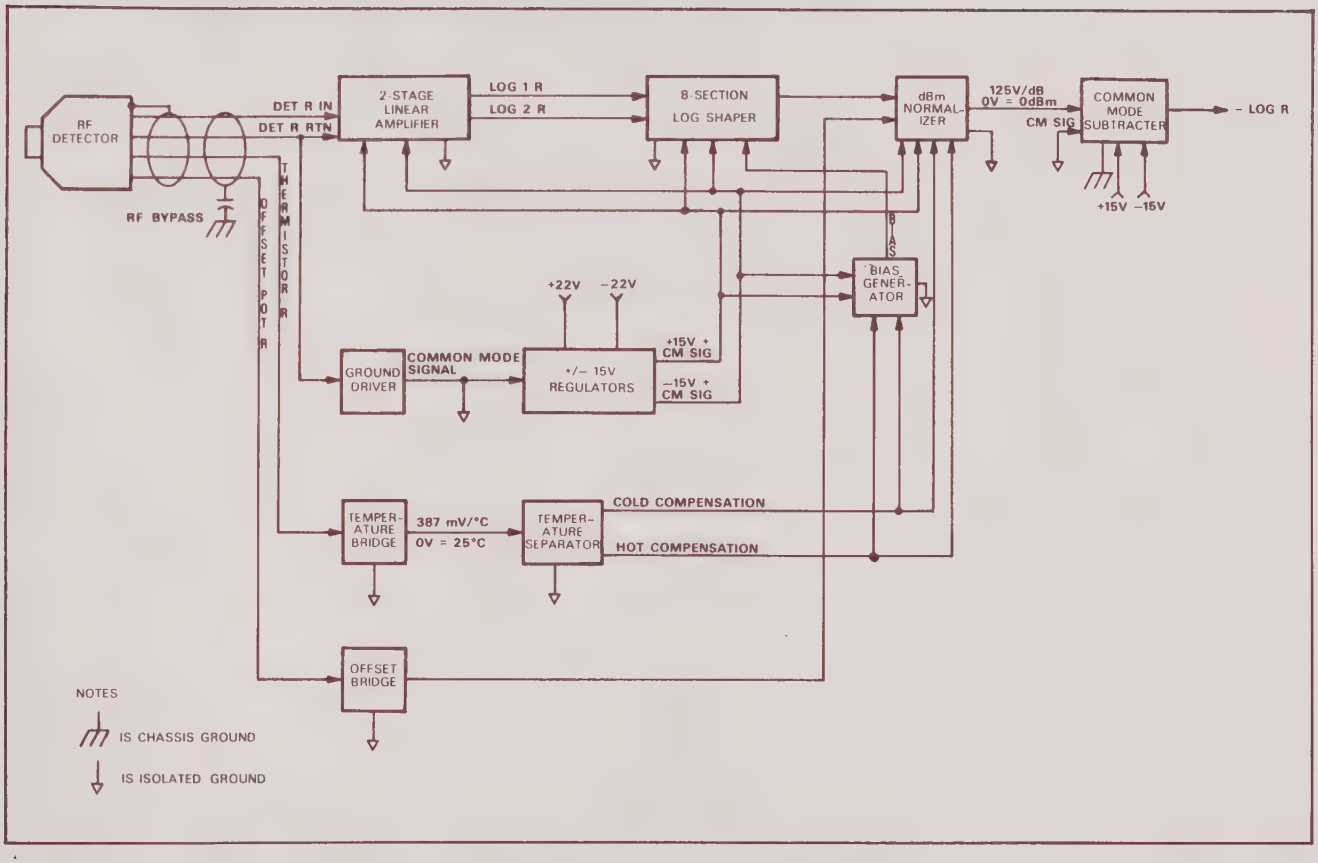
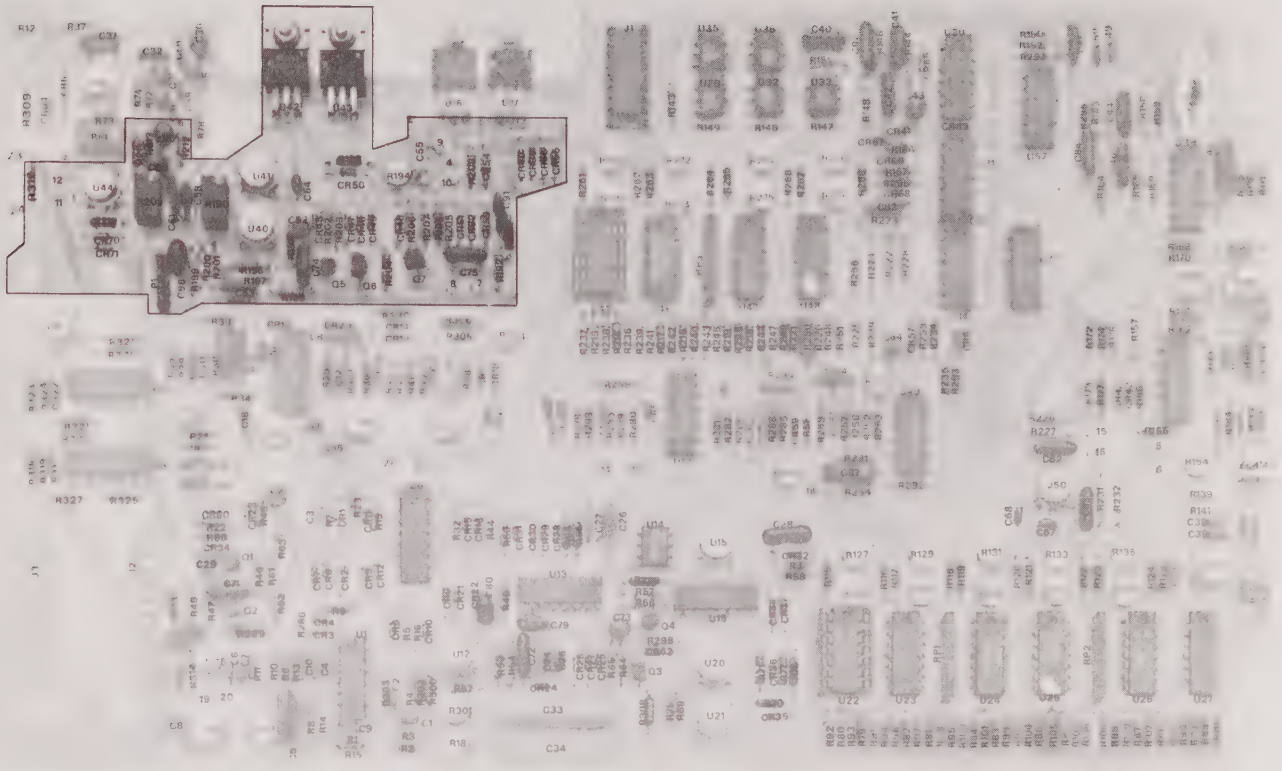


Figure 7-31. R Channel Log Amplifier, Block Diagram



TEST POINT VOLTAGE CHART

Test Point	Voltage	Schematic Location	Remarks
TP7	0 ± 100μVdc	6D	1. Reference measurement to TP12. 2. Connect RF detector to front panel R connector 3. Do not connect test device to RF detector input connector.
TP8	0 ± 3.0mVdc	8C	
TP9	+15 ± 0.6Vdc	4E	Reference measurement to TP12.
TP10	-15 ± 0.6Vdc	4G	
TP11	0 ± 50μVdc	6E	
TP12	0 Vdc	6E	Isolated-ground point.

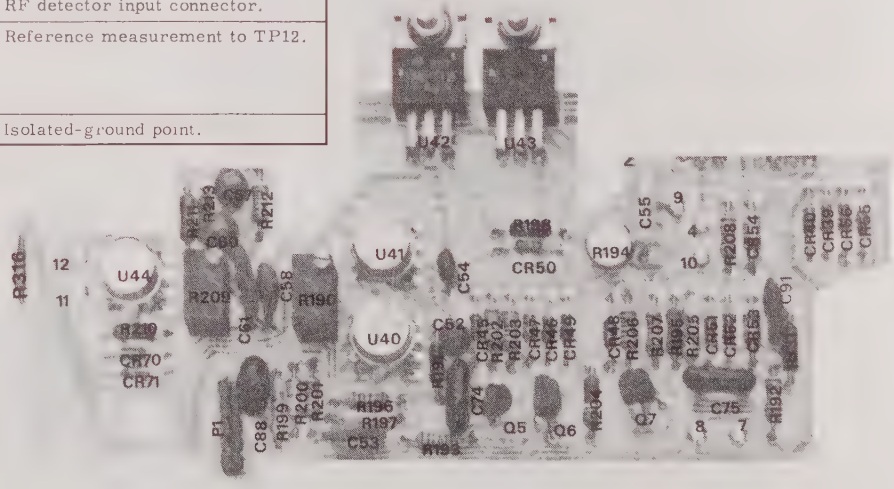
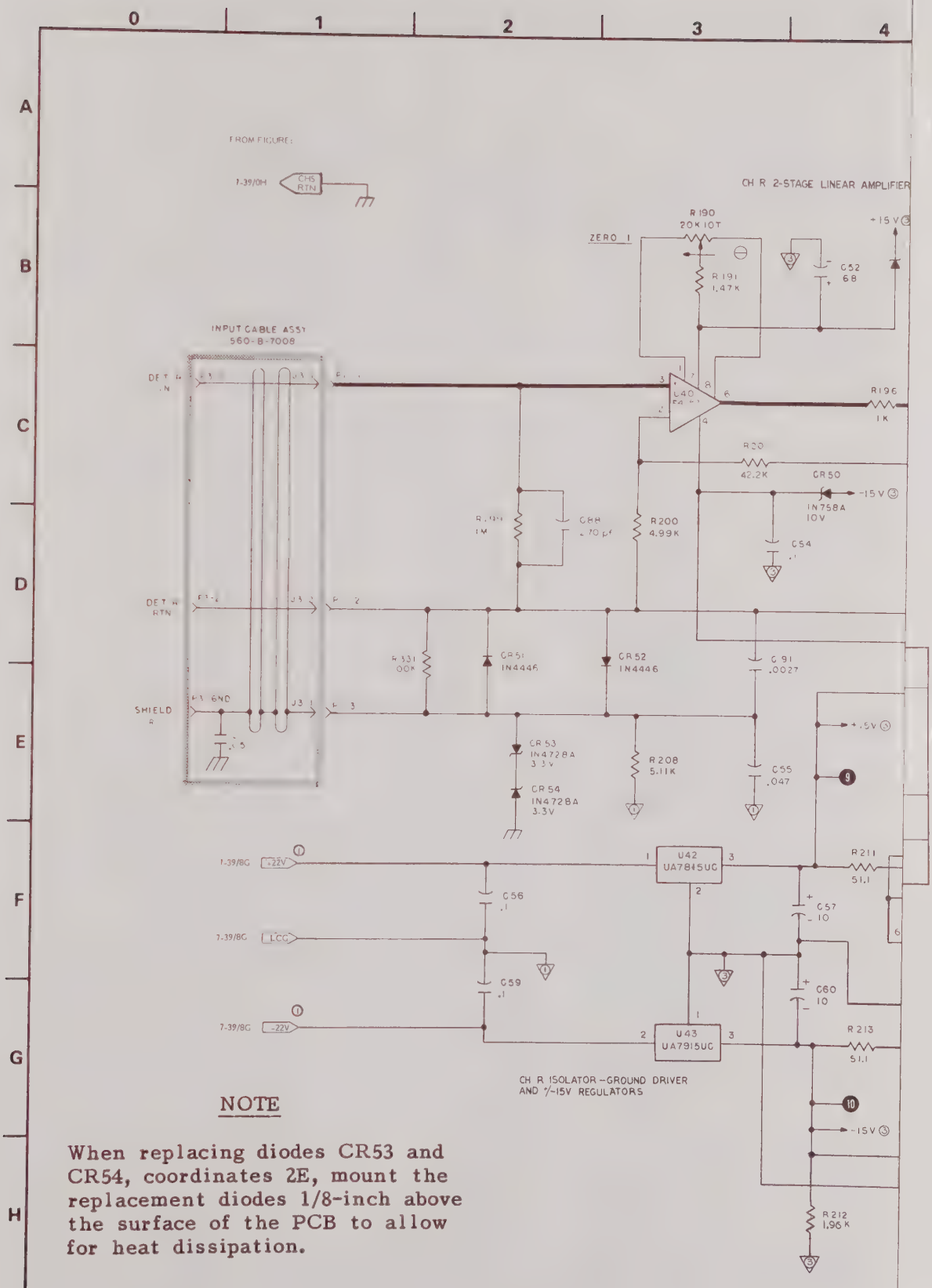


Figure 7-32, Sheet 1. Log Amplifier (A3) PCB Channel R 2-Stage Linear Amplifier, Isolated-Ground Driver, and ±15V Regulator Circuits Parts Locator Diagram



NOTE

When replacing diodes CR53 and CR54, coordinates 2E, mount the replacement diodes 1/8-inch above the surface of the PCB to allow for heat dissipation.

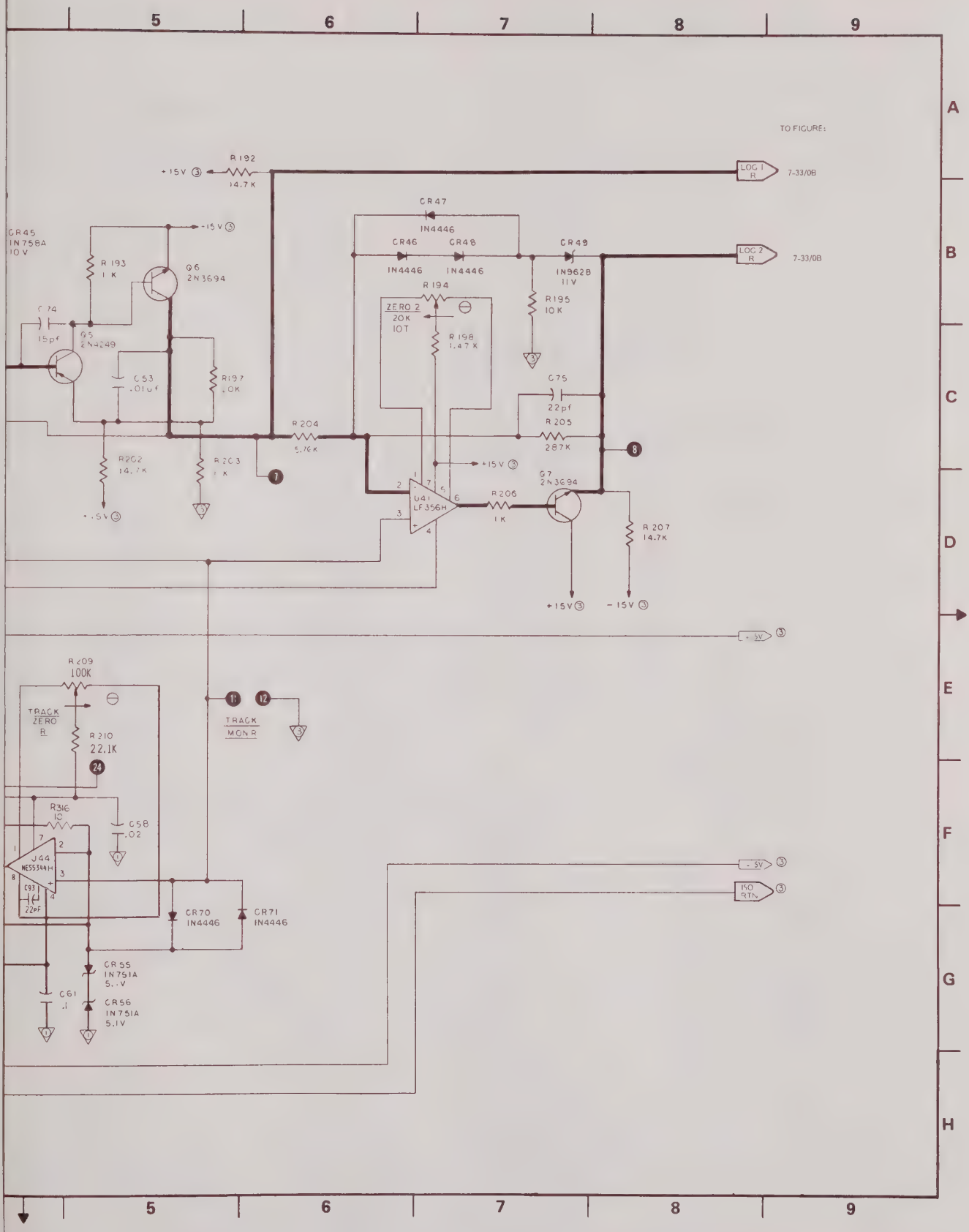


Figure 7-33, Sheet 1. Log Amplifier (A3) PCB Channel R 2-Stage Linear Amplifier, Isolated-Ground Driver, and ±15V Regulator Circuits Schematic Diagram

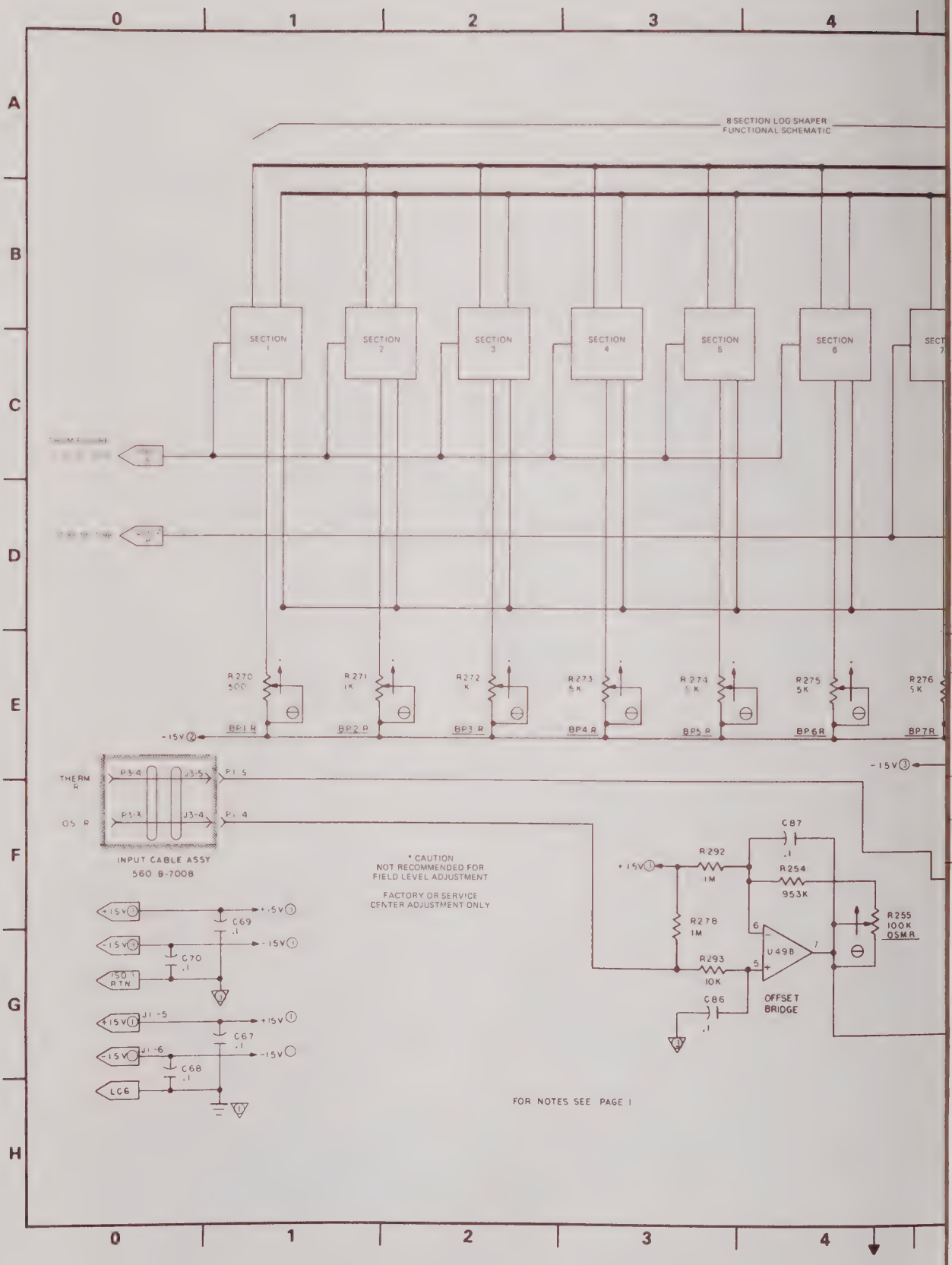
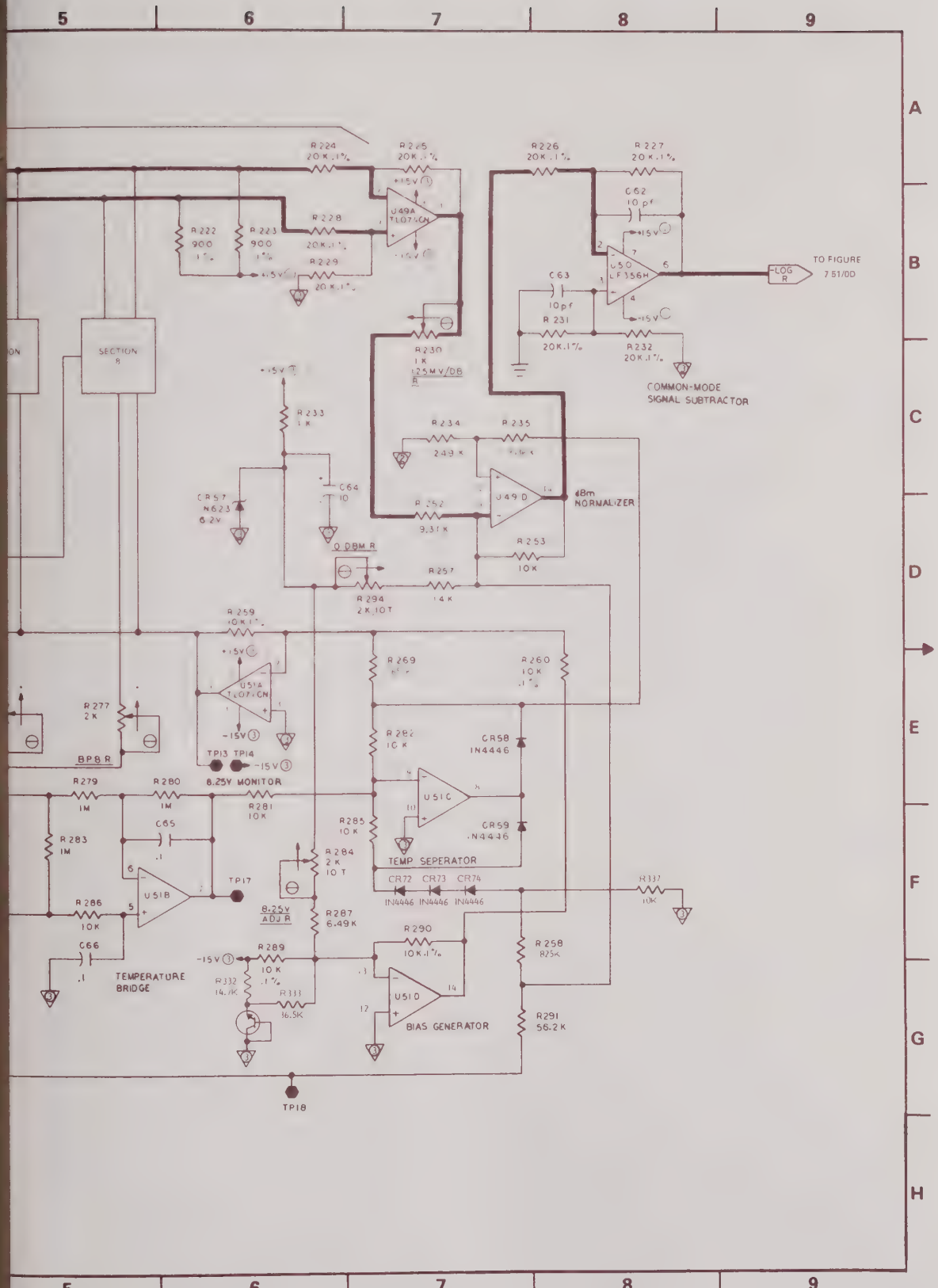
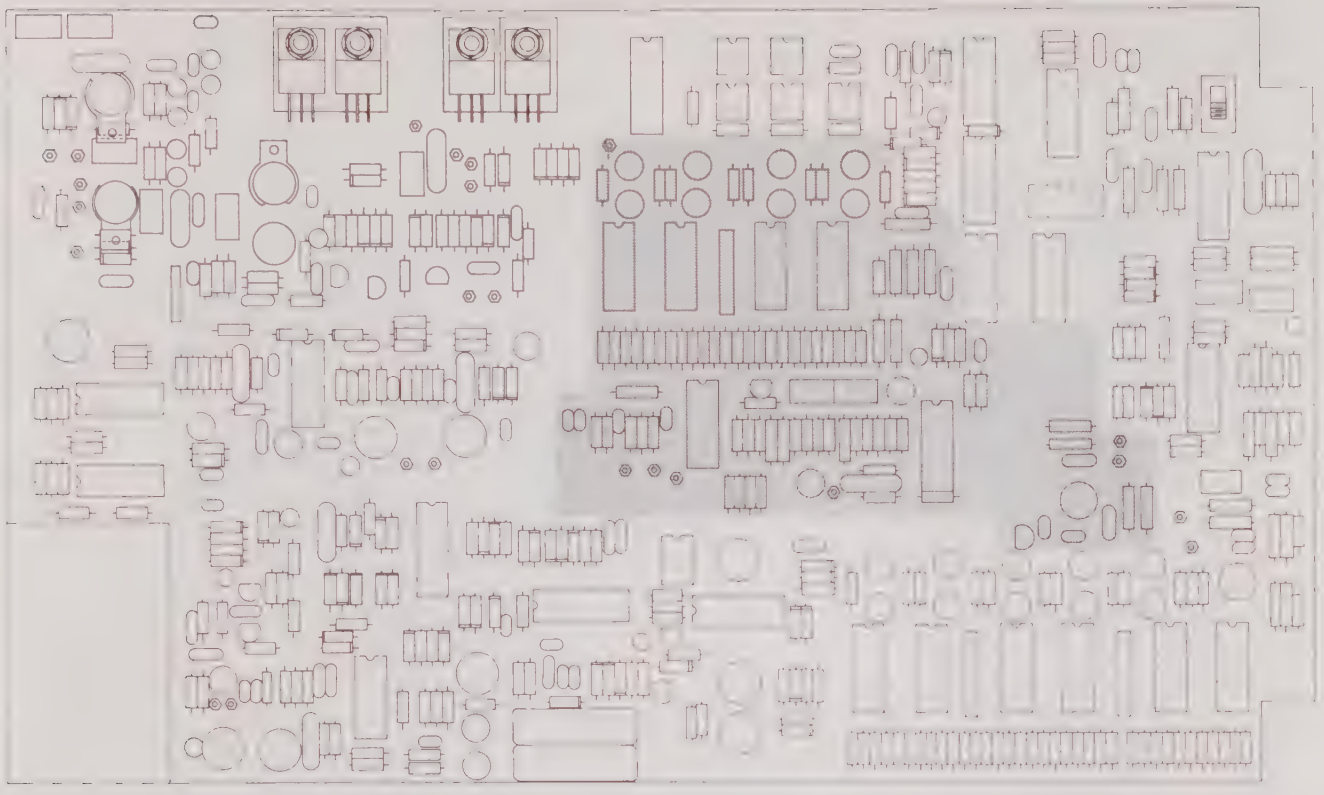


Figure 7-33, Sheet 2. Log Amplifier (A3) PCB Channel R 8-Section Log Shaper, Log Shaper Bias Generator, dBm Normalizer, Common-Mode Signal Subtractor, Offset Bridge, and Temperature Bridge and Separator Circuits Schematic Diagram


5
6
7
8
9
A
B
C
D
E
F
G
H
R224 20K .1%
R225 20K .1%
R226 20K .1%
R227 20K .1%
R222 900 1%
R223 900 1%
R228 20K .1%
R229 20K .1%
U49A TL074CN
+15V
-15V
C62 10 pf
U50 LF356H
C63 10pf
R231 20K .1%
R232 20K .1%
TO FIGURE 7 51/0D
LOG R
COMMON-MODE SIGNAL SUBTRACTOR
SECTION 8
R230 1K .25MV/DB R
R233 1K
C64 10
CR57 IN623 6.2V
R234 249 K
R235
R252 9.31 K
U49 D
dBm NORMALIZER
R253 10K
R257 14 K
0 DBM R
R294 2K .10T
R259 10K .1%
U51A TL074CN
R277 2K
BPB R
TP13 TP14
6.25V MONITOR
R269
R260 10K .1%
R282 10 K
CR58 IN4446
U51C
CR59 IN4446
TEMP SEPERATOR
R279 1M
R280 1M
R281 10K
R283 1M
C65 .1
R285 10 K
R284 2 K 10 T
U51B
TP17
CR72 CR73 CR74
IN4446 IN4446 IN4446
R337 10K
R286 10K
C66 .1
8.25V ADJ R
R287 6.49K
R289 10 K .1%
R290 10K .1%
R258 825K
TEMPERATURE BRIDGE
R332 14.7K
R333 36.5K
U51D
BIAS GENERATOR
R291 56.2 K
TP18



TEST POINT VOLTAGE CHART

Test Point	Voltage	Schematic Location	Remarks
TP13 & TP14	8.25 ± 0.003 Vdc	6E	1. Positive voltmeter lead to TP13; negative lead to TP14. 2. Connect simulated detector (Figure 7-29) to front panel R connector.
TP17	0 ± 100 mVdc	6F	1. Reference measurement to TP12
TP18	0 ± 20 mVdc	6G	2. Connect simulated detector to front panel R connector.

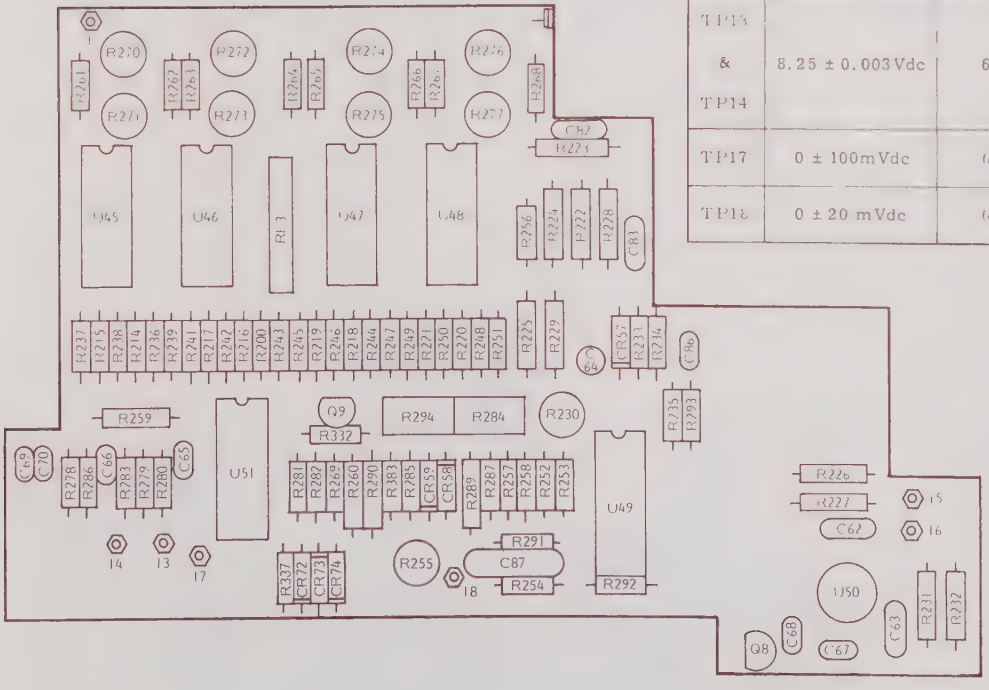


Figure 7-32, Sheet 2. Log Amplifier (A3) PCB Channel R 8-Section Log Shaper, Log Shaper Bias Generator, dBm Normalizer, Common-Mode Signal Subtractor, Offset Bridge, and Temperature Bridge and Separator Circuits Parts Locator Diagram

Figure 7-33.

d. 8-Section Log Shaper Circuit (Figure 7-33, Sh. 2). This circuit shapes the sensitivity-input power response curve of the R channel log amplifier to compensate for variations in RF detector sensitivity with input power. At high input-power levels (+16 to 0 dBm), the RF detector sensitivity response is linear; at low input-power levels (-18 to -50 dBm), the RF detector sensitivity response is square-law; and at medium input-power levels (0 to -18 dBm), the RF detector sensitivity response is in transistion between linear and square-law.

Repair and/or adjustment of this circuit is not recommended at the field level. The adjustments for log conformity, R270 thru R277, require specialized test equipment available only at the factory or at factory-authorized service centers.

e. Log Shaper Bias Generator (Figure 7-33, Sh. 2). This circuit generates a bias voltage that varies with the temperature of the RF detector. This bias voltage controls the conduction of current through the eight log-shaper sections. The bias generator, by controlling log shaper current conduction, controls the shape of the sensitivity-input power response curve of the log shaper circuit. The bias generator circuit consists of operational amplifiers U51A, U51D, and associated components.

f. dBm Normalizer Circuit. This circuit normalizes the log shaper circuit output signal for 125mV per dBm of input signal. It also sets the normalized output signal so that 0 volts equals 0 dBm. The circuit consists of operational amplifier U49D and associated components. Resistor R154 provides the 125mV/dBm adjustment; resistor R181 provides the 0 dBm adjustment.

g. Common-Mode-Signal Subtractor Circuit (Figure 7-33, Sh. 2). This circuit subtracts the common-mode signal from the normalized R signal. The circuit consists of operational amplifier U50 and associated components. The V_{CC} voltage for this circuit comes from the Digital (A2) PCB, a different source than that used for the other R channel log amplifier circuits. The use of different ±15-volt regulators causes this circuit's V_{CC} supply to be referenced to chassis ground, rather than to isolated ground; instead, isolated ground provides the reference signal for the U50 non-inverting (+) input. The normalized R signal, which is referenced to isolated ground, provides the input to the U50 inverting (-) input. The U50 output is the inverted normalized R signal, minus the common-mode signal. The circuit output-LOG R goes to two places:

1. Operational amplifier U39D (Figure 7-51), where it is summed with the LOG A, B signal and supplied to the A3 PCB output circuit. The output of U39D is the LOG A, B-R signal.

2. Operational amplifier U39B (Figure 7-51), where it is inverted and supplied to the A3 PCB output circuit. The output of U39B is the LOG R signal.

h. Offset Bridge Circuit (Figure 7-33, Sh. 2). This circuit converts the resistance of the RF detector offset potentiometer to a voltage. This voltage, in conjunction with the voltage outputs of U51D (bias generator) and U51B/U51C (temperature bridge and separator), controls absolute calibration in dBm.

The offset potentiometer in the RF detector compensates for the minute differences that like diodes have in their operational characteristics. When the resistance of this potentiometer is set according to factory specifications, the field-replaceable detector module in the RF detector presents a standard RF power-in vs. voltage-out to the R channel log amplifier circuits.

This circuit consists of operational amplifier U49B and associated components.

i. Temperature Bridge and Separator Circuit (Figure 7-33, Sh. 2). This circuit performs two functions: (1) it converts the temperature of the RF detector diode to a voltage, and (2) it separates between hot (>25°C) and cold (<25°C) temperatures.

The temperature bridge, which converts temperature to voltage, consists of operational amplifier U51B and associated components. The output of U51B is a voltage signal whose magnitude is equal to 387mV/°C, with 0V equal to 25°C. This voltage, in conjunction with the voltage outputs of U49B (offset bridge), U51D (bias generator), and U51C (temperature separator), controls log shaper bias.

The temperature separator, which separates between hot and cold temperatures, consists of operational amplifier U51C and associated components. Resistor-diode circuit R285 and CR59 separates hot temperatures; resistor-diode circuit R282 and CR58 separates cold temperatures. This separation is needed because the RF detector-diode's voltage-input power characteristics are degraded with hot and cold temperatures.

7-6.2 A10 Input Module Assembly

The A10 is a sealed assembly used to multiplex between RF detectors (or SWR Autotesters) A and B to provide one input signal for the A and B log amplifier input circuits. This log A&B input signal is either the detector (SWR Autotester) A or the detector (SWR Autotester) B signal, depending upon which channel is selected (paragraph 7-7. 12). A block diagram of this assembly is provided in Figure 7-34. The A10 Assembly is electrically connected between the front panel and the A3 PCB by four connectors. Figure 7-35 provides pinout charts for these connectors. This figure also contains a diagram of the A10 that shows each connector's location and pin orientation. The A10 circuit is described below.

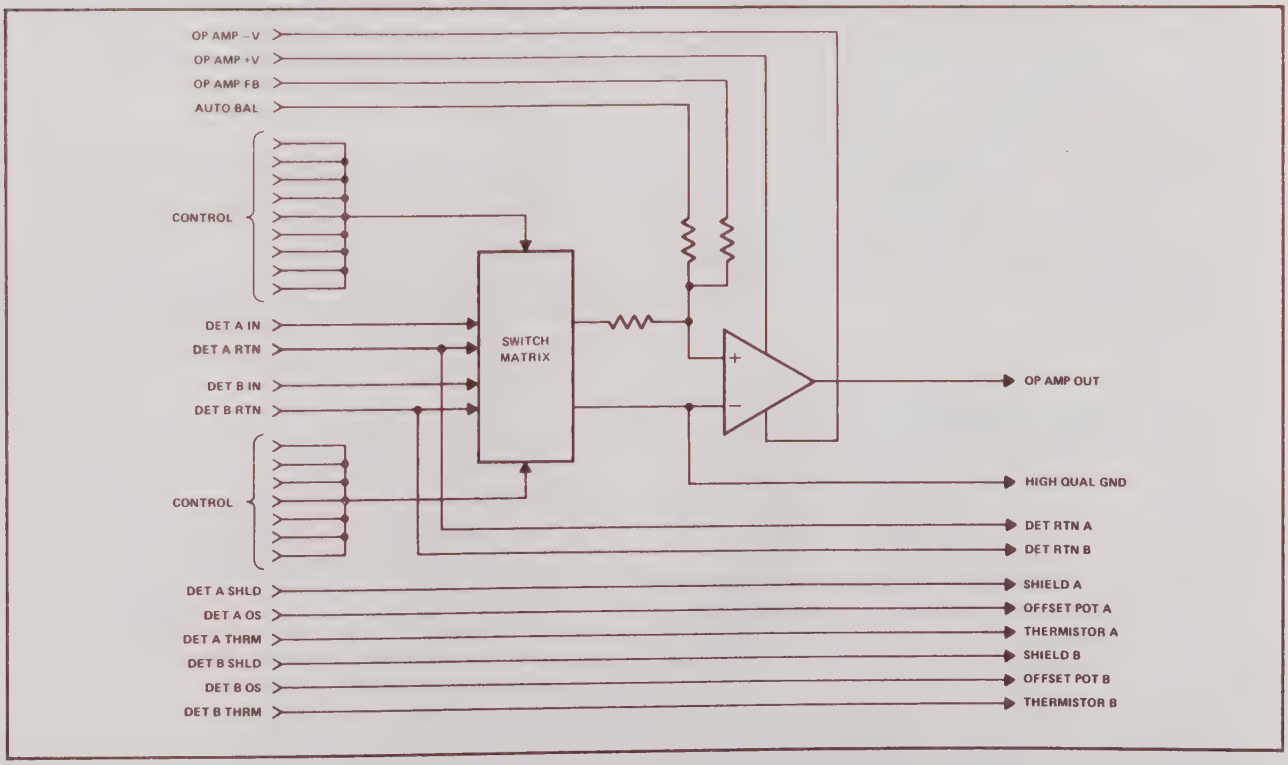


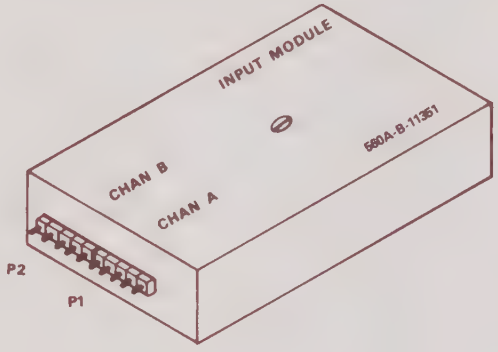
Figure 7-34. Input Module Block Diagram

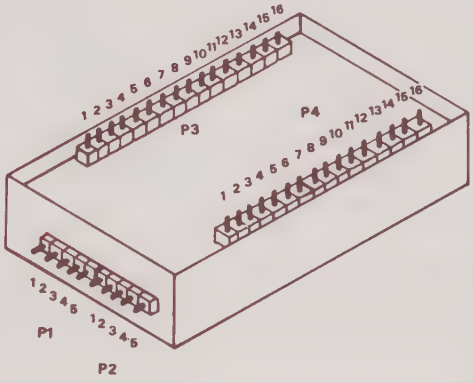
P1
Connects to Front
Panel A

Pin No.	Signal Name
1	DET A IN
2	DET A RTN
3	DET A SHLD
4	DET A OS
5	DET A THRM

P2
Connects to Front
Panel B

Pin No.	Signal Name
1	DET B IN
2	DET B RTN
3	DET B SHLD
4	DET B OS
5	DET B THRM





P4
Connects to A3J2

Pin No.	Signal Name
1	OFFSET POT B
2	THERMISTOR B
3	SHIELD B
4	DET RTN B
5	DET BAL B
6	CM DRV B
7	[4]
8	DET RTN A
9	[6]
10	[6]
11	AUTO BAL
12	CM DRV A
13	HIGH QUAL GND
14	DET BAL A
15	OP AMP V+
16	OP AMP OUT

P3
Connects to A3J3

Pin No.	Signal Name
1	+15V
2	HCG*
3	+5V
4	SHIELD A
5	OFFSET POT A
6	THERMISTOR A
7	GUARD
8	[5]
9	[2]
10	[1]
11	[3]
12	[3]
13	LOW LEVEL TRACK B
14	OP AMP FB
15	OP AMP V-
16	LOW LEVEL TRACK A

* High Current Ground

Figure 7-35. Pinout Charts, Input Module Connectors

As shown in Figure 7-34, the input module consists of a switch matrix and an operational amplifier. The detected A and B input signals, both signal and return, provide the inputs to the switch matrix. In accordance with the logic state of the LDETA control signal from the Digital (A2) PCB (not shown), the + input to the operational amplifier will be either the detected A (DET A IN) or the detected B (DET B IN) input signal. The HIGH QUAL GND output signal will be either the detected A return (DET A RTN) or the detected B return (DET B RTN) signal. The output signal from the operational amplifier, OP AMP OUT, provides the input for the 3-Stage Linear Amplifier circuit.

7-6.3 Channel A Local Isolated-Ground Driver and +/— 15V Regulator Circuits

These two circuits are described below. A parts locator diagram is shown in Figure 7-37, and the schematic is shown in Figure 7-38.

a. Channel A Local Isolated-Ground Driver Circuit. This circuit provides the reference input to 15 volt regulators U2 and U3. This U2 and U3 reference input is a voltage from a low-impedance source that is equal to the Channel A RF detector (or SWR Autotester) common-mode voltage. The common-mode voltage is the voltage present on the detector (or SWR Autotester) case that is common to both the input and the return signals. The isolated-ground driver circuit consists of operational amplifier U1A and associated components.

b. Channel A ±15 Volt Regulator Circuit. The two 15 volt regulators U2 and U3 provide the V_{CC} voltages for operational amplifiers U1A, U1B, U1C, and U1D. These four amplifiers are used to process the Channel A detector (or SWR Autotester) thermistor and offset voltages, and to provide opposite channel and chassis common-mode signal rejection for the Channel A input signal (paragraphs 7-6.4 and 7-6.5). With the V_{CC} supply referenced as described, interference normally attributed to common-mode signals is cancelled.

7-6.4 Channel A Temperature and Offset Bridge Circuits

These circuits are described below. A parts locator diagram is shown in Figure 7-37, and the schematic is shown in Figure 7-38.

a. Channel A Temperature Bridge Circuit. This circuit converts the temperature of the RF detector (or SWR Autotester), as sensed by a thermistor, to a voltage. This voltage is equal to 387 mV per degree C., with 0 volts equal to 25°C. The thermistor bridge consists of operational amplifier U1C and associated components. The output of U1C goes to the contacts of FET switch U6C. The ③ control line from the Channel A&B Multiplexer circuit (paragraph 7-6.14) controls U6C. When Channel A is selected (paragraph 7-7.12), the ③ control line goes LOW and closes the U6C switch contacts. The output of U6C, THERM A, goes to the Channel A&B Temperature Separator circuit.

b. Channel A Offset Bridge Circuit. This circuit converts the resistance of the Channel A RF detector offset potentiometer to a voltage. (In the SWR Autotester, the offset potentiometer is replaces by a fixed 1 MΩ resistor.) The offset bridge consists of operational amplifier U1B and associated components. The output of U1C goes to FET switch U6B, whose operation is the same as U6C, above. The output of U6B, OS A, goes to the dBm Normalizer circuit.

The offset potentiometer in the RF detector compensates for the minute differences that like diodes have in their operational characteristics. When the resistance of this potentiometer is set according to factory specifications, the field-replaceable-detector module presents a standard RF power-in versus dc voltage-out to the A B channel log amplifier circuits.

7-6.5 Cross-Channel and Chassis Common-Mode Signal-Rejection Circuit

This circuit cancels (rejects) the off-channel (channel not currently selected (paragraph 7-7.12)) and chassis common-mode signals; whereby preventing these signals from causing interference to the on-channel's input signal. A simplified schematic of this circuit is shown in Figure 7-36, a parts locator diagram is shown in Figure 7-37, and the schematic is shown in Figure 7-38.

As shown in Figure 7-36, the Channel A signal return line (DET RTN A) goes to operational amplifier U1A, and the Channel B signal return line (DET RTN B) goes to operational amplifier U8A. These two return lines contain their respective channel's common-mode signal, regardless of whether the channel has been selected. Amplifier U1A buffers the DET RTN A signal and applies it to the non-inverting (+) input of U1D, and via R304 and R305, to the reference input of U8D. Amplifier U8A buffers the DET RTN B signal and applies it to the non-inverting (+) input of U8D, and, via R301 and R300, to the reference input of U1D. The chassis common-mode signal is also summed into the reference input of U1D, via R302, and into the reference input of U8D, via R306. The output of U1D is the CMA signal minus the CMB and the CM (common mode) chassis signals. Factory adjustable potentiometer R301 permits the Channel B and chassis common-mode signals to be completely cancelled when Channel A is selected. The output of U8D and the operation of potentiometer R304 is the same as described for U1D and R301.

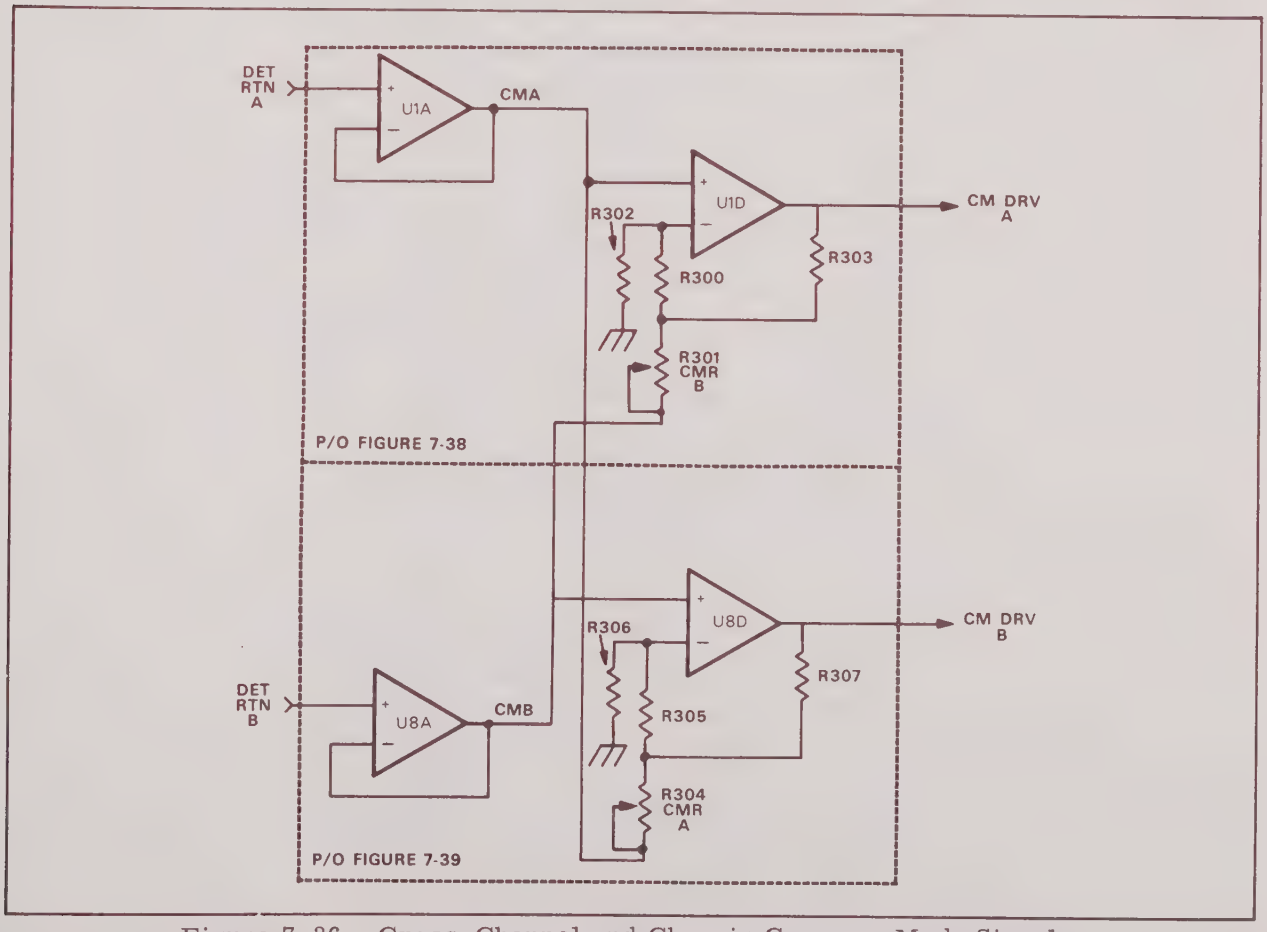


Figure 7-36. Cross-Channel and Chassis Common-Mode Signal-Refection Circuit, Simplified Schematic

TEST POINT VOLTAGE CHART

Test Point	Voltage	Schematic Location	Remarks
TP19	+15 ± 0.6Vdc	3D	1. Select Channel A for display (CHANNEL A ON pushbutton depressed; CHANNEL B ON pushbutton not depressed. 2. Reference measurement to TP4.
TP20	-15 ± 0.6Vdc	4C	

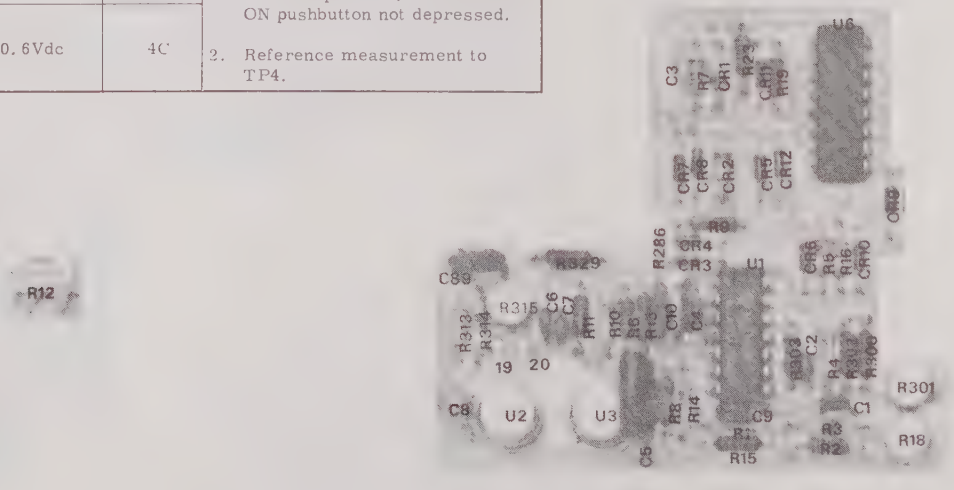
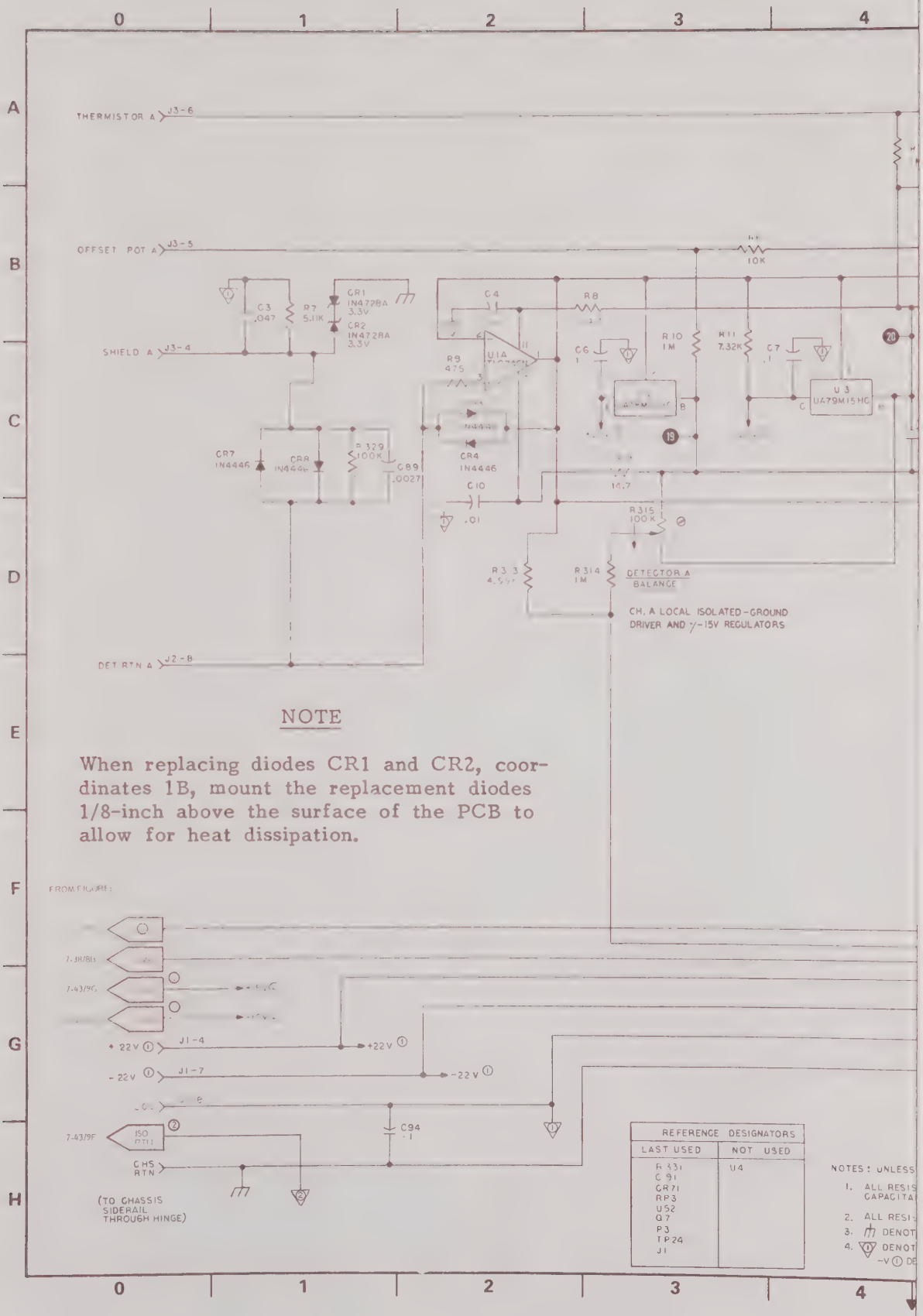


Figure 7-37. Log Amplifier (A3) PCB Channel A Local Isolated-Ground Driver, ±15V Regulator, Temperature Bridge, Offset Bridge, and Cross-Channel and Chassis Common-Mode Rejection Circuits Parts Locator Diagram



NOTE

When replacing diodes CR1 and CR2, coordinates 1B, mount the replacement diodes 1/8-inch above the surface of the PCB to allow for heat dissipation.

REFERENCE DESIGNATORS	
LAST USED	NOT USED
R331	U4
C91	
GR71	
RP3	
U52	
Q7	
P3	
TP24	
J1	

NOTES: UNLESS
1. ALL RESIS CAPACITA
2. ALL RESI
3. DENOT
4. DENOT -V DE

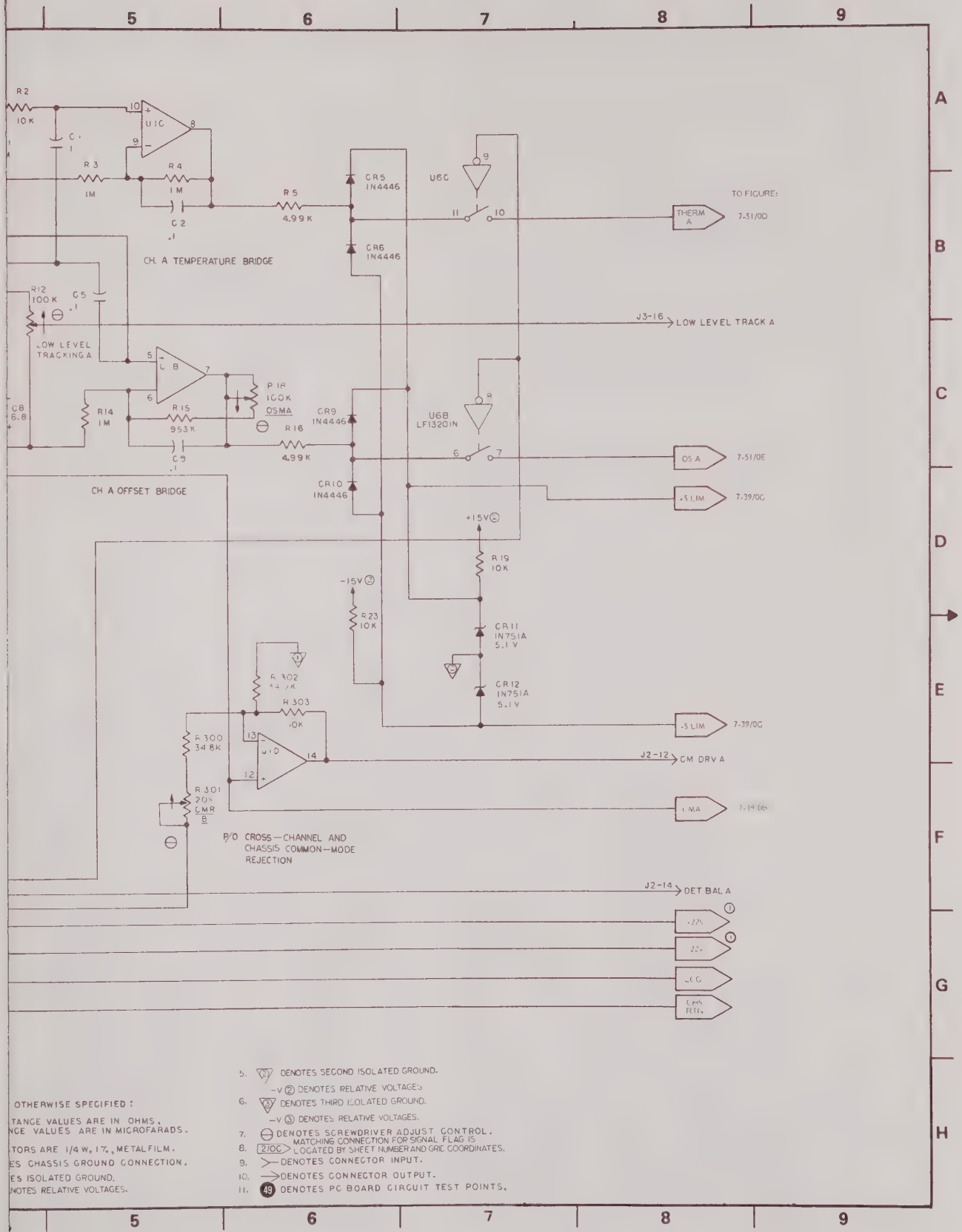


Figure 7-38. Log Amplifier (A3) PCB Channel A Local Isolated-Ground, Driver, ±15V Regulator, Temperature Bridge, Offset Bridge, and Cross-Channel and Chassis Common-Mode Rejection Circuits Schematic Diagram

Figure 7-37

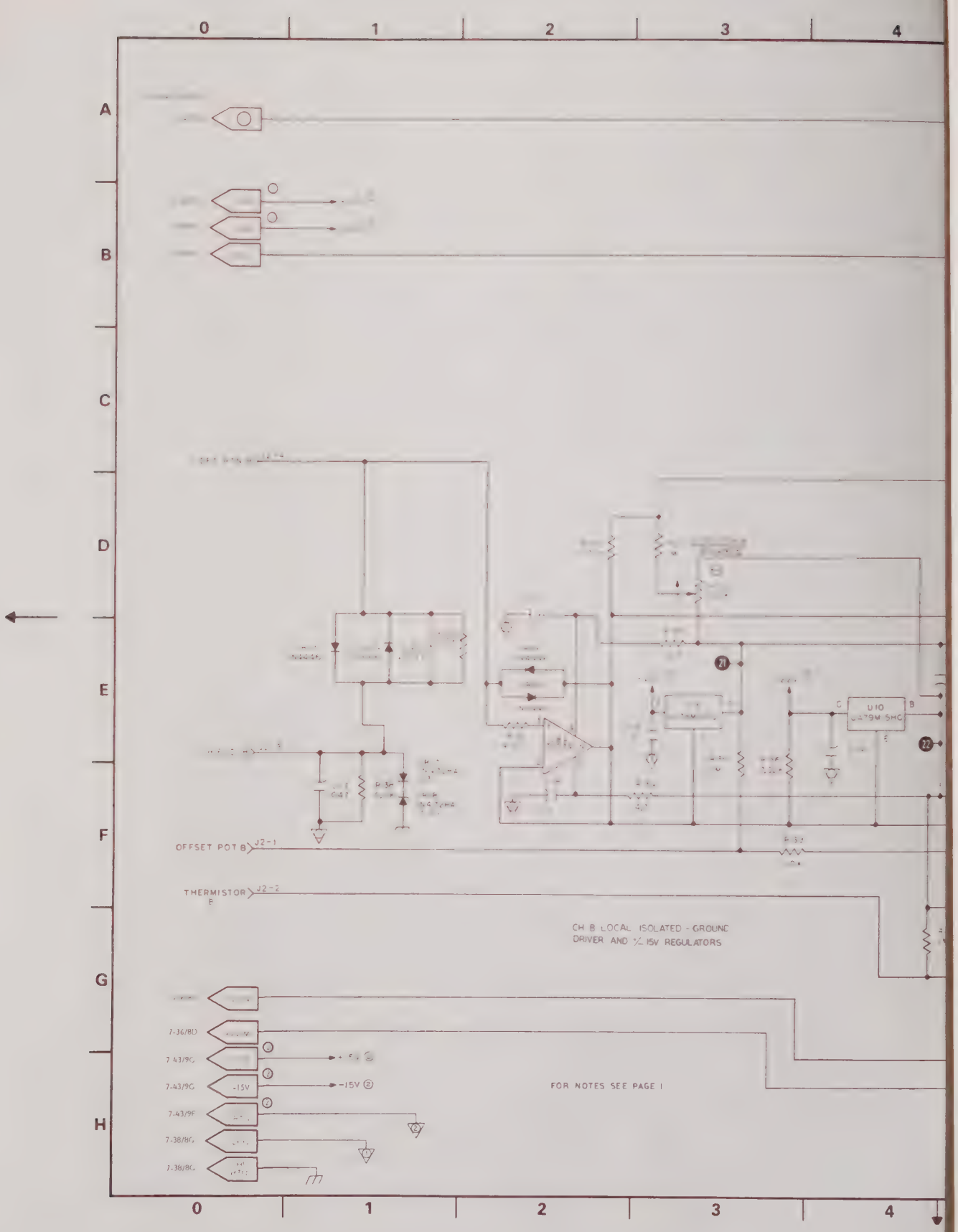
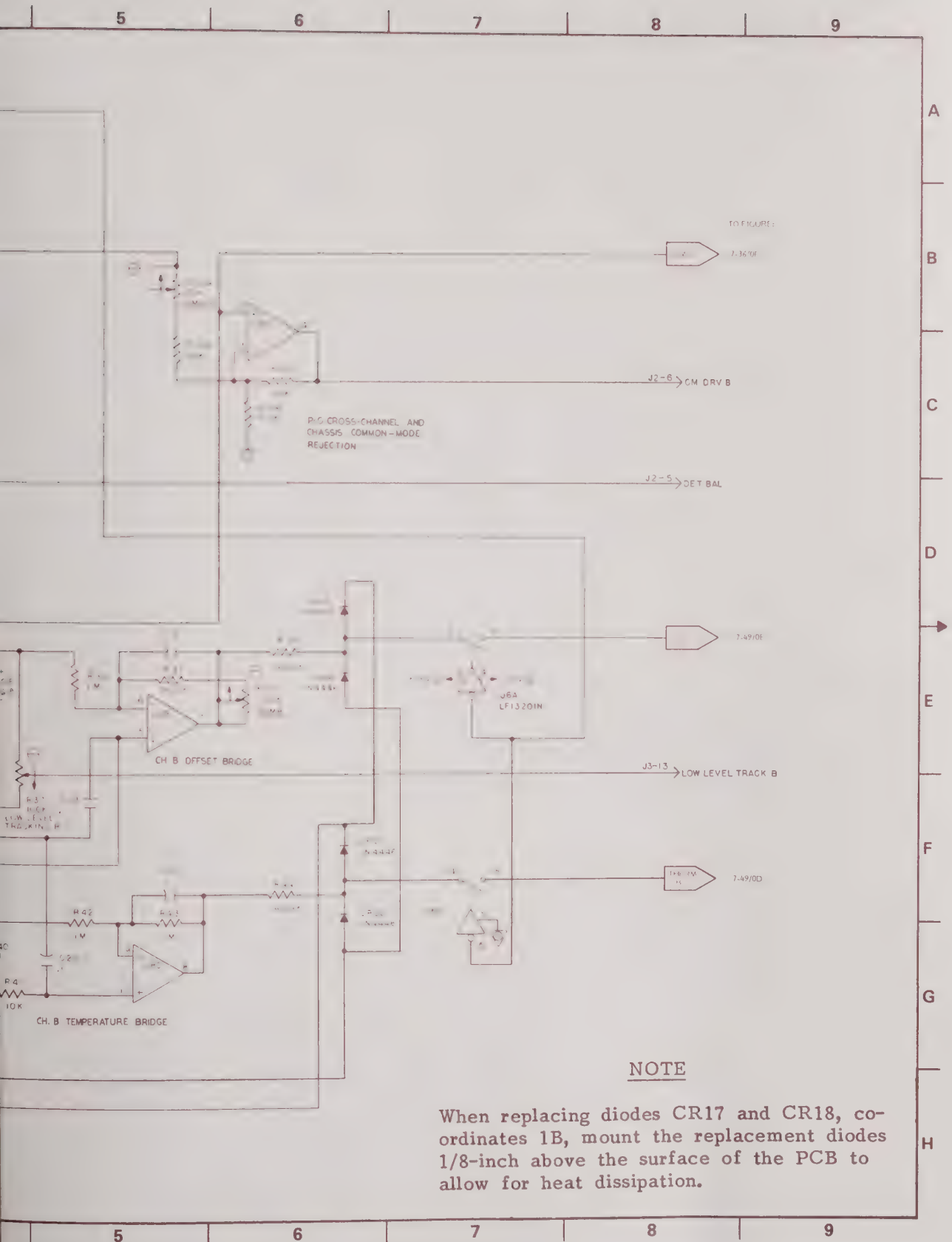
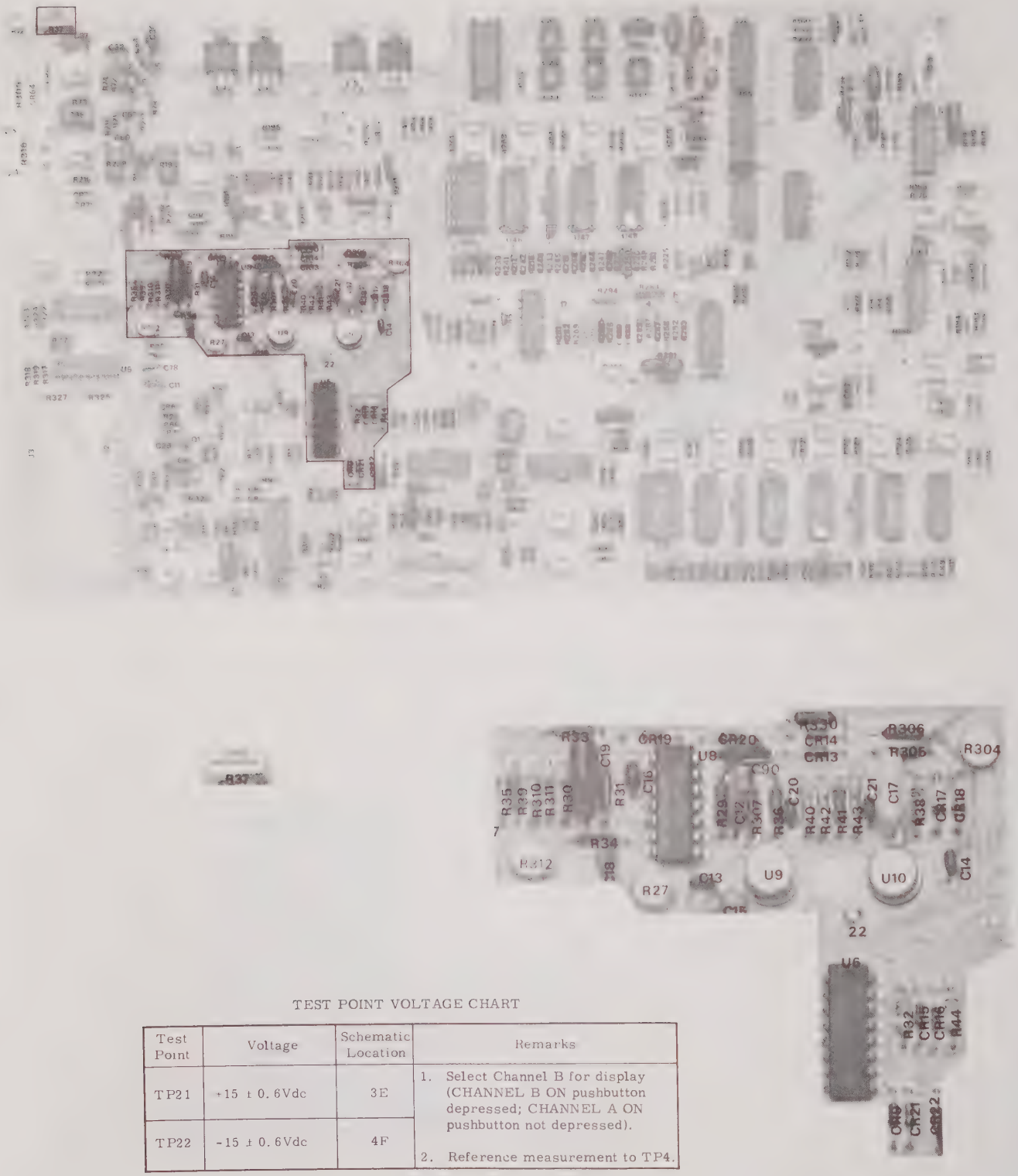


Figure 7-39. Log Amplifier (A3) PCB Channel B Local Isolated-Ground Driver, ±15V Regulator, Temperature Bridge, and Offset Bridge Circuits Schematic Diagram



NOTE

When replacing diodes CR17 and CR18, coordinates 1B, mount the replacement diodes 1/8-inch above the surface of the PCB to allow for heat dissipation.



TEST POINT VOLTAGE CHART

Test Point	Voltage	Schematic Location	Remarks
TP21	+15 ± 0.6Vdc	3E	1. Select Channel B for display (CHANNEL B ON pushbutton depressed; CHANNEL A ON pushbutton not depressed). 2. Reference measurement to TP4.
TP22	-15 ± 0.6Vdc	4F	

Figure 7-40. Log Amplifier (A3) PCB Channel B Local Isolated-Ground Driver, ±15V Regulator, Temperature Bridge, and Offset Bridge Circuits Parts Locator Diagram

Figure 7-39.

7-6.6 Channel B Local Isolated-Ground Driver and +/— 15V Regulator Circuits

These circuits are described below. The schematic is shown in Figure 7-39, and the parts locator diagram is shown in Figure 7-40.

a. Channel B Local Isolated-Ground Driver Circuit. This circuit provides the reference input to 15 volt regulators U9 and U10. This U9 and U10 reference input is a voltage from a low-impedance source that is equal to the Channel A RF detector (or SWR Autotester) common-mode voltage. The common-mode voltage is the voltage present on the detector (or SWR Autotester) case that is common to both the input and the return signals. The isolated-ground driver circuit consists of operational amplifier U8A and associated components.

b. Channel B ±15 Volt Regulator Circuit. The two 15 volt regulators U9 and U10 provide the V_{CC} voltages for operational amplifiers U8A, U8B, U8C, and U8D. These four amplifiers are used to process the Channel B detector (or SWR Autotester) thermistor and offset voltages, and to provide opposite channel and chassis common-mode signal rejection for the Channel B input signal (paragraphs 7-6.7 and 7-6.5). With the V_{CC} supply referenced as described, interference normally attributed to common-mode signals is cancelled.

7-6.7 Channel B Temperature and Offset Bridge Circuits

These circuits are described below. The schematic is shown in Figure 7-39, and the parts locator diagram is shown in Figure 7-40.

a. Channel B Temperature Bridge Circuit. This circuit converts the temperature of the RF detector (or SWR Autotester), as sensed by a thermistor, to a voltage. This voltage is equal to 387mV per degree C., with 0 volts equal to 25°C. The thermistor bridge consists of operational amplifier U8C and associated components. The output of U8C goes to the contacts of FET switch U6D. The ⑥ control line from the Channel A&B multiplexer circuit (paragraph 7-6.14) controls U6D. When Channel B is selected (paragraph 7-7.12), the ⑥ control line goes LOW and closes the U6D switch contacts. The output of U6D, THERM B, goes to the Channel A&B Temperature Separator circuit.

b. Channel B Offset Bridge Circuit. This circuit converts the resistance of the Channel B RF detector offset potentiometer to a voltage. (In the SWR Autotester, a 1MΩ resistor replaces the offset potentiometer.) The offset bridge consists of operational amplifier U8B and associated components. The output of U8B goes to FET switch U6A, whose operation is the same as U6D, above. The output of U6A, OS B, goes to the dBm Normalizer circuit.

The offset potentiometer in the RF detector compensates for the minute differences that like diodes have in their operational characteristics. When the resistance of this potentiometer is set according to factory specifications, the field-replaceable-detector module presents a standard RF power-in versus dc voltage-out to the A&B channel log amplifier circuits.

7-6.8 Channel A&B Switched Isolated-Ground Driver and +/— 15 Volt Regulator Circuits

These circuits are described below. A parts locator diagram is shown in Figure 7-42, and the schematic is shown in Figure 7-43.

a. Channel A&B Switched Isolated-Ground Driver Circuit. This circuit provides the reference input for 15 volt regulators U16 and U17. This U16 and U17 reference input is a voltage from a low-impedance source that is equal to the selected channel (paragraph 7-7.12) detector's (or SWR Autotester's) common-mode voltage.

The common-mode voltage is the voltage present on the detector (or SWR Autotester) case that is common to both the input and return signals. The isolated-ground driver consists of operational amplifier U18 and associated components.

b. Channel A&B ±15 Volt Regulator Circuit. The two 15 volt regulators U16 and U17 provide the V_{CC} voltages for all of the Channel A&B circuits, except the Common-Mode Subtractor (U39A), Test Summer (U39C), and -R Summer (U39D) and Inverter (U39B) circuits. With the V_{CC} supply referenced as described in subparagraph a, above, interference normally attributed to common-mode signals is cancelled.

7-6.9 Autozero Circuit

This circuit, when enabled by sweeper retrace or GPIB programming, closes a loop making the Channel A&B 3-Stage Linear Amplifier circuit a closed-loop amplifier system. Closing the amplifier loop and either (1) switching the RF detector (or SWR Autotester) out of the input circuit or (2) leaving the RF detector (or SWR Autotester) in the circuit with the RF source turned off has the effect of automatically cancelling (zeroing) any residual error-signals that remain on the amplifier input. A simplified schematic of the circuit is shown in Figure 7-41, a parts locator diagram is shown in Figure 7-42, and the full schematic is shown in Figure 7-43.

There are two methods for accomplishing log amplifier autozeroing. The normal method, as used by the 560A, is to electronically switch the RF detector (or SWR Autotester) out of the input circuit and at the same time provide the Autozero circuit with an enabling signal. This method cancels the effects of all dc error sources from the Input Module switch matrix to the amplifier input. For local (front panel) operation when the rear panel LOW LEVEL CAL switch is in the NORM position, normal autozeroing occurs automatically during sweep retrace. For remote (GPIB) operation, normal autozeroing occurs when the controller sends the LC command over the bus.

The alternate method of autozeroing, which

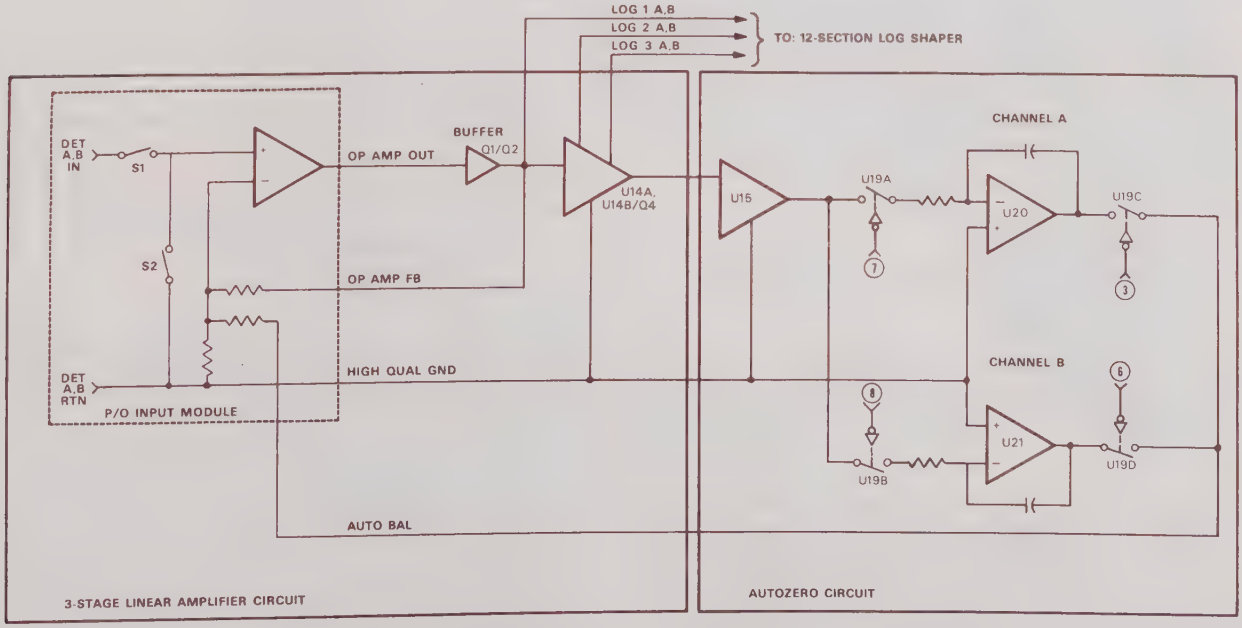


Figure 7-41. Autozero Circuit, Simplified Schematic

can be used by the 560A, is to leave the RF detector (or SWR Autotester) in the circuit and electronically turn the RF source off when the autozero circuit is enabled. This method is known as external calibrate; it cancels the effects of all dc error sources from the RF detector (or SWR Autotester) to the amplifier input.

NOTE

The external calibrate autozeroing method can be used during mixer tests for cancellation of the local oscillator leakage signal.

For local operation, External Calibrate can be accomplished by (1) placing the LOW LEVEL CAL switch in the EXTERNAL position, (2) turning the RF off during sweeper retrace, and (3) attenuating the sweeper RF output by -40 dB. The application of -40 dB of attenuation to sweep generator reduces the RF source to -60 dBm during sweep retrace. At -60 dBm, the RF source is effectively turned off.

For remote operation External Calibrate can be accomplished by (1) programming the EC command to be sent over the bus, and (2) programming the sweep generator RF source to be turned off (<-60 dBm) coincident with the EC command.

As shown in Figure 7-41, switches S1 and S2 route the detected signal (DET A, B IN) to the Input Module operational amplifier. These two switches are incorporated in the Input Module's switch matrix; they are opened and closed in accordance with the logic state of the A3 PCB LSWR input signal. When LSWR is TRUE (low), S1 is open and S2 is closed. In this switch configuration the RF detector (or SWR Autotester) is switched out of the input circuit. The LSWR control line goes LOW at the same time that the autozero circuit enabling signal (LAZ) goes LOW.

The LAZ signal and the LDETA (detector A) signal are the source signals that enable either the Channel A or the Channel B autozero circuit. When gated by the Channel A & B Autozero Logic circuit (paragraph 7.6.14), the LAZ signal, in conjunction with the LDETA signal, drives either the ⑦ and the ③ control lines LOW or the ⑧ and the ⑥ control lines LOW. When LDETA is LOW, the ⑦ and the ③ lines are driven LOW; when LDETA is HIGH, the ⑧ and the ⑥ lines are driven LOW.

7-6.10 Channel A&B 3-Stage Linear Amplifier and Smoothing Circuit

This circuit provides three stages of linear amplification, plus smoothing, for the A&B input signal (OP AMP OUT). The parts locator diagram for this circuit is shown in Figure 7-42, and the schematic is shown in Figure 7-43.

The first stage of linear amplification (Figure 7-43) consists of the operational amplifier and associated components in the A10 Input Module Assembly (Figure 7-34), and transistors Q1, Q2, and associated components in the A3 PCB assembly (Figure 7-43). This stage has a gain of 10.8; its output signal, LOG 1 A, B, goes to the high input-signal-power (+16 to approximately -20 dBm) section of the 12-Section Log Shaper circuit.

The second amplifier stage consists of operational amplifier U12, transistor Q3, and associated components. This stage is a high gain (A=-44.2) limiter-amplifier, with smoothing capacitors. The components consisting of resistor R49 and diodes CR25 thru CR27 perform the limiting function; they limit the stage output to +11.7 volts. Capacitor C24 or C25 performs the smoothing function. C24 performs smoothing for Channel A signals, and C25 performs smoothing for Channel B signals. The switching logic for these two capacitors comes from the Channel A&B Smoothing Logic circuit (paragraph 7-6.14). The output of this stage, LOG 2 A, B, goes to the medium input-signal-power (approximately -20 to -40 dBm) section of the 12-Section Log Shaper circuit.

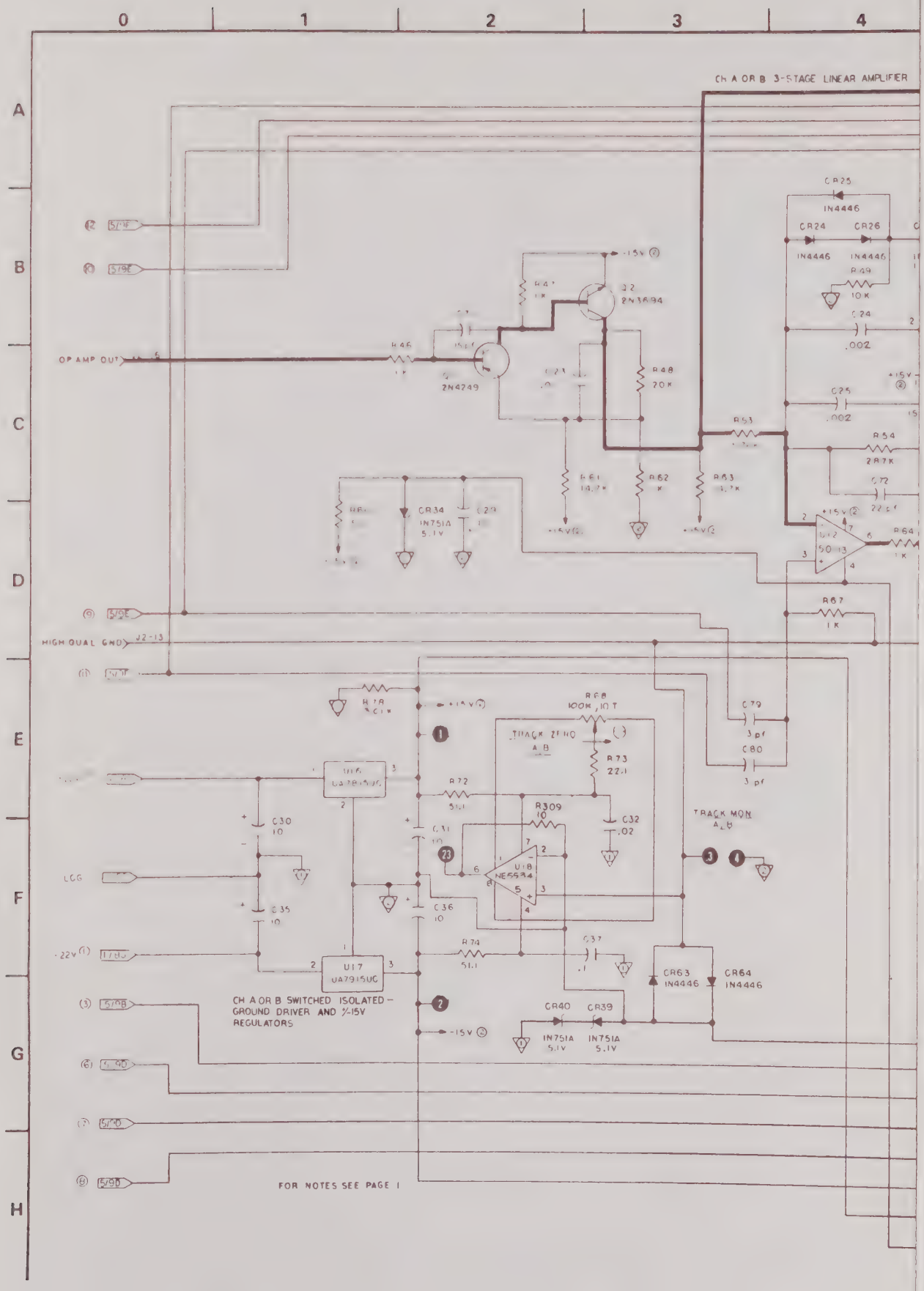
The third amplifier stage consists of operational amplifiers U14A, U14B, transistor Q4, and associated components. This stage

is also a high-gain (A=-133) limiter-amplifier, with smoothing capacitors. The components consisting of resistor R50 and diodes CR29 thru CR31 perform the limiting function; they limit the stage output to +11.7 volts. Capacitor C26 or C27 performs the smoothing function. C26 performs smoothing for Channel A signals, and C27 performs smoothing for Channel B signals. The switching logic for these to capacitors also comes from the Channel A&B Smoothing Logic circuit. The output of this stage, LOG 3 A, B, goes to the low input-signal-power (approximately -40 to -55 dBm) section of the 12-Section Log Shaper circuit.

TEST POINT VOLTAGE CHART

Test Point	Voltage	Schematic Location	Remarks
TP1	+15 ± 0.6Vdc	2F	Reference measurement to TP4.
TP2	-15 ± 0.6Vdc	2G	
TP3	0 ± 50μVdc	3F	
TP4	0 Vdc	3F	Isolated ground point.

Figure 7-42. Log Amplifier (A3) PCB Channel A&B Switched Isolated-Ground Driver, ±15V Regulator, Autozero, and 3-Stage Linear Amplifier Circuits Parts Locator Diagram


CH A OR B 3-STAGE LINEAR AMPLIFIER
OP AMP OUT
HIGH QUAL GND J2-13
LCG
-22V
TRACK MON A,B
CH A OR B SWITCHED ISOLATED - GROUND DRIVER AND +/-15V REGULATORS
FOR NOTES SEE PAGE 1

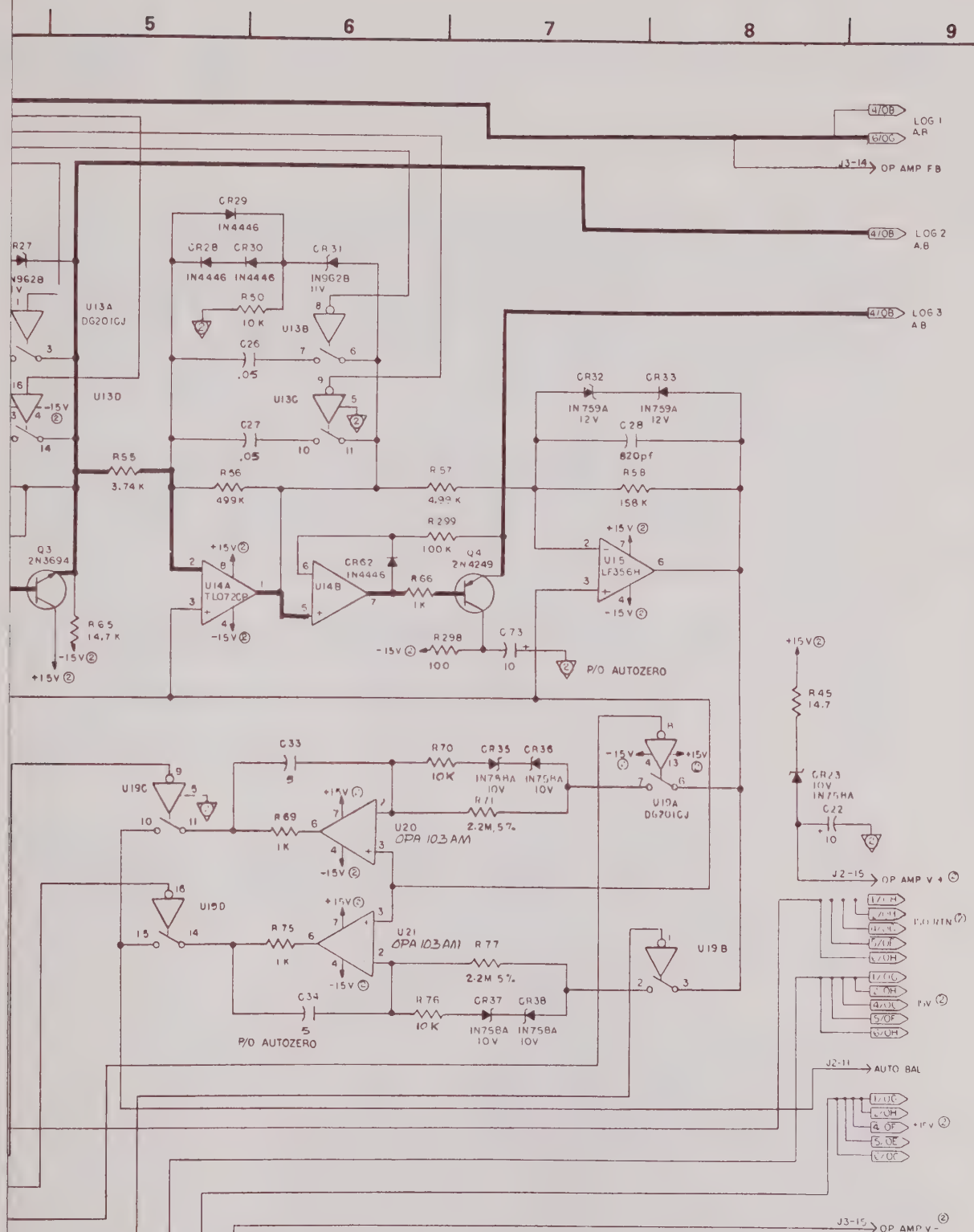
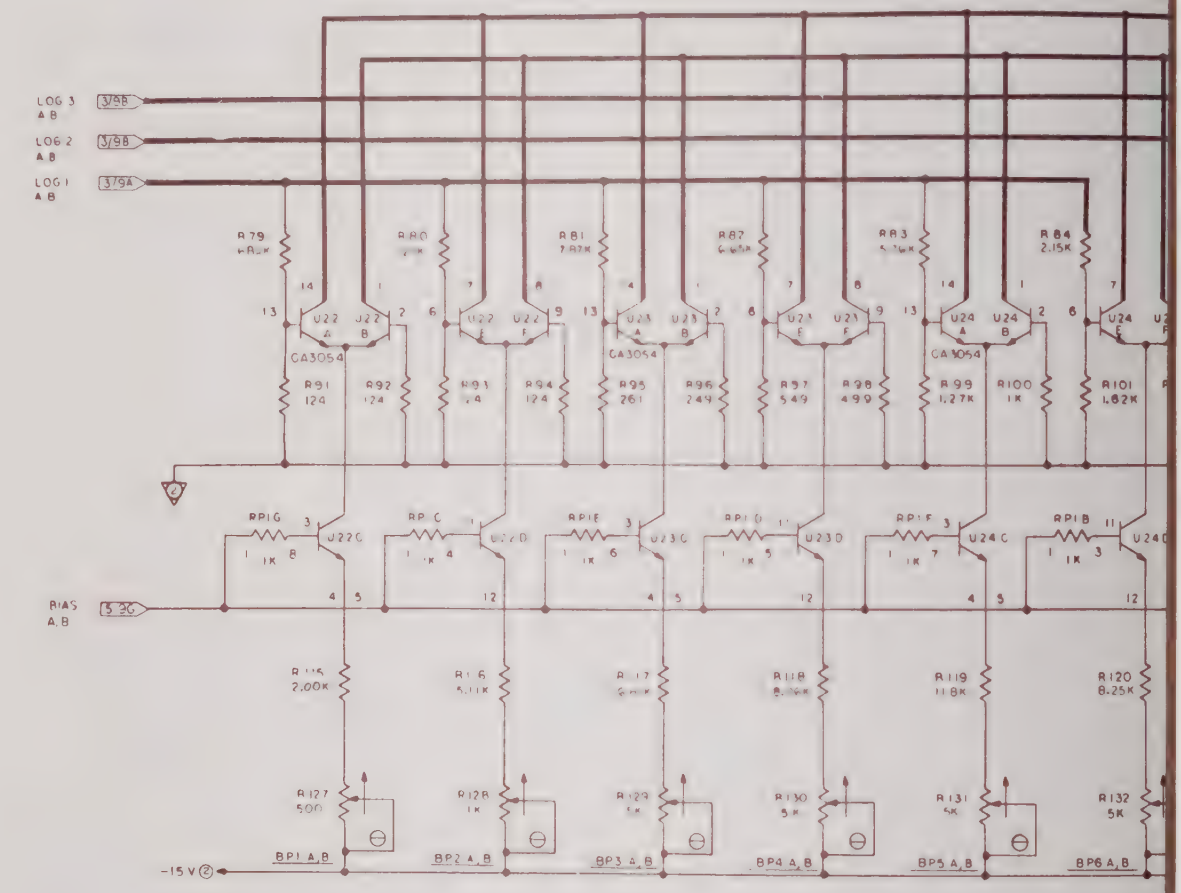


Figure 7-43 Log Amplifier (A3) PCB Channel A&B Switched Isolated Ground Driver, ±15V Regulator, Autozero, and 3-Stage Linear Amplifier Circuits Schematic Diagram

Figure 7-42.



FOR NOTES SEE PAGE 1

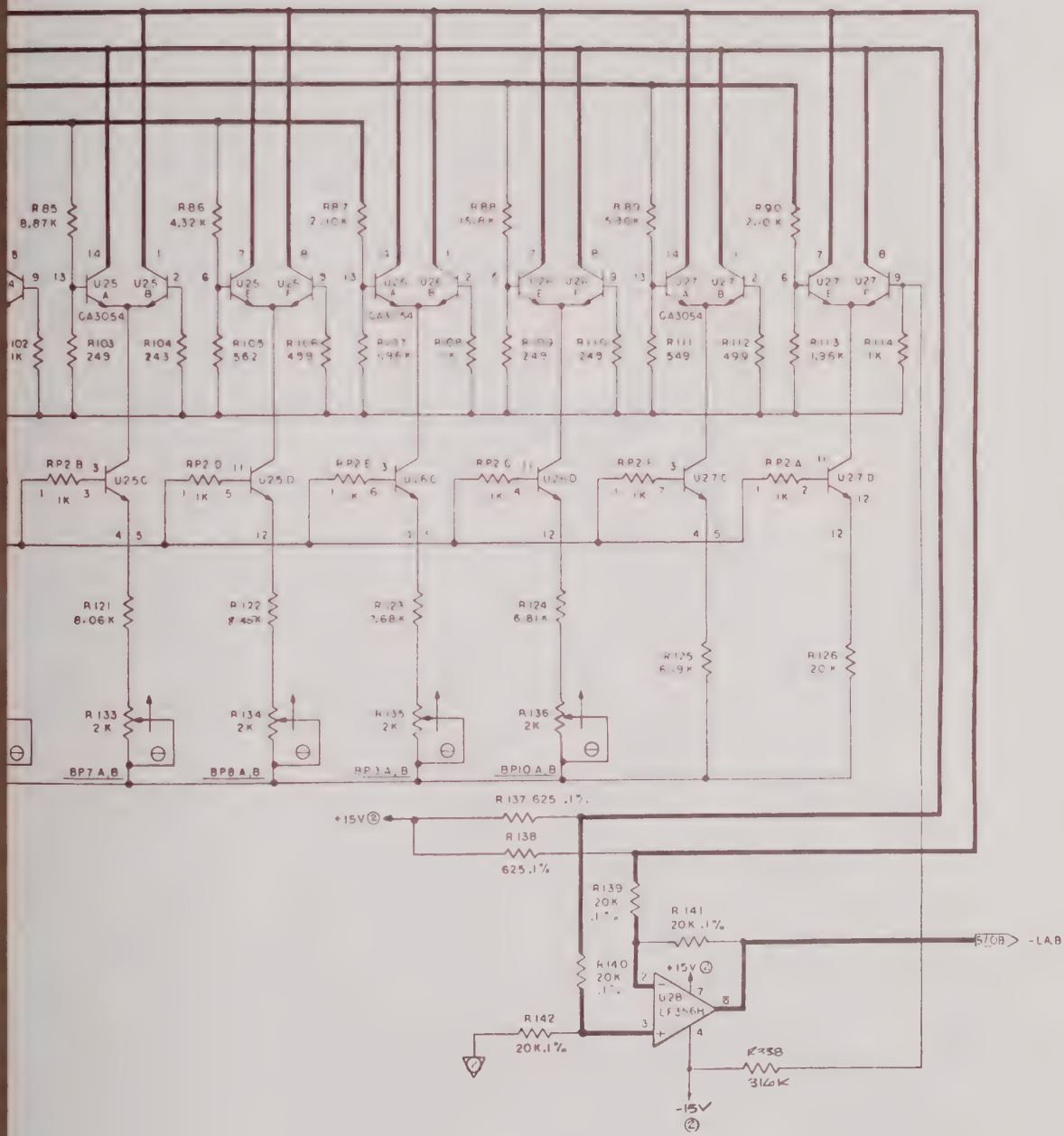


Figure 7-44. Log Amplifier (A3) PCB Channel A&B 12-Section Log Shaper Circuit Schematic Diagram

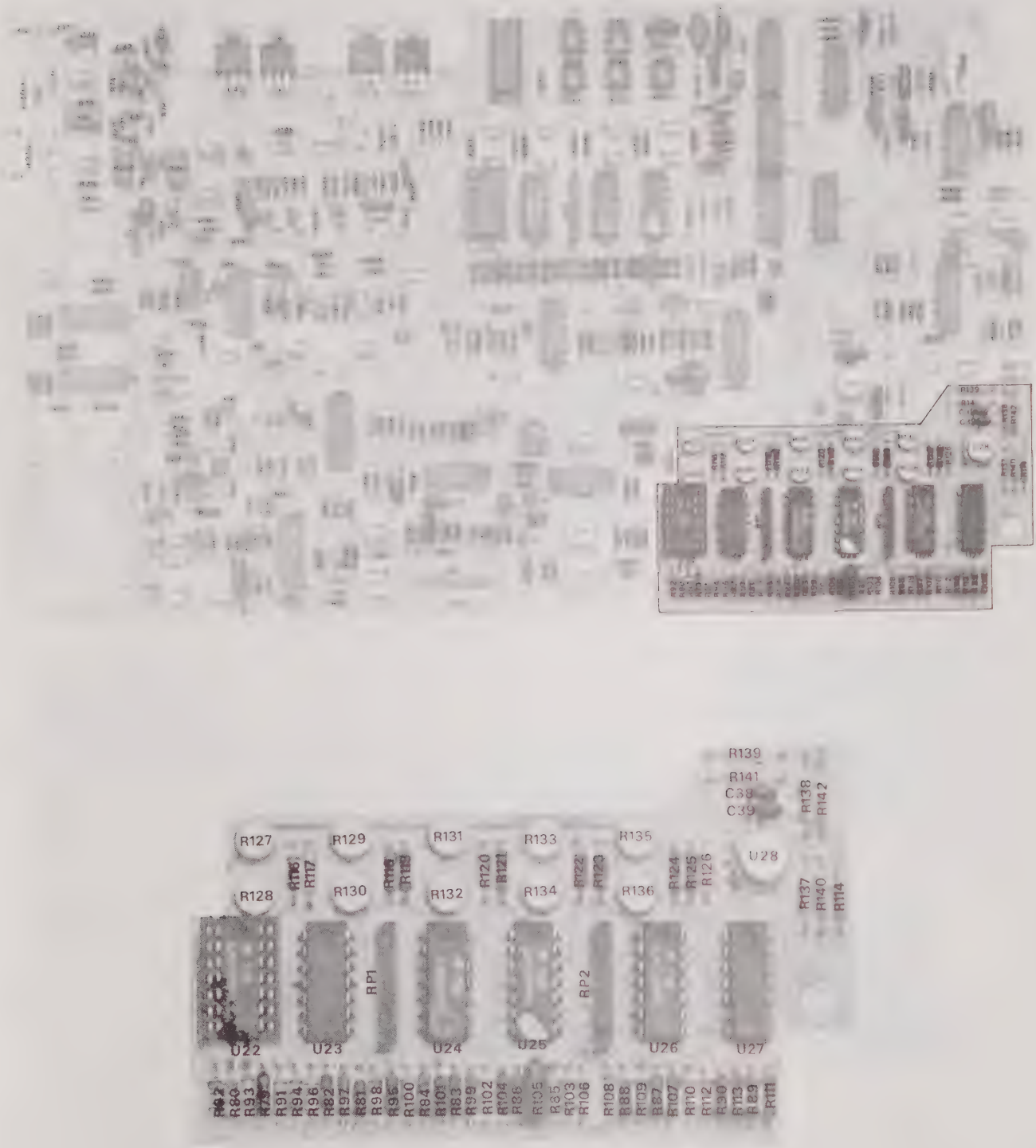


Figure 7-45. Log Amplifier (A3) PCB Channel A&B 12-Section Log Shaper Circuit Parts Locator Diagram

Figure 7-44.

7-6.11 Channel A&B 12-Section Log Shaper Circuit

This circuit shapes the sensitivity-input power response curve of the A or B channel log amplifier to compensate for variations in RF detector (or SWR Autotester) sensitivity with input power. At high input-power levels (+16 to 0 dBm), the RF detector (or SWR Autotester) sensitivity response is linear; at low input-power levels (-18 to -50 dBm), the RF detector (or SWR Autotester) sensitivity response is square-law, and at medium input-power levels (0 to -18 dBm), the RF detector (or SWR Autotester) sensitivity response is in transition between linear and square-law. A functional schematic of this circuit is shown in Figure 7-44, and the parts locator diagram is shown in Figure 7-45.

Repair and/or adjustment of this circuit is not recommended at the field level. The adjustments for log conformity, R127 thru R136, require specialized test equipment available only at the factory, or at factory authorized service centers.

7-6.12 Channel A&B Temperature Separator and Log Shaper Bias Generator Circuits

A parts locator diagram for these circuits is shown in Figure 7-50, the schematic is shown in Figure 7-51. The circuits are described below.

a. Channel A&B Temperature Separator Circuit. This circuit separates between hot (>25°C) and cold (<25°C) temperatures. The temperature separator consists of operational amplifier U38B and associated components. The resistor-diode circuit consisting of R174 and CR43 separates hot temperatures; the resistor-diode circuit consisting of R172 and CR42 separates cold temperatures. The separation is needed because the RF detector-diode's voltage-input power characteristics are degraded with hot and cold temperatures. The voltage output of this circuit in conjunction with the voltage output of the bias generator (U38C/U38D) circuit, controls log shaper bias.

b. Channel A&B Log Shaper Bias Generator Circuit. This circuit generates a bias voltage that varies with the temperature of the RF detector (or SWR Autotester). This bias voltage controls the conduction of current through the twelve log-shaper sections. The bias generator, by controlling log shaper current conduction, controls the shape of the sensitivity-input power response curve of the log shaper circuit. The bias-generator circuit consists of operational amplifiers U38C, U38D, and associated components. The output of this circuit, BIAS A, B, goes to the 12-Section Log Shaper circuit.

7-6.13 Channel A&B dBm Normalizer, Common-Mode Subtractor, Test Summer, and -R Summer and Inverter Circuits

A parts locator diagram for these circuits is shown in Figure 7-50, the schematic is shown in Figure 7-51. The circuits are described below.

a. Channel A&B dBm Normalizer Circuit. This circuit normalizes the log shaper circuit output signal for 125mV per dBm of input signal. It also sets the normalized signal so that 0 volts equals 0 dBm. The circuit consists of operational amplifier U38A, and associated components. Resistor R154 provides the 125mV/dBm adjustment; resistor R181 provides the 0 dBm adjustment.

b. Channel A&B Common-Mode Subtractor Circuit. This circuit subtracts the common-mode signal from the normalized A&B signal. The circuit consists of operational amplifier U39A and associated components. The V_{CC} voltage for this circuit comes from the digital (A2) PCB, which is a source different from that used for the other A&B log amplifier circuits. The use of different ±15 volt regulators causes this circuit's V_{CC} supply to be referenced to chassis ground instead of

isolated ground. Isolated ground, instead, provides the reference signal for the U39A non-inverting (+) input. The normalized A&B signal, referenced to isolated ground, provides the input to the U39A inverting (-) input. The U39A output is an inverted replica of the normalized A&B signal, minus the common-mode signal. The output of this circuit goes to test summer U39C.

c. Channel A&B Test Summer Circuit. This circuit provides either of two output signals, dependent upon the TEST-NORM switch position.

When the A3 PCB TEST-NORM switch is in the TEST position, the circuit adds an external 100 mV/dBm signal derived from the input horizontal ramp voltage to the A&B log amplifier output signal. The circuit output provides a vertical test signal for the performance verification and, if necessary, subsequent calibration of the digital (A2) PCB.

When the TEST-NORM switch is in the NORM position, the circuit provides unity gain for the A&B log amplifier output signal. The circuit output is the LOG A, B input signal to the front panel/digital PCB circuits.

d. -R Summer Circuit. This circuit sums the -R signal from the R Channel Log Amplifier circuit with the A&B signal from the Test Summer circuit. The circuit output provides the LOG A, B-R input to the front panel/digital PCB circuits.

e. -R Inverter Circuit. The circuit provides either of two output signals, also dependent upon TEST-NORM switch position.

When the TEST-NORM switch is in the TEST position, the circuit adds an external 100 mV/dBm signal derived from the input horizontal ramp voltage to the R channel log amplifier output signal. The circuit output provides a vertical test signal for the performance verification and, if necessary, subsequent calibration of the Digital (A2) PCB.

When the TEST-NORM switch is in the NORM position, the circuit provides inversion for the -R signal. The circuit output provides the LOG R input to the front panel/digital PCB circuits.

7-6.14 Channel A&B Demultiplexer, Switch-Reference, Autozero, and Smoothing Logic Circuits

A parts locator diagram for these circuits is shown in Figure 7-50,the schematic is shown in Figure 7-51. The circuits are described below.

a. Channel A&B Demultiplexer Logic Circuit. This circuit demultiplexes the LDETA (channel-select) control line to create individual Channel A and Channel B control signals. The circuit also triggers a one-shot multivibrator whose output pulse inhibits logic gates in the smoothing logic circuit. A simplified schematic of this circuit is shown in Figure 7-46.

The LDETA control line, (Figure 7-46), which is LOW when Channel A is selected (paragraph 7-7.12) and HIGH when Channel B is selected, is applied to optical isolator U32. U32 optically couples the LDETA signal to inverter U30D and the ± edge-sensitive one-shot multivibrator circuit consisting of EX-OR gates U52A and U52D.

The output of the U52A/U52D circuit, when triggered by either a negative-going (Channel A) or a positive-going (Channel B) U32 output pulse, produces a 300μs negative pulse. Within approximately 40μs (the time it takes the R167/C82 delay circuit to transition from a 1 to a 0) the U52A/U52D output pulse inhibits NAND gates U34C, U37A, U37B, and U37C ($FILT_1$-$FILT_2$ HENB/LINH line goes LOW). When these gates are inhibited, the logic state of the ⑨, ⑩, ⑪, and ⑫ control lines goes HIGH.

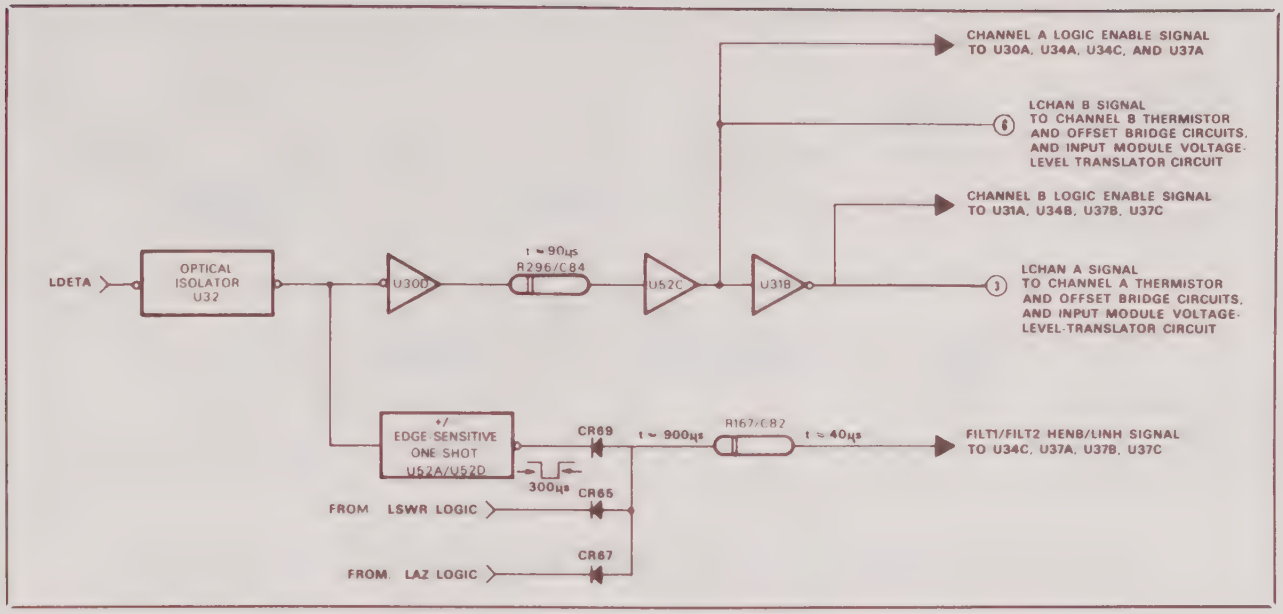

CHANNEL A LOGIC ENABLE SIGNAL TO U30A, U34A, U34C, AND U37A
LCHAN B SIGNAL TO CHANNEL B THERMISTOR AND OFFSET BRIDGE CIRCUITS, AND INPUT MODULE VOLTAGE-LEVEL TRANSLATOR CIRCUIT
CHANNEL B LOGIC ENABLE SIGNAL TO U31A, U34B, U37B, U37C
LCHAN A SIGNAL TO CHANNEL A THERMISTOR AND OFFSET BRIDGE CIRCUITS, AND INPUT MODULE VOLTAGE-LEVEL-TRANSLATOR CIRCUIT
LDETA
OPTICAL ISOLATOR U32
U30C
t ≈ 90µs R296/C84
U52C
U31B
+/- EDGE-SENSITIVE ONE-SHOT U52A/U52D
300µs
CR69
t ≈ 900µs
R167/C82
t ≈ 40µs
FILT1/FILT2 HENB/LINH SIGNAL TO U34C, U37A, U37B, U37C
FROM LSWR LOGIC
CR65
FROM LAZ LOGIC
CR67

Figure 7-46. Channel A or B Demultiplexer Logic Circuit, Simplified Schematic

If any of the smoothing filters in the Channel A&B 3-Stage Linear Amplifier circuit are switched into the amplifier circuit, the HIGH state of these four lines switches them out. Within approximately 900 µs after the U52A/U52D circuit times out, the $FILT_1$-$FILT_2$ HENB/LINH line returns to its HIGH state.

The output of U30D, after being delayed 90µs, gets split into individual Channel A and Channel B control signals. These two control signals go several places, as indicated on the simplified schematic.

b. Channel A&B SWR Logic Circuit. This circuit inverts and delays the input LSWR (switch-reference) signal and gates it with a channel-select signal from the demultiplexer logic circuit. The circuit gating action produces Channel A and Channel B switch-reference control signals. The circuit also temporarily inhibits logic gates in the smoothing logic circuit when the LSWR input signal goes LOW. A simplified schematic of this circuit is shown in Figure 7-47.

The LSWR control line (Figure 7-47) is applied to optical isolator U29. U29 optically couples the LSWR signal to inverter U30B and diode CR65, which functions as an OR gate. CR65, when it becomes forward biased, causes NAND gates U34C, U37A, U37B, and U37C to become inhibited. The circuit action of the R167/C82 delay circuit is the same as described in subparagraph a., above. U30B inverts the output of U29 and applies it to the R166/C81/CR66 delay circuit. This circuit delays the signal 70 µs and then applies it to NOR gates U30A and U31A. The output logic states of U30A and U31A are as follows:

1. U30A and U31A are both LOW when the LSWR input signal is LOW, regardless of which channel is selected.

2. U30A is LOW and U31A is HIGH when Channel A is selected and the LSWR input signal is HIGH.

3. U30A is HIGH and U31A is LOW when Channel B is selected and the LSWR input signal is HIGH.

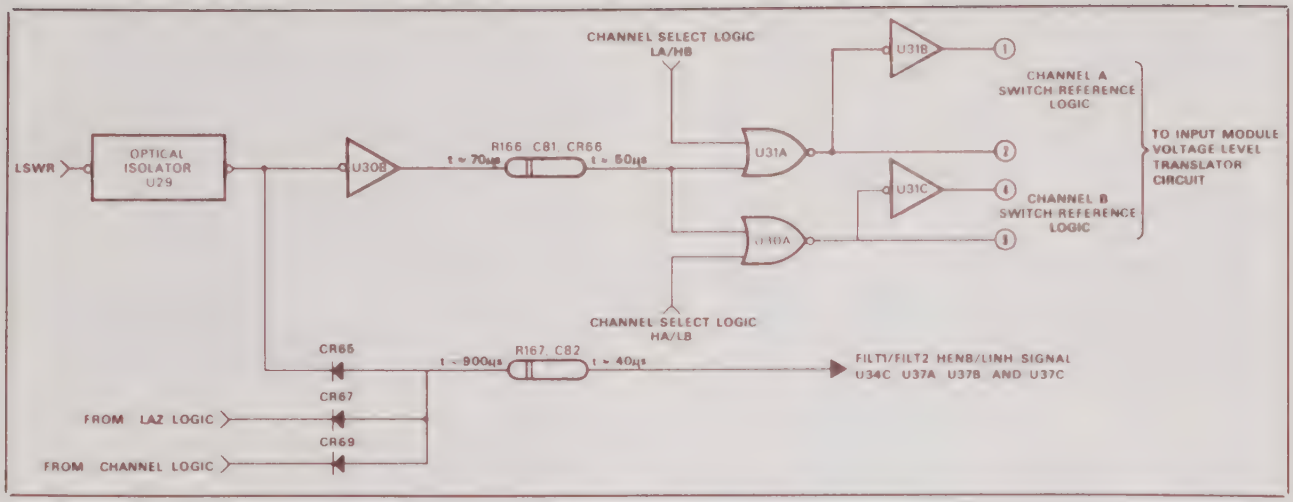


Figure 7-47. Channel A&B SWR Logic Circuit, Simplified Schematic

c. Channel A&B Autozero Logic Circuit. This circuit inverts and delays the input LAZ (autozero) signal and gates it with a channel-select signal from the demultiplexer logic circuit. The circuit gating action produces Channel A and Channel B autozero control signals. The circuit also temporarily inhibits logic gates in the smoothing logic circuit when the LAZ input signal goes LOW. A simplified schematic of this circuit is shown in Figure 7-48.

The LAZ control line (Figure 7-48) is applied to optical isolator U33. U33 optically couples the LAZ signal to inverter U30C and diode CR67, which functions as an OR gate. CR67, when forward biased, causes NAND gates U34C, U37A, U37B, and U37C to become inhibited. The circuit action of the R167/C82 delay circuit is the same as described in subparagraph a., above. U30C inverts the output of U33 and applies it to the R295/C83/CR68 delay circuit. This circuit delays the signal 300 μs and then applies it to NAND gates U34A and U34B. Only one of these gates, depending on which channel is selected, will be enabled at any one time. If Channel A is selected, U34A is enabled and its output goes LOW. Conversely, if Channel B is selected, U34B is enabled and its output goes LOW.

d. Channel A&B Smoothing Logic Circuit. This circuit inverts and gates the $LFILT_1$ (smoothing minimum) and $LFILT_2$ (smoothing maximum) input signals with (1) the channel-select logic signals from the demultiplexer logic circuit and (2) the enable/inhibit (HENB/LINH) logic signal from either the demultiplexer, switch-reference, or autozero logic circuits. The circuit gating action produces four output signals: ⑨ -Channel A $FILT_1$, ⑩ -Channel A $FILT_2$, ⑪ -Channel B $FILT_1$, and ⑫ -Channel B $FILT_2$. A simplified schematic of this circuit is shown in Figure 7-49.

The $LFILT_1$ control line (Figure 7-49) is applied to optical isolator U35; the $LFILT_2$ control line is applied to optical isolator U36. The outputs of U35 and U36 are inverted and applied to the gating circuit, where they are gated with both channel-select logic and enable/inhibit logic signals.

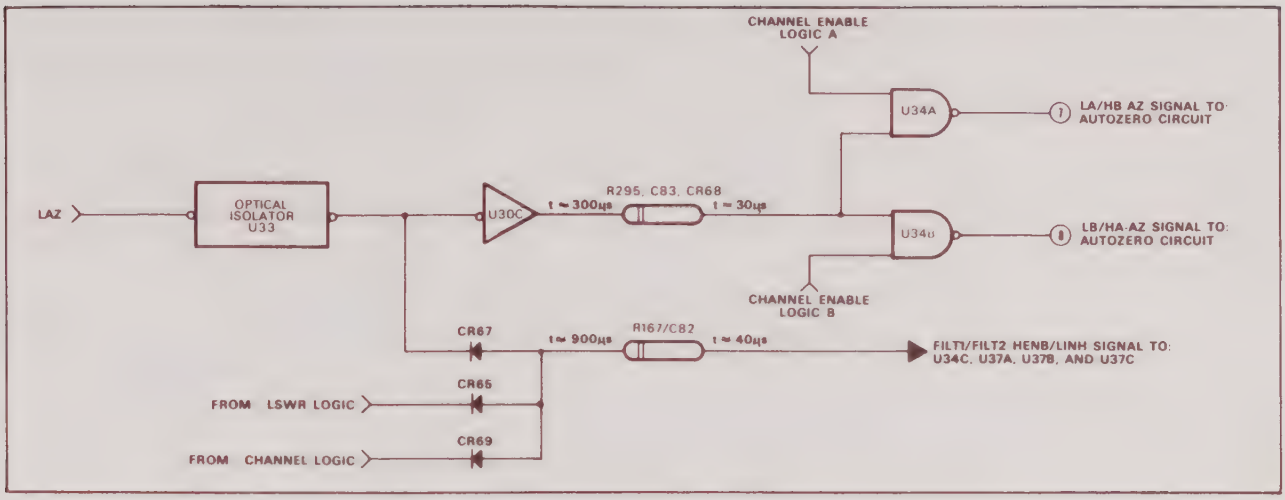


Figure 7-48. Channel A & B Autozero Logic Circuit, Simplified Schematic

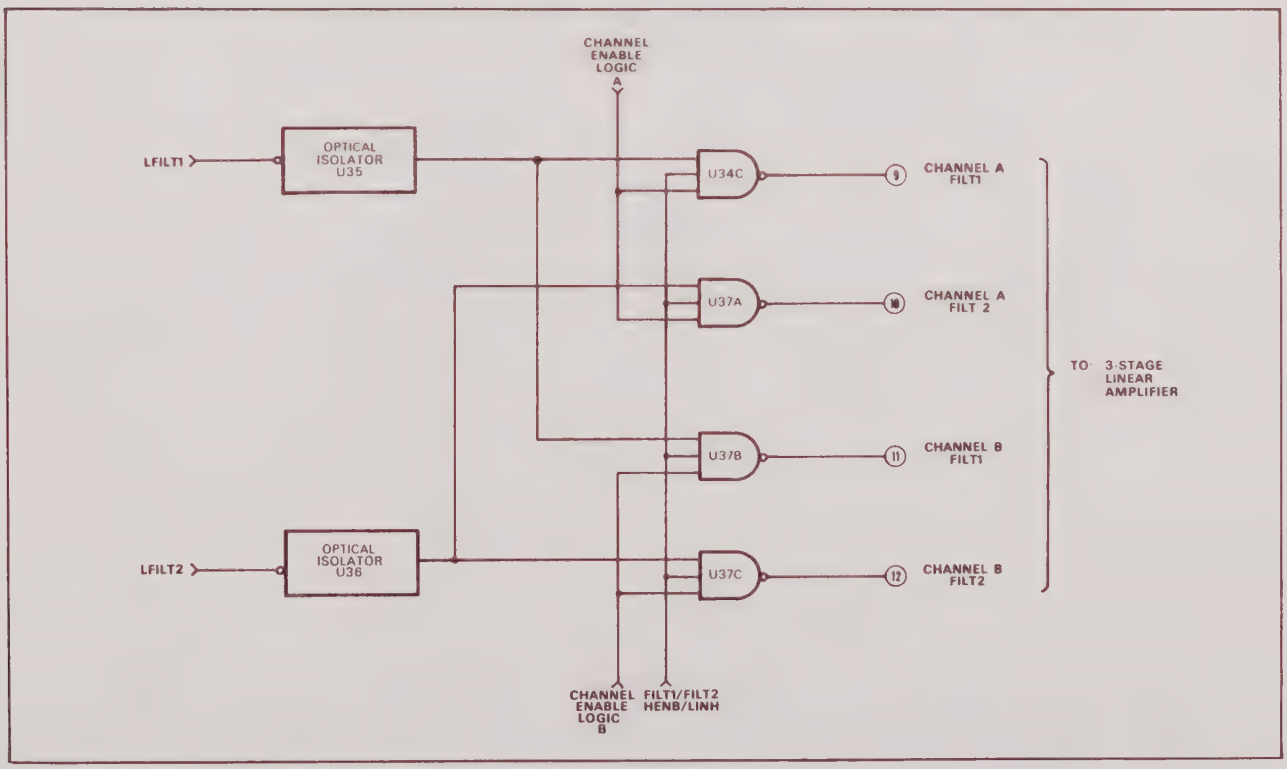
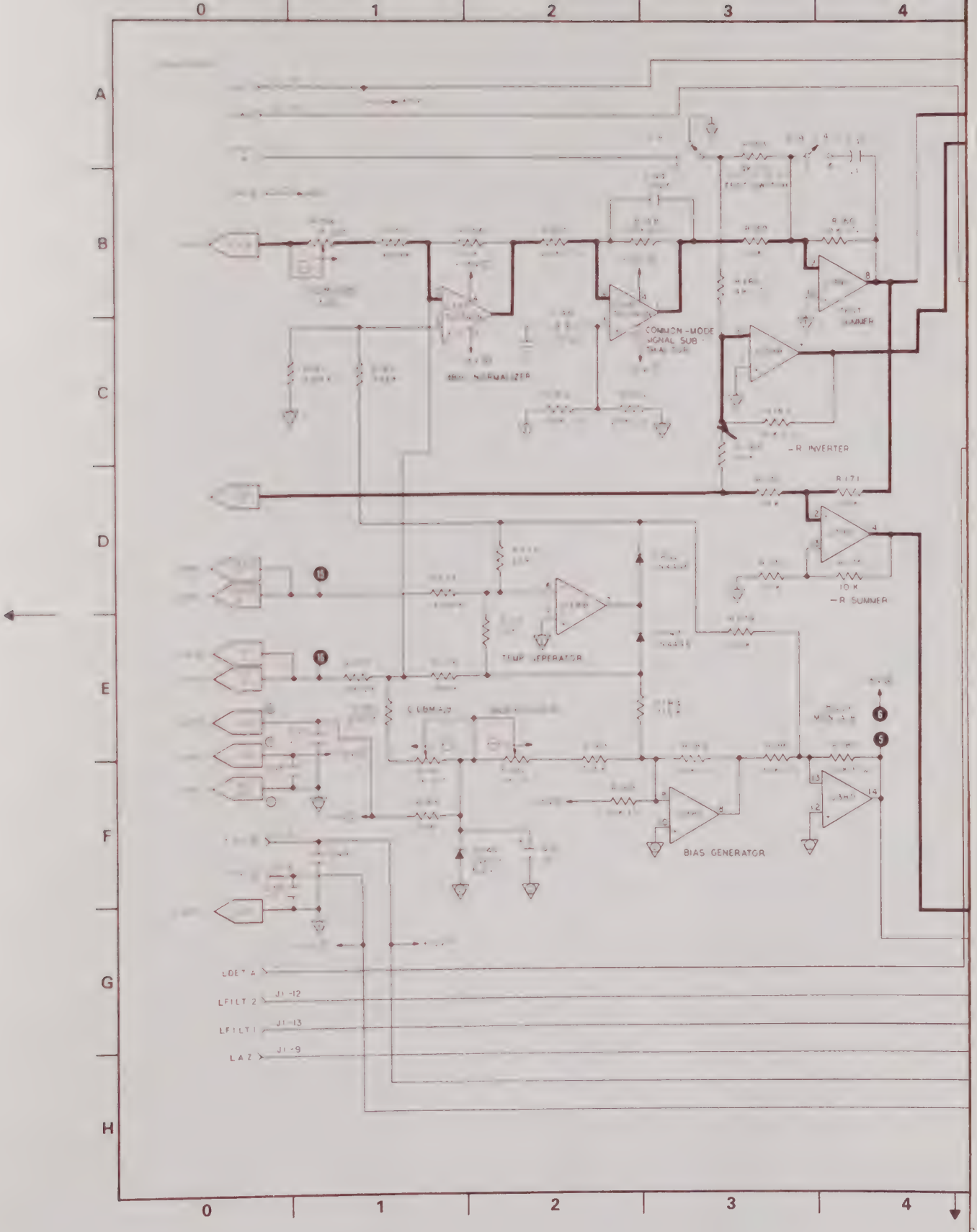


Figure 7-49. Channel A&B Smoothing Logic Circuit, Simplified Schematic

TEST POINT VOLTAGE CHART

Test Point	Voltage	Schematic Location	Remarks
TP5 & TP6	8.25 ± 0.003 Vdc	4E	1. Positive voltmeter lead to TP5; negative lead to TP6. 2. Connect simulated detector (Figure 7-29) to front panel A or B connector; select appropriate channel (refer to paragraph 7-7.12).
TP15	0 ± 100 mVdc	1D	1. Reference measurement to TP4. 2. Connect simulated detector to front panel A or B connector; select appropriate channel.
TP16	0 ± 20 mVdc	1E	

Figure 7-50. Log Amplifier (A3) PCB Channel A&B Temperature Separator, Log-Shaper Bias-Generator, dBm Normalizer, Common-Mode Signal-Subtractor, Test Summer, -R Summer, -R Inverter, and Demultiplexer, Switch-Reference, Autozero, and Smoothing Logic Circuits Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
COMMON-MODE
SIGNAL SUB
-R INVERTER
R171
10 K
-R SUMMER
TRIP GENERATOR
BIAS GENERATOR
LDET A
LFILT 2
J1-12
LFILT 1
J1-13
LAZ
J1-9

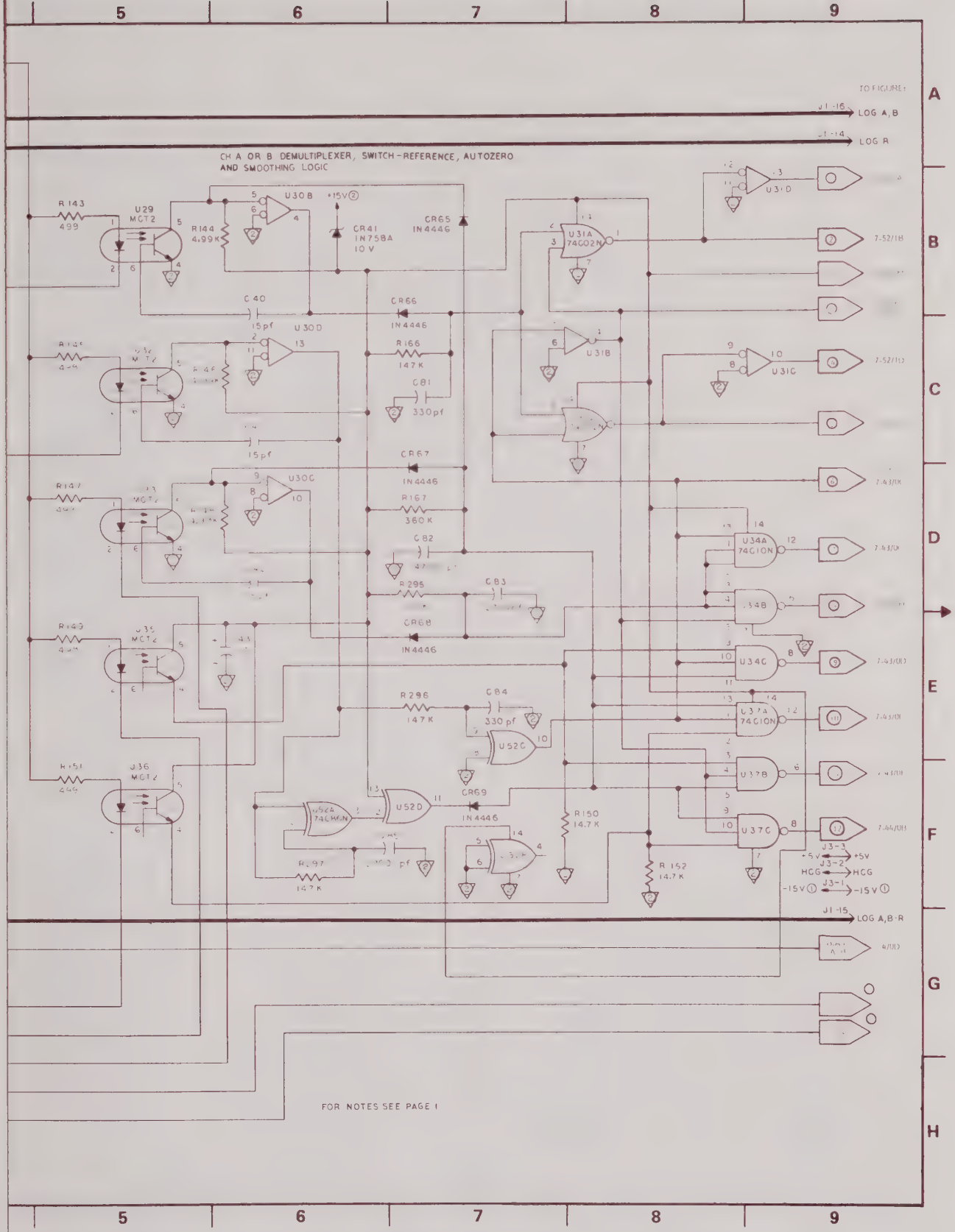


Figure 7-51. Log Amplifier (A3) PCB Channel A&B Temperature Separator, Log-Shaper Bias-Generator, dBm Normalizer, Common-Mode Signal-Subtractor, Test Summer, -R Summer, -R Inverter, and Demultiplexer, Switch-Reference, Autozero, and Smoothing Logic Circuits Schematic Diagram

Figure 7-50.

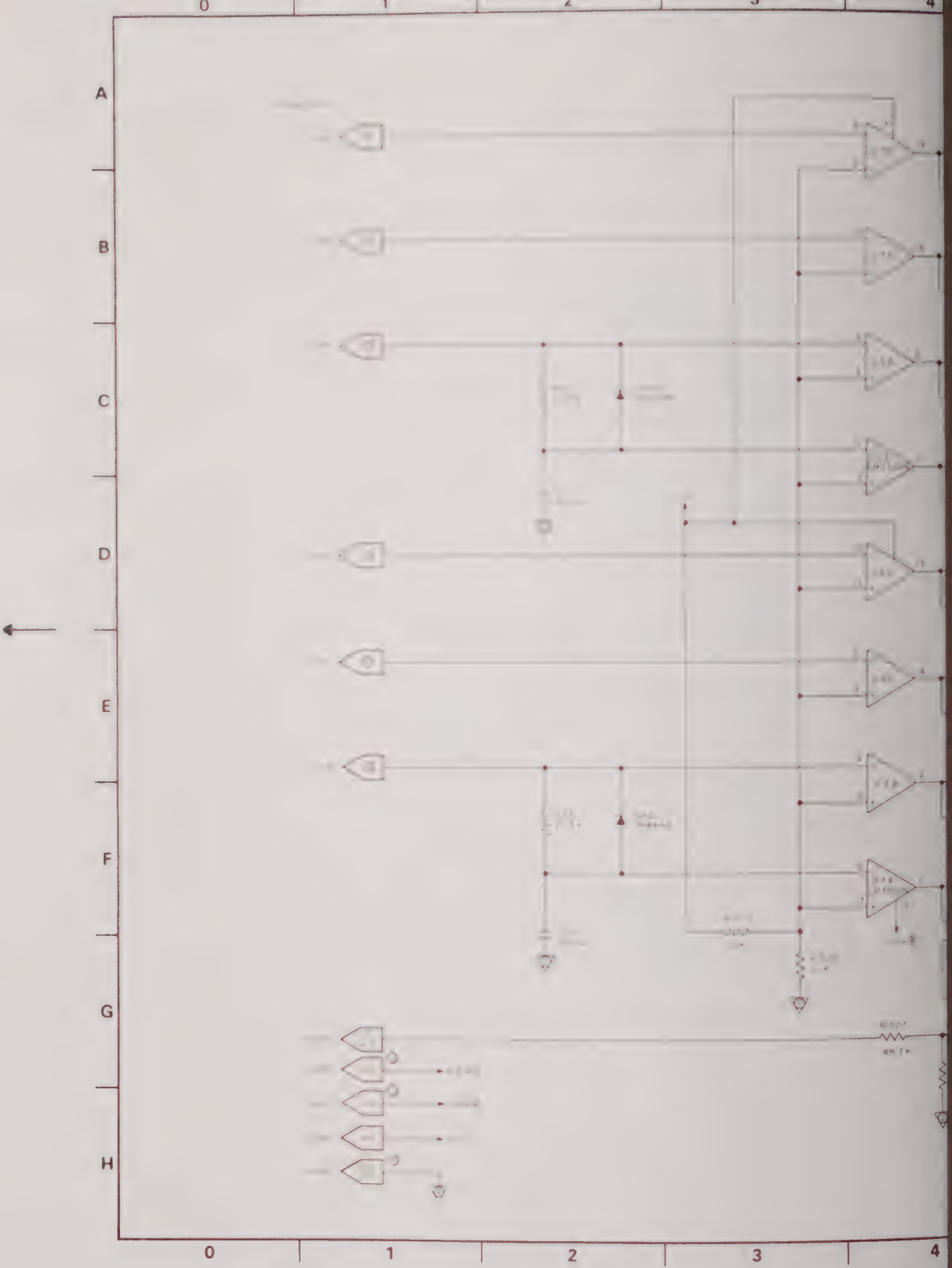
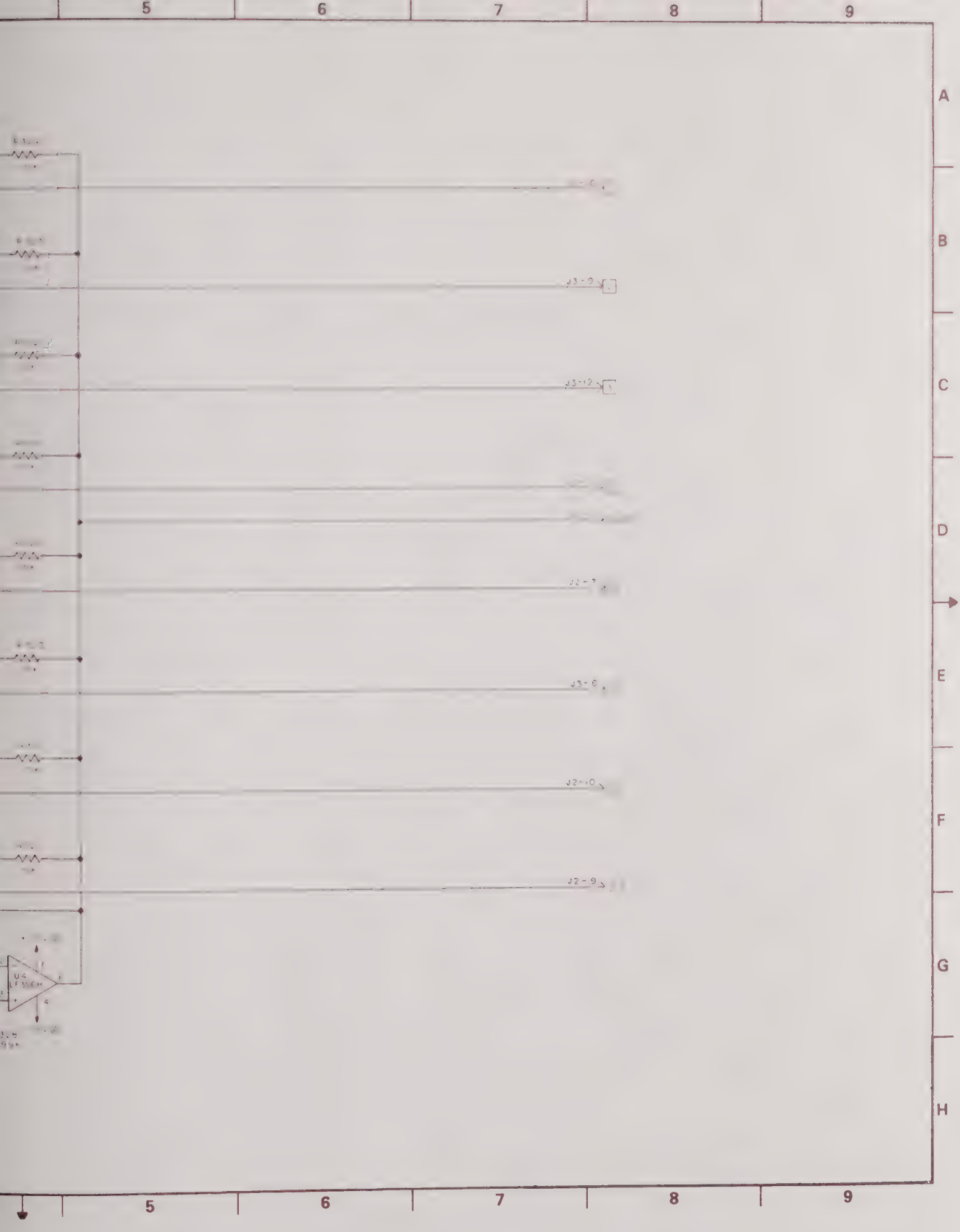


Figure 7-52. Log Amplifier (A3) PCB Input Module Voltage Translator Circuit Schematic Diagram


5
6
7
8
9
A
B
C
D
E
F
G
H
J3-9
J3-12
J3-7
J3-6
J2-10
J2-9

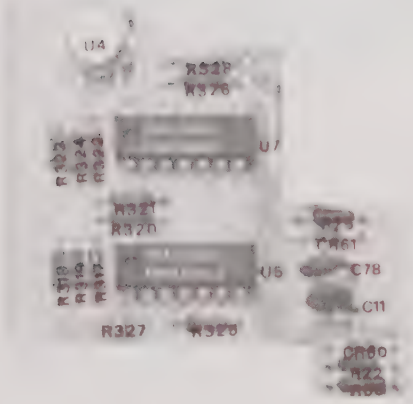


Figure 7-53. Log Amplifier (A3) PCB Input Module Voltage Translator Circuit Parts Locator Diagram

Figure 7-52.

7-6.15 Input Module Voltage Translator Circuit

This circuit translates between CMOS and J-FET voltage levels. The voltage levels of the output pulses from the Channel A&B Demultiplexer and Switch-Reference circuits are CMOS (0 to +5 volts); the pulse voltage levels required by the Input Module multiplexer circuits are J-FET (-15 to 0 volts). The schematic for this circuit is shown in Figure 7-52, the parts locator diagram is shown in Figure 7-53, and a diagram showing the voltage levels of the circuit's input and output pulses is shown in Figure 7-54.

The inputs to this circuit (Figure 7-52) are the ① , ② , ③ , ④ , ⑤ , and ⑥ pulse signals from the Channel A&B Demultiplexer and Switch-Reference Logic circuits. The circuit outputs are the [1] , [2] , [3] , [3'] , [4] , [5] , [6] , and [6'] pulse signals. These signals go to the A10 Input Module Assembly.

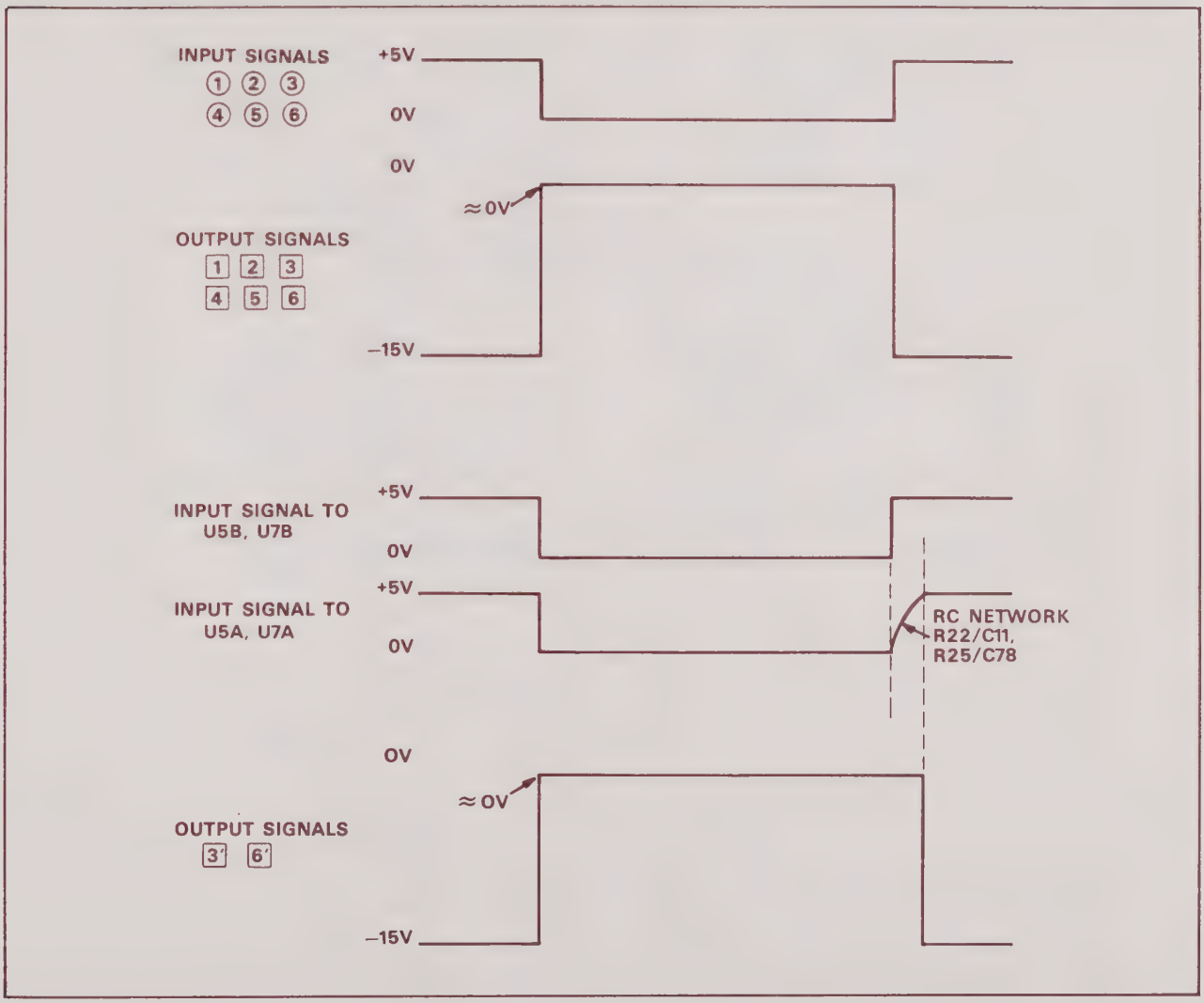


Figure 7-54. Input Module Voltage Translator Circuit, Input and Output Signal Levels

7-7 FRONT PANEL (A1) AND DIGITAL (A2) PRINTED CIRCUIT BOARDS

These two circuit boards are the heart of the network analyzer. They function together to (1) interface front panel switches and indicators with the circuits they control, (2) provide digital storage and display-refresh memory processing for measured signals, and (3) supply analog drive signals to the CRT blanking and deflection circuits. The A1 and A2 PCBs together contain 23 major circuits, diagrammed on 12 sheets of schematics - 2 sheets for the A1 PCB and 10 sheets for the A2 PCB. To provide continuity between schematics, a system of descriptive mnemonic symbols identify the control and signal lines used. Table 7-2 provides an alphabetical listing of these mnemonic symbols, including a "Definition," "To," and "From" column for each one.

To interconnect the A2 PCB with both the rear panel connectors and with the A1, A3, A4, A6, and A8 PCBs, 11 connectors are used. Figure 7-55 provides a photograph of the A2 PCB that shows where these 11 connectors are physically located; this figure also provides a pinout diagram for each connector. This pinout diagram identifies each pin with the mnemonic symbol of the control or signal line to which it is attached; the diagram also shows the figure number of the schematic from which the control or signal line comes.

To provide maintenance instructions, technical information for the A1/A2 PCBs is organized into blocks of data. Each schematic is presented on a foldout page. Along with the schematic is a parts locator diagram showing the physical location of applicable components, and, where appropriate, photographs showing waveforms at schematic test points. A description for each circuit shown on the schematic is contained on the adjacent, facing page(s).

To begin the circuit descriptions, a broad, overall block diagram is presented in Figure 7-56. This diagram shows the general organization of major circuits on the A2 PCB, indicates the paragraph number(s) where the circuit is described, and shows the functional relationship between the A1, A2, A3, A6, and A8 PCBs.

To conclude the circuit descriptions, a detailed overall block diagram of the A1/A2 major circuits is provided in Figure 7-95. This diagram puts all of the major circuits close together on a single page and presents them with enough detail to permit the diagram to be used to aid in preliminary troubleshooting.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits

MNEMONIC	DEFINITION	FROM*	TO*
BLANK INPUT	Blanking Input Signal	Fig. 7-124/8D	Fig. 7-81/0A via A2P8-5
BLANK OUT	Blanking Output Signal	Fig. 7-88/9E	Fig. 7-124/0F
COMP BLANK INPUT	Composite Blanking Input Signal	Z AXIS SELECT switch, Fig. 7-126/3E	Fig. 7-81/0F via A2P5-1
CRT BLANK	Blanking Output Signal	Fig. 7-88/9E	A2P4-4
CRT HOR	Horizontal Output Ramp Signal	Fig. 7-80/9E	A2P4-6
CRT VERT	Vertical Output Signal	Fig. 7-80/9F	A2P4-5
DOA	Display Out A	Fig. 7-59, Sh. 1/9D	Fig. 7-80/0F via A2P2-23
DOB	Display Out B	Fig. 7-59, Sh. 1/9E	Fig. 7-80/0G via A2P2-10
-EXT VERT	Negative Polarity Vertical Output Signal	Fig. 7-80/9G	A6 PCB via A2J1-1
H	Horizontal Signal	Fig. 7-59, Sh. 1/9F	Fig. 7-80/0E via A2P1-6
-HI	Negative Polarity Horizontal Sweep Ramp Signal	Fig. 7-80/9E via A2P1-4	Fig. 7-59, Sh. 1/0H
HAMKR	High active-state, Digitized Analog Marker Signal	Fig. 7-80/9C	Fig. 7-81/0F
HAON	High active-state, Channel A ON Signal	Fig. 7-59, Sh. 1/9A	Fig. 7-59, Sh. 2/0B
HCA	High active-state, Channel A Sweep-on	Fig. 7-88/9D	Fig. 7-80/0H

* The numeric/alpha characters (e.g., 0F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
HCG	High Current Ground	A2P6-5, 6	Fig. 7-68/0E
HCH	High active-state, Counter Hold Signal	Fig. 7-89/9F	Fig. 7-88/0D
HDL PLOT	High active-state, Dual Channel Refresh X-Y Plot in Progress Signal	Fig. 7-89/9C	Fig. 7-73/0E & Fig. 7-88/0B
HDV	High active-state, Data Valid Signal	Fig. 7-81/9F	Fig. 7-88/0C
HERWB	High active-state, Enable Refresh Memory Write Bus Signal	Fig. 7-88/9B	Fig. 7-72/0C
HEWB	High active-state, Enable Storage Memory Write Bus Signal	Fig. 7-63/9B	Fig. 7-88/0C
HFO	High active-state, Filter Off Signal	Fig. 7-81/9B	Fig. 7-59, Sh. 1/0H via A2P1-6
HHOLD	High active-state, Hold Signal	Fig. 7-63/9F	Fig. 7-62/0C
HINDC	High active-state, Internal Dot Connector Signal	Fig. 7-72/9G	Fig. 7-89/0B
HINTA	High active-state, Internal A Signal	Fig 7-81/9F	Fig. 7-62/0B & Fig. 7-67/0D & Fig. 7-88/0D & Fig. 7-89/0H
HLDBA	High active-state, Load dB A Signal	Fig. 7-88/9C	Fig. 7-68/0D
HLDBB	High active-state, Load dB B Signal	Fig. 7-88/9G	Fig. 7-68/0F
HLML	High active-state, Load Storage Memory Latch Signal	Fig. 7-63/9B	Fig. 7-67/0C & Fig. 7-73/0A
HLRL	High active-state, Load Refresh Memory Latch Signal	Fig. 7-72/9A	Fig. 7-72/0A
HLSB	High active-state, Least Significant Bit Signal	Fig. 7-63/9D	Fig. 7-67/0E & Fig. 7-72/0F
HMCA	High active-state, Memory Enable A Signal	Fig. 7-59, Sh. 1/9C	Fig. 7-68/0G via A2P2-24
HMEB	High active-state, Memory Enable B Signal	Fig. 7-59, Sh. 1/9D	Fig. 7-68/0G via A2P2-26

* The numeric/alpha characters (e.g., 0F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
HMKR	High active-state, Marker Output Signal	Fig. 7-81/9D	Fig. 7-73/0D
HMSB	High active-state, Most Significant Bit Signal	Fig. 7-63/9E	Fig. 7-67/0G & Fig. 7-72/0H
HOCLK	High active-state, Output Counter Clock Signal	Fig. 7-88/9B	Fig. 7-72/0B
HOCEN	High active-state, Output Counter Enable Signal	Fig. 7-89/9E	Fig. 7-72/0B
HOCØ thru HOC6	High active-state, Count Signals	Fig. 7-72/9C	Fig. 7-89/0A
HPLOT	High active-state, Refresh X-Y Plot In Progress Signal	Fig. 7-89/9D	Fig. 7-73/0D & Fig. 7-80/0D & Fig. 7-88/0A
HPLOT ON	High active-state, X-Y Plot LED Control Signal	Fig. 7-88/9E	Fig. 7-89/0C
HRCD	High active-state, Real Time X-Y Plot In Progress Signal	Fig. 7-89/9G	Fig. 7-88/0E
HRPD	High active-state, Refresh Plot Pen Down Signal	Fig. 7-89/9F	Fig. 7-88/0D
HRTPD	High active-state, Real Time Plot Pen Down Signal	Fig. 7-89/9G	Fig. 7-88/0C
HRTR	High active-state, Retrace Blanking Signal	Fig. 7-81/9A	Fig. 7-63/0A & Fig. 7-88/0G & Fig. 7-89/0H
HSFS	High active-state, Single Frequency Sweep Control Signal	Fig. 7-89/9C	Fig. 7-80/0A
HWM	High active-state, Write Memory Signal	Fig. 7-88/9G	Fig. 7-63/0A
H1MHZ	High active-state, 1 MHz Clock Signal	Fig. 7-88/9A	Fig. 7-63/0D

* The numeric/alpha characters (e.g., 0F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
HO	Horizontal Output Ramp Signal	Fig. 7-59, Sh. 2/9A	Fig. 7-59, Sh. 1/0F, Fig. 7-63/0E Fig. 7-124/1D
HORIZON-TAL IN	Horizontal Input Signal	HORIZONTAL INPUT Connector Fig. 7-126/9D	Fig. 7-80/0F via A2P5-2
HOR OUT	Horizontal Output Signal	Fig. 7-80/9F	HORIZ OUT Connector
-(IN+OS)A	Negative Polarity INA + OSA Analog Voltage Signal	Fig. 7-80/9A via A2P2-25	Fig. 7-59, Sh. 1/0A
-(IN+OS)B	Negative Polarity INB + OSB Analog Voltage Signal	Fig. 7-80/9B via A2P3-4	Fig. 7-59, Sh. 1/0E
INA	Input A Analog Voltage Signal	Fig. 7-59, Sh. 1/8A	Fig. 7-80/0B via A2P3-23
INB	Input B Analog Voltage Signal	Fig. 7-60, Sh. 1/9D	Fig. 7-80/0C via A2P3-13
LOG A, B	Input Channel A or B Signal	A3 PCB via A2J2-16	Fig. 7-62/0G & Fig. 7-59, Sh. 1/0A via A2P3-24
LOG A,B-R	Input Channel A,B-R Signal	A3 PCB via A2J2-15	Fig. 7-62/0G & Fig. 7-59/0B via A2P3-25
LOG R	Input Channel R Signal	A3 PCB via A2J2-14	Fig. 7-62/0G & Fig. 7-59/0B via A2P3-26
LA	Low-active state, Input Channel A Only Signal	Fig. 7-124/8F	Fig. 7-88/0 via A2P8-11
LA, B	Low active-state, Channel A and Channel B ON Signal	Fig. 7-72/9A	Fig. 7-81/0F & Fig. 7-88/0C & Fig. 7-89/0E
LA/HB	Low active-state, Channel A ON/ Channel B Off Signal	Fig. 7-59, Sh. 1/8A	Fig. 7-72/0C via A2P3-18

* The numeric/alpha characters (e.g., 0F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
LAZ	Low active-state, Autozero Output Signal	Fig. 7-81/9B	A3 PCB via A2J2-9
LB/HA	Low active-state, Channel B ON/ Channel A Off Signal	Fig. 7-59, Sh. 1/9D	Fig. 7-72/0D via A2P3-7
LCA	Low active-state, Channel B Sweep-On Signal	Fig. 7-88/9D	Fig. 7-80/0G
LCG	Low Current Ground	A2P6-11	Fig. 7-62/0D
LCRT/HRCD	Low active-state when OUTPUT MODE switch is in CRT position--High active-state when switch is in RCDR position	A8 PCB via A2P8-7	Fig. 7-89/0F
LDC	Low active-state, Dot Connector Signal	Fig. 7-72/9A	Fig. 7-73/0H
LDETA	Low active-state, Detector A Signal	Fig. 7-88/9G	A3 PCB via A2J2-11
LDL PLOT	Low active-state, Dual Channel Refresh X-Y Plot In Progress Signal	Fig. 7-89/9E	Fig. 7-88/0B
LDRTR	Low active-state, Delayed Retrace Blanking Signal	Fig. 7-81/9G	Fig. 7-89/0F
LDV	Low active-state, Data Valid Signal	Fig. 7-81/9E	Fig. 7-62/0C Fig. 7-125/ via A2P8-10
LERWB	Low active-state, Enable Refresh Memory Write Bus	Fig. 7-81/9B	Fig. 7-72/0C
LEWB	Low active-state, Enable Storage Memory Write Bus	Fig. 7-63/9B	Fig. 7-72/0C
LEXT AZ	Low active-state, External Autozero Signal	A6 PCB via A2J1-9	Fig. 7-81/0E
LEXT DETA	Low active-state, External Detector A Signal	A6 PCB via A2J1-11	Fig. 7-81/0H
LEXT FILT1	Low active-state, External Filter 1 Signal	A6 PCB via A2J1-13	Fig. 7-81/0E

* The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
LEXT FILT2	Low active-state, External Filter 2 Signal	A6 PCB via A2J1-12	Fig. 7-81/0E
LEXT PLT	Low active-state, External Plot Signal	A6 PCB via A2J1-5	Fig. 7-89/0G
LEXT SWR	Low active-state, External Switch Reference Signal	A6 PCB via A2J1-10	Fig. 7-81/0E
LFLSHA	Low active-state, Flasher A Signal	Fig. 7-62/9C via A2P2-16	Fig. 7-59, Sh. 1/0C
LFLSHB	Low active-state, Flasher B Signal	Fig. 7-62/9C via A2P2-15	Fig. 7-59, Sh. 1/0G
LFILT1	Low active-state, Filter (smoothing) 1 Signal	Fig. 7-81/9B	A3 PCB via A2J2-13
LFILT2	Low active-state, Filter (smoothing) 2 Signal	Fig. 7-81/9C	A3 PCB via A2J2-12
LFMX	Low active-state, Filter Maximum LED Control Signal	Fig. 7-81/9B via A2P1-3	Fig. 7-59, Sh. 1/0H
LINC	Low active-state, Increment Smoothing Sequencer Control Signal	Fig. 7-59, Sh. 1/9G	Fig. 7-81/0E via A2P1-13
LINTA	Low active-state, Internal A Signal	Fig. 7-87/9F	Fig. 7-62/0B & Fig. 7-67/0E & Fig. 7-88/0D & Fig. 7-89/0D
LMWE	Low active-state, Storage Memory Write Enable Signal	Fig. 7-63/9A	Fig. 7-67/0D

* The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
LNORM/ HEXT	Low active-state when rear panel LOW LEVEL CAL switch is in NORM position--High active-state when LOW LEVEL CAL switch is in EXT position.	LOW LEVEL CAL Switch via A2J3-6	Fig. 7-81/0C
LOUT CONT	Low active-state, Vertical and Horizontal Output Control Signal	Fig. 7-89/9F	Fig. 7-80/0H
LPON	Low active-state, Power-On Reset Signal	Fig. 7-89/9F	Fig. 7-81/0D & Fig. 7-88/0E
LPLOT	Low active-state, Refresh X-Y Plot In Progress Signal	Fig. 7-89/9C	Fig. 7-73/0E & Fig. 7-80/0D & Fig. 7-88/0A
LPLOT LED	Low active-state, X-Y Plot LED Control Signal	Fig. 7-89/9D via A2P1-5	Fig. 7-59, Sh. 1/0H
LRH	Low active-state, REFRESH HOLD Signal	Fig. 7-59, Sh. 1/9E	Fig. 7-88/9B via A2P1-8
LRLTM	Low active-state, REAL TIME Signal	Fig. 7-59, Sh. 1/9F	Fig. 7-73/0A via A2P1-11 & Fig. 7-88/0B & Fig. 7-89/0G
LRSS	Low active-state, Reduce Sweep Speed LED Control Signal	Fig. 7-81/9G via A2P1-2	Fig. 7-59, Sh. 1/0H
LRST	Low active-state, Refresh Horizontal Sweep Ramp Reset Signal	Fig. 7-89/9D	Fig. 7-80/0C & Fig. 7-88/0A
LRTR	Low active-state, Retrace Blanking Signal	Fig. 7-88/9F	Fig. 7-89/0H
LRWE	Low active-state, Refresh Memory Write Enable Signal	Fig. 7-88/9C	Fig. 7-73/0E
LSTA	Low active-state, Store Trace A Signal	Fig. 7-59, Sh. 1/8A	Fig. 7-88/0D via A2P3-19
LSTB	Low active-state, Store Trace B Signal	Fig. 7-59, Sh. 1/9D	Fig. 7-88/0F via A2P3-5

* The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
LSWR	Low active-state, Switch Reference Signal	Fig. 7-81/9B	A3 PCB via A2J2-10
LXY PLOT	Low active-state, XY PLOT Control Signal	Fig. 7-59, Sh. 1/9F	Fig. 7-89/0G via A2P1-9
L.5A thru L10A	Low active-state, Vertical Sensitivity A Control Signals	Fig. 7-59, Sh. 1/8A	Fig. 7-68/0C
L.5B thru L10B	Low active-state, Vertical Sensitivity B Control Signals	Fig. 7-59, Sh. 1/9D	Fig. 7-68/0E
L1MHz	Low active-state, 1 MHz Clock Signal	Fig. 7-88/9A	Fig. 7-72/0C
—M	Negative Polarity Marker Signal	Fig. 7-73/9A via A2P3-11	Fig. 7-59, Sh. 1/0G
—MA	Negative Polarity Memory A Signal	Fig. 7-68/9B via A2P3-17	Fig. 7-59, Sh. 1/0C
—MB	Negative Polarity Memory B Signal	Fig. 7-68/9E via A2P2-13	Fig. 7-59, Sh. 1/0F
MARKER IN	Marker Input Signal	MARKER INPUT Connector	Fig. 7-80/0A
MEM OUT	Memory Output Signal	Fig. 7-67/9C	Fig. 7-68/0A
MI	Marker Input Signal	Fig. 7-80/0C via A2P3-12	Fig. 7-59, Sh. 1/0G
—MO	Negative Polarity Marker Output Signal	Fig. 7-59, Sh. 1/9G	Fig. 7-80/0D via A2P3-9
NH	Normalized Horizontal Ramp Signal	Fig. 7-59, Sh. 1/9G	Fig. 7-59, Sh. 2/0A
OSA	Offset A Signal	Fig. 7-59, Sh. 1/9C	Fig. 7-59, Sh. 2/0F & Fig. 7-80/0A via A2P1-15

* The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits (continued)

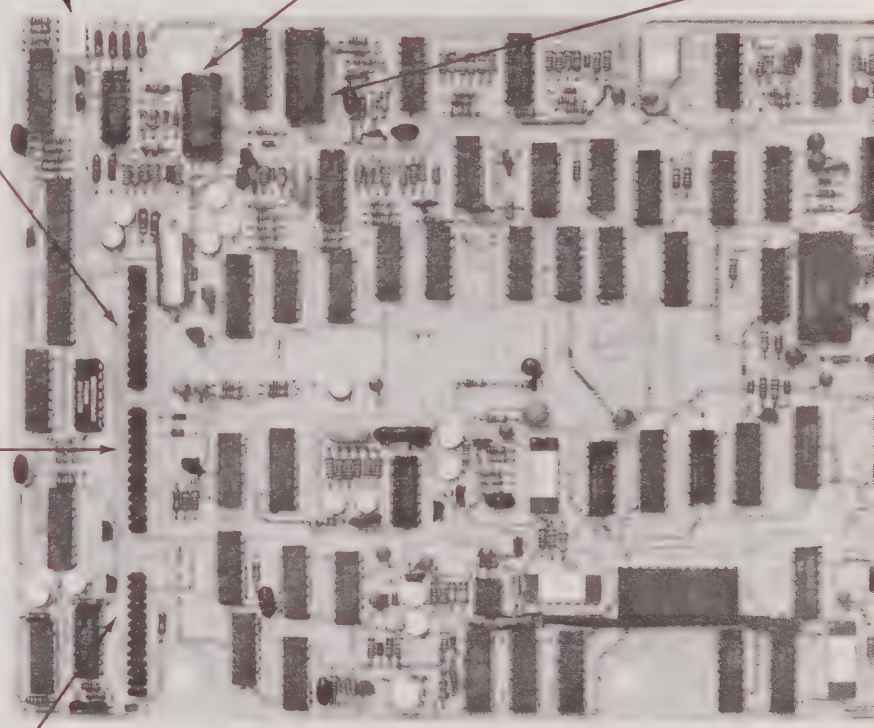
MNEMONIC	DEFINITION	FROM*	TO*
OSB	Offset B Signal	Fig. 7-59, Sh. 1/9E	Fig. 7-59 Sh. 2 0F & Fig. 7-80/0C via A2P1-14
RFH	Refresh Horizontal Analog Signal	Fig. 7-80/9B via A2P1-12	Fig. 7-59, Sh. 1/0G
−RFV	Negative Polarity Refresh Vertical Analog Signal	Fig. 7-73/9G via A2P2-14	Fig. 7-59, Sh. 1/0G
RSA	Reset A Signal	Fig. 7-59, Sh. 1/9C	Fig. 7-80/0B via A2P2-18
RSB	Reference B Signal	Fig. 7-59, Sh. 1/9F	Fig. 7-80/0C via A2P2-9
RTV	Real Time Vertical Signal	Fig. 7-62/9B via A2P2-1	Fig. 7-59, Sh. 1/0G
SOA	SET Output A	Fig. 7-59, Sh. 1/9D	Fig. 7-80/0F via A2P2-21
SOB	SET Output B	Fig. 7-59, Sh. 1/9F	Fig. 7-80/0G via A2P1-24
SYNC	Synchronize Alternate-Sweep Signal	Fig. 7-124/8F	Fig. 7-81/0F via A2P8-9
−T	Minus Marker Signal	Fig. 7-59, Sh. 1/9H	Fig. 7-80/0E via A2P2-3
+T	Plus Marker Signal	Fig. 7-59, Sh. 1/9H	Fig. 7-80/0E via A2P2-5
− TO	Negative Polarity TILT Output Signal	Fig. 7-59, Sh. 1/9G	Fig. 7-80/0F via A2P2-4
TEST IN	Horizontal Ramp Voltage Used As Test Input Signal For A3 PCB (Used for factory adjustment of A2 PCB Log Conformity)	Fig. 7-80/9E	A3 PCB via A2J2-1 and Fig. 7-81
VERT OUT	Vertical Signal	Fig. 7-80/9F	VERTICAL OUTPUT Connector, Fig. 7-126/1A via A2J3-3

* The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.

Table 7-2. Listing of Mnemonic Symbols used with A1 and A2 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
VO	Vertical Input Signal To AD Converter	Fig. 7-62/9B	Fig. 7-63/0G
VOA	Vertical Output A Signal From dB Per Division Gain Circuit	Fig. 7-59, Sh. 1/8B	Fig. 7-62/0B via A2P1-21
VOB	Vertical Output B Signal From DB Per Division Gain Circuit	Fig. 7-59, Sh. 1/9D	Fig. 7-62/0C via A2P2-6

* The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number indicate the schematic grid coordinates.



P5 TO BACK PANEL (SHIELDED)

1	O	LCG (FIG 7-62, 9D)
2	O	HORIZONTAL IN (FIG 7-80, 0F)
3	O	LCG (FIG 7-62, 9D)
4	O	MARKER IN (FIG 7-80, 0A)

J2 TO LOG AMP. PCB

(FIG 7-80, 9E) TEST IN	O 1		16 O	LOG A, B (FIG 7-62, 0G)
(FIG 7-62, 9E) HCG	O 2		15 O	LOG A,B R (FIG. 7-62, 0G)
(FIG. 7-62, 9E) +5V	O 3		14 O	LOG R (FIG 7-62, 0G)
(FIG. 7-62, 9F) +22V	O 4		13 O	LFILT 1 (FIG 7-81, 9C)
(FIG 7-62, 9C) +15V	O 5		12 O	LFILT 2 (FIG 7-81, 9C)
(FIG 7-62, 9E) 15V	O 6		11 O	LDETA (FIG 7-88, 9G)
(FIG 7-62, 9F) 22V	O 7		10 O	LSWR (FIG. 7-81, 9C)
(FIG 7-62, 9D) LCG	O 8		9 O	LAZ (FIG 7-81, 9C)

J1 TO

				(FIG 7-80, 9G) LEXT VERT
				(FIG 7-62, 9D) HCG
				(FIG 7-62, 9F) +5V
				(FIG 7-81, 0F) LRMT
				(FIG 7-89, 0G) LEXT PLT
				(FIG 7-62, 9C) +18V
				(FIG 7-62, 9E) 18V
				(FIG. 7-62, 9D) LCG
				(FIG 7-81, 0E) LEXT AZ

P1 TO FRONT PANEL PCB

(FIG 7-81, 9C) LRMT	1 O		O 14	OSB (FIG 7-80, 0C)
(FIG 7-81, 9G) LRSS	2 O		O 15	OSA (FIG 7-80, 0B)
(FIG 7-81, 9B) LFMX	3 O		O 16	OPEN
(FIG 7-80, 9E) HI	4 O		O 17	LCG (FIG 7-62, 9D)
(FIG 7-89, 9D) LPLOT LED	5 O		O 18	OPEN
(FIG 7-81, 9B) HFO	6 O		O 19	L 5A (FIG 7-68, 0C)
(FIG 7-68, 0E) L 5B	7 O		20	L1A (FIG 7-68, 0C)
(FIG 7-88, 0B) LRH	8 O		21	VOA (FIG 7-62, 0B)
(FIG 7-89, 0G) LXY PLOT	9 O		O 22	L2A (FIG 7-68, 0C)
(FIG 7-68, 0E) L1B	10 O		23	L5A (FIG 7-68, 0C)
(FIG 7-73, 0A) LRLTM	11 O		24	SOB (FIG 7-80, 0G)
(FIG 7-80, 9B) RFH	12 O		25	L2B (FIG 7-68, 0E)
(FIG 7-81, 0E) LINC	13 O		26	H (FIG 7-80, 0E)

P2 TO FRONT PANEL PCB

(FIG 7-62, 9B) RTV	1 O		O 14	RFV (FIG 7-73, 9G)
(FIG 7-68, 0E) L5B	2 O		O 15	LFLSHB (FIG 7-62, 9C)
(FIG 7-80, 0E) T	3 O		O 16	LFLSHA (FIG 7-62, 9C)
(FIG 7-80, 0F) TO	4 O		17	OPEN
(FIG 7-80, 0E) +T	5 O		O 18	RSA (FIG 7-80, 0B)
(FIG 7-62, 0C) VOB	6 O		O 19	L10A (FIG 7-68, 0C)
(FIG 7-68, 0E) L10B	7 O		20	+15V (FIG 7-62, 9C)
OPEN	8 O		O 21	SOA (FIG 7-80, 0F)
(FIG 7-80, 0C) RSB	9 O		O 22	15V (FIG 7-62, 9E)
(FIG 7-80, 0G) DOB	10 O		O 23	DOA (FIG 7-80, 0F)
OPEN	11 O		24	LMEA (FIG 7-68, 0G)
(FIG 7-62, 9E) 10.5 BOOST	12 O		O 25	(IN+OS)A (FIG 7-80, 9A)
(FIG 7-68, 9E) MB	13 O		O 26	LMEB (FIG 7-68, 0G)

P3 TO FRONT PANEL PCB

(FIG 7-62, 9C) +10.5V BOOST	1 O		O 14	HCG (FIG 7-62, 9E)
OPEN	2 O		O 15	HCG (FIG 7-62, 9E)
OPEN	3 O		O 16	HCG (FIG. 7-62, 9E)
(FIG 7-80, 9B) (IN+OS)B	4 O		O 17	MA (FIG. 7-68, 9B)
(FIG 7-88, 0F) LSTB	5 O		O 18	HA/LB (FIG. 7-72, 0C)
(FIG. 7-62, 9F) +5V	6 O		O 19	LSTA (FIG 7-88, 0D)
(FIG 7-72, 0C) LB/HA	7 O		O 20	+5V (FIG. 7-62, 9F)
OPEN	8 O		O 21	+5V (FIG. 7-62, 9F)
(FIG. 7-80, 0D) MO	9 O		O 22	+5V (FIG. 7-62, 9F)
(FIG 7-63, 0E) HO	10 O		O 23	INA (FIG. 7-80, 0B)
(FIG. 7-73, 9A) -M	11 O		O 24	LOG A,B (FIG. 7-62, 9G)
(FIG. 7-80, 9C) MI	12 O		O 25	LOG A,B-R (FIG. 7-62, 9G)
(FIG. 7-80, 0C) INB	13 O		O 26	LOG R (FIG. 7-62, 9G)

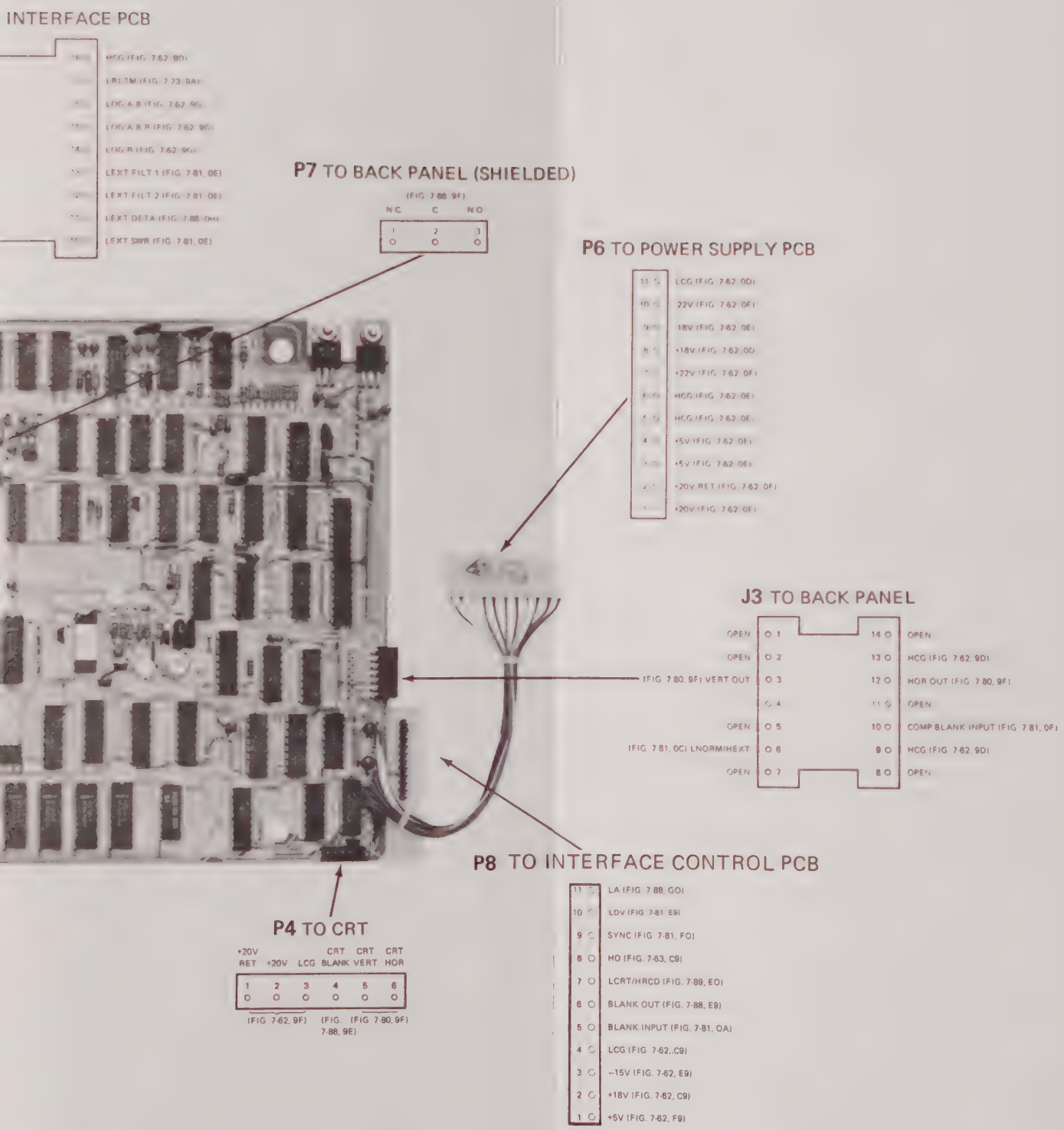
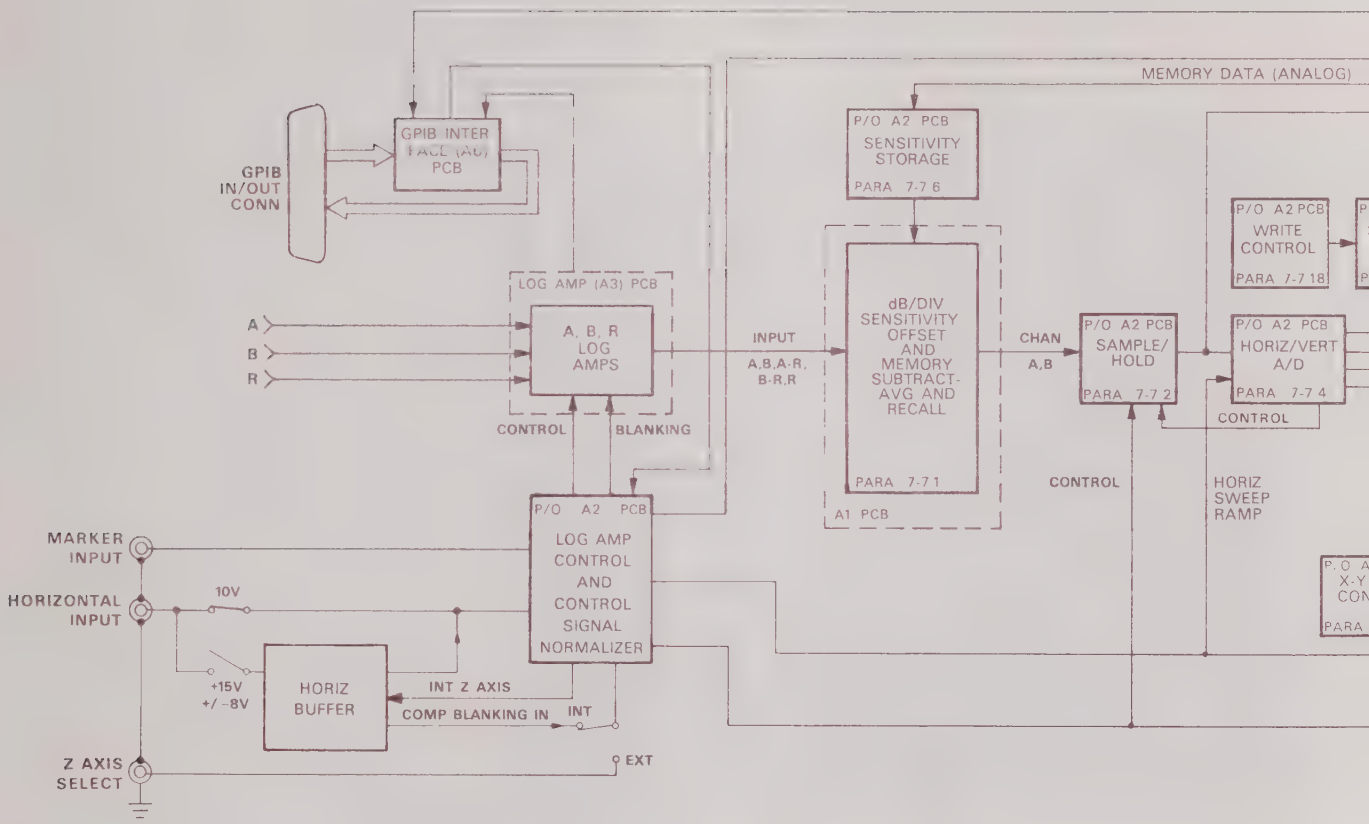

INTERFACE PCB
HCG (FIG. 7-62, 9D)
LRI TM (FIG. 7-73, 9A)
LOG A,B (FIG. 7-62, 9G)
LOG A,B,R (FIG. 7-62, 9G)
LOG R (FIG. 7-62, 9G)
LEXT FILT 1 (FIG. 7-81, 0E)
LEXT FILT 2 (FIG. 7-81, 0E)
LEXT DETA (FIG. 7-88, 0H)
LEXT SWR (FIG. 7-81, 0E)
P7 TO BACK PANEL (SHIELDED)
(FIG. 7-88, 9F)
N.C. C N.O.
1 2 3
P6 TO POWER SUPPLY PCB
LCG (FIG. 7-62, 0D)
22V (FIG. 7-62, 0F)
18V (FIG. 7-62, 0E)
+18V (FIG. 7-62, 0D)
+22V (FIG. 7-62, 0F)
HCG (FIG. 7-62, 0E)
HCG (FIG. 7-62, 0E)
+5V (FIG. 7-62, 0E)
+5V (FIG. 7-62, 0E)
+20V RET (FIG. 7-62, 0F)
+20V (FIG. 7-62, 0F)
J3 TO BACK PANEL
OPEN 1 14 OPEN
OPEN 2 13 HCG (FIG. 7-62, 9D)
(FIG. 7-80, 9F) VERT OUT 3 12 HOR OUT (FIG. 7-80, 9F)
4 11 OPEN
OPEN 5 10 COMP BLANK INPUT (FIG. 7-81, 0F)
(FIG. 7-81, 0C) LNORM/HEXT 6 9 HCG (FIG. 7-62, 9D)
OPEN 7 8 OPEN
P8 TO INTERFACE CONTROL PCB
LA (FIG. 7-88, G0)
LDV (FIG. 7-81, E9)
SYNC (FIG. 7-81, F0)
HO (FIG. 7-63, C9)
LCRT/HRCD (FIG. 7-89, E0)
BLANK OUT (FIG. 7-88, E9)
BLANK INPUT (FIG. 7-81, 0A)
LCG (FIG. 7-62, C9)
–15V (FIG. 7-62, E9)
+18V (FIG. 7-62, C9)
+5V (FIG. 7-62, F9)
P4 TO CRT
+20V RET
+20V
LCG
CRT BLANK
CRT VERT
CRT HOR
1 2 3 4 5 6
(FIG. 7-62, 9F)
(FIG. 7-88, 9E)
(FIG. 7-80, 9F)

Figure 7-55. Digital (A2) PCB Connector Pinout Diagram


MEMORY DATA (ANALOG)
GPIB IN/OUT CONN
GPIB INTER FACE (A6) PCB
P/O A2 PCB
SENSITIVITY STORAGE
PARA 7-7 6
P/O A2 PCB
WRITE CONTROL
PARA 7-7 18
LOG AMP (A3) PCB
A
B
R
A, B, R LOG AMPS
INPUT
A,B,A-R, B-R,R
dB/DIV SENSITIVITY OFFSET AND MEMORY SUBTRACT-AVG AND RECALL
PARA 7-7 1
A1 PCB
CHAN
A,B
P/O A2 PCB
SAMPLE/ HOLD
PARA 7-7 2
P/O A2 PCB
HORIZ/VERT A/D
PARA 7-7 4
CONTROL
BLANKING
CONTROL
CONTROL
HORIZ SWEEP RAMP
MARKER INPUT
HORIZONTAL INPUT
10V
P/O A2 PCB
LOG AMP CONTROL AND CONTROL SIGNAL NORMALIZER
+15V +/-8V
HORIZ BUFFER
INT Z AXIS
COMP BLANKING IN
INT
EXT
Z AXIS SELECT

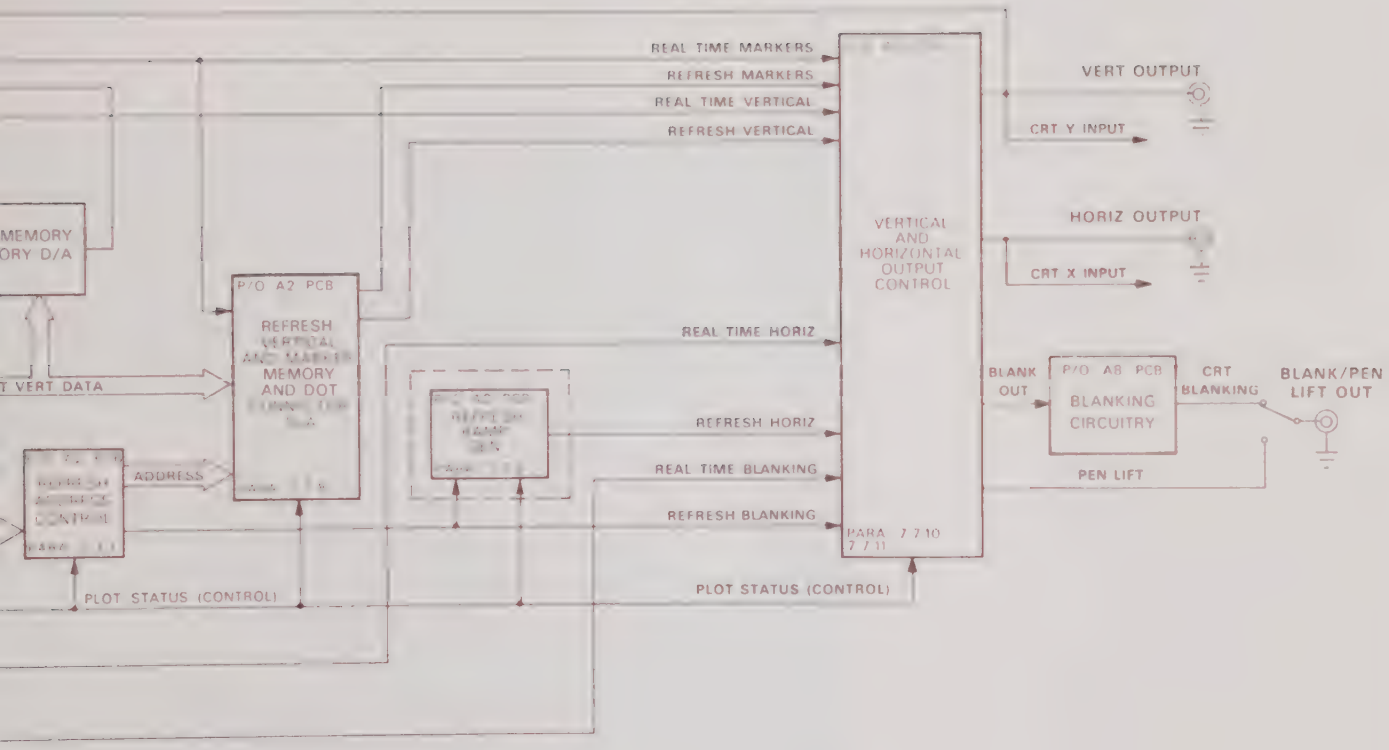


Figure 7-56. Network Analyzer Section Overall Block Diagram

7-7.1 Front Panel (A1) PCB Circuits

The Front Panel (A1) PCB is the connecting plane for the front panel switches, controls, and indicators. In addition, it also contains the following circuits: (1) input summing, (2) offset dB display, (3) memory subtract, average, and recall, (4) dB per division gain and vertical signal output, (5) horizontal input-signal normalizing and 0-10V clamp, and (6) 10.5 volt reference voltage. A block diagram of these circuits is shown in Figure 7-57, a parts locator diagram is shown in Figure 7-58, and the schematic is shown in Figure 7-59. With the exception of the horizontal normalizing and the 10.5 volt circuits, the circuits mentioned above are identical for Channels A and B. Channel A circuits are described below; descriptions are referenced to the block diagram. To correlate between the blocks shown on the block diagram and the actual circuits shown on the schematic diagram, use the mnemonic symbols. The mnemonic symbols used to identify control and signal lines point to the circuit components on the schematic diagram.

a. Input Summing Circuit. This circuit sums the input vertical signal (INA) with voltages from the OFFSET dB display circuit and the REFERENCE dB/dBm switch (signal lines OSA and RSA respectively). The circuit is physically located on the Digital (A2) PCB. The circuit's output, -(IN+OS)A, is applied to the front panel memory switch circuits.

b. Offset dB Display Circuit. This circuit is a precision digital voltmeter whose display is calibrated in dB. Input to the circuit is from the input summing circuit. The vertical input to the input summing circuit, INA, is the output from the Log Amplifier PCB. The voltage level of this signal has been standardized at 125 mV per dB of input signal. When the REFERENCE dB/dBm switch is in the dBm position, and when the OFFSET control is adjusted to obtain zero output from the summing circuit (zero output occurs when the input signal displayed on the CRT crosses the REF POS LOCATE reference line) the OFFSET dB display indicates the absolute (dBm) power level of the input signal.

c. MEMORY Switch (SUBTRACT, AVG, and RECALL) Circuits. These circuits subtract memory from input, average memory with input, or recall memory for display. The MEMORY switch circuits have two inputs: -(IN+OS)A, from the Input Summing circuit, and -MA, from the storage memory via the Sensitivity Storage circuit. The output of the MEMORY switch circuit depends on switch positioning and is described below.

- Depressing the OFF switch causes the Subtract, Average, and Recall circuits to be bypassed and applies the -(IN+OS)A signal directly to the dB Per Division Gain circuit.

- Depressing the SUBTRACT switch causes the -(IN+OS)A signal to be summed with the inverted -MA signal and routes the resultant signal to the dB Per Division Gain circuit. The dB Per Division Gain circuit inverts the signal a second time; this second inversion results in the memory signal being subtracted from the input signal.

- Depressing the AVG switch causes the -(IN+OS)A and the -MA signals to be applied to a resistive network where their respective amplitudes are halved and then summed. The resultant signal is then applied to the dB Per Division Gain circuit.

- Depressing the RECALL switch routes the -MA signal directly to the dB Per Division Gain circuit.

d. dB Per Division Gain Circuit. In addition to gain, this circuit provides a vertical signal whose amplitude has been standardized at 1.25 volts per CRT division and whose positive and negative excursions cannot exceed ± 10 volts. Circuit gain is determined by the dB Per Division switch-bank. The circuit

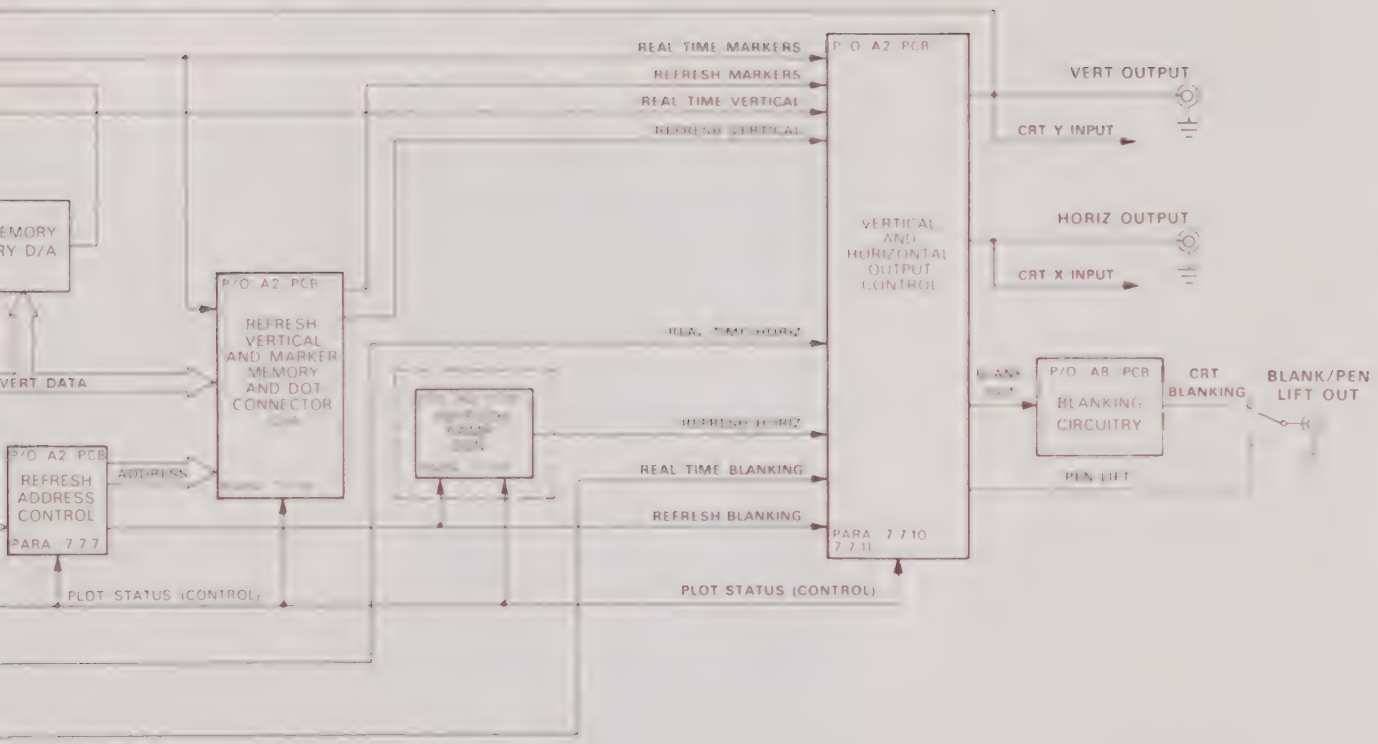


Figure 7-56. Network Analyzer Section Overall Block Diagram

7-7.1 Front Panel (A1) PCB Circuits

The Front Panel (A1) PCB is the connecting plane for the front panel switches, controls, and indicators. In addition, it also contains the following circuits: (1) input summing, (2) offset dB display, (3) memory subtract, average, and recall, (4) dB per division gain and vertical signal output, (5) horizontal input-signal normalizing and 0-10V clamp, and (6) 10.5 volt reference voltage. A block diagram of these circuits is shown in Figure 7-57, a parts locator diagram is shown in Figure 7-58, and the schematic is shown in Figure 7-59. With the exception of the horizontal normalizing and the 10.5 volt circuits, the circuits mentioned above are identical for Channels A and B. Channel A circuits are described below; descriptions are referenced to the block diagram. To correlate between the blocks shown on the block diagram and the actual circuits shown on the schematic diagram, use the mnemonic symbols. The mnemonic symbols used to identify control and signal lines point to the circuit components on the schematic diagram.

a. Input Summing Circuit. This circuit sums the input vertical signal (INA) with voltages from the OFFSET dB display circuit and the REFERENCE dB/dBm switch (signal lines OSA and RSA respectively). The circuit is physically located on the Digital (A2) PCB. The circuit's output, -(IN+OS)A, is applied to the front panel memory switch circuits.

b. Offset dB Display Circuit. This circuit is a precision digital voltmeter whose display is calibrated in dB. Input to the circuit is from the input summing circuit. The vertical input to the input summing circuit, INA, is the output from the Log Amplifier PCB. The voltage level of this signal has been standardized at 125 mV per dB of input signal. When the REFERENCE dB/dBm switch is in the dBm position, and when the OFFSET control is adjusted to obtain zero output from the summing circuit (zero output occurs when the input signal displayed on the CRT crosses the REF POS LOCATE reference line) the OFFSET dB display indicates the absolute (dBm) power level of the input signal.

c. MEMORY Switch (SUBTRACT, AVG, and RECALL) Circuits. These circuits subtract memory from input, average memory with input, or recall memory for display. The MEMORY switch circuits have two inputs: -(IN+OS)A, from the Input Summing circuit, and -MA, from the storage memory via the Sensitivity Storage circuit. The output of the MEMORY switch circuit depends on switch positioning and is described below.

- Depressing the OFF switch causes the Subtract, Average, and Recall circuits to be bypassed and applies the -(IN+OS)A signal directly to the dB Per Division Gain circuit.

- Depressing the SUBTRACT switch causes the -(IN+OS)A signal to be summed with the inverted -MA signal and routes the resultant signal to the dB Per Division Gain circuit. The dB Per Division Gain circuit inverts the signal a second time; this second inversion results in the memory signal being subtracted from the input signal.

- Depressing the AVG switch causes the -(IN+OS)A and the -MA signals to be applied to a resistive network where their respective amplitudes are halved and then summed. The resultant signal is then applied to the dB Per Division Gain circuit.

- Depressing the RECALL switch routes the -MA signal directly to the dB Per Division Gain circuit.

d. dB Per Division Gain Circuit. In addition to gain, this circuit provides a vertical signal whose amplitude has been standardized at 1.25 volts per CRT division and whose positive and negative excursions cannot exceed ± 10 volts. Circuit gain is determined by the dB Per Division switch-bank. The circuit

output signal, VOA, is applied to the A2 PCB vertical signal multiplexing circuit (Figure 7-62).

e. Horizontal Normalizing and 0-10V Clamp Circuit. This circuit normalizes the input horizontal ramp to start at 0 volts and to end at 10 volts. The START control adjusts the ramp to start at 0 volts and the STOP control adjusts the ramp to end at 10 volts. (When adjusting these front panel potentiometers, adjust START first, then adjust STOP; otherwise, START will interact with STOP and affect adjustment at the high end.)

f. 10.5 Volt Reference-Voltage Circuit. This circuit supplies a precision reference voltage for front panel potentiometers. The circuit is composed of operational amplifiers U1B, U1C, and associated components. The input to this circuit comes from the DVM CAL potentiometer, a very stable 1.000-volt source.

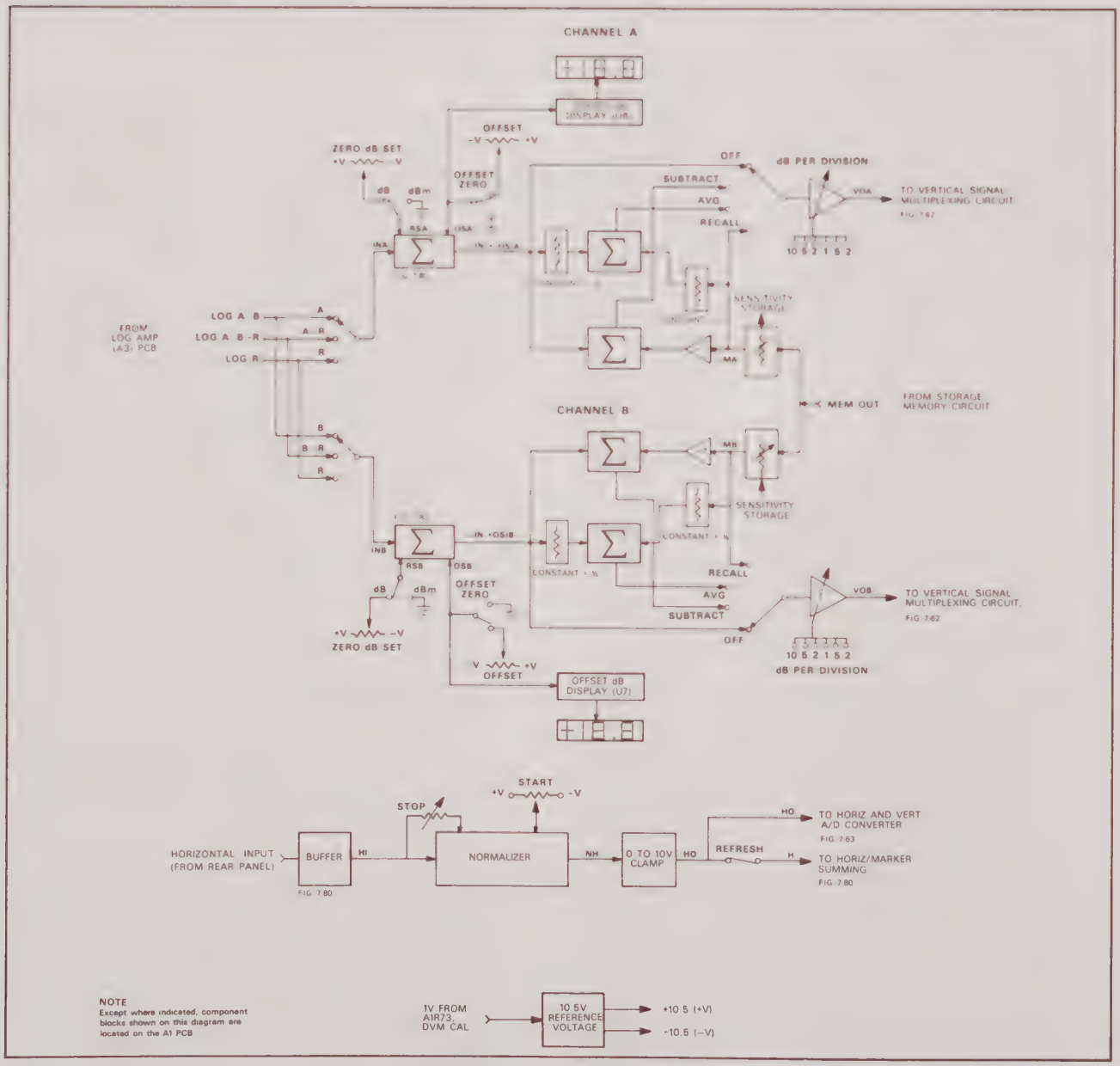


Figure 7-57. A1 PCB Block Diagram

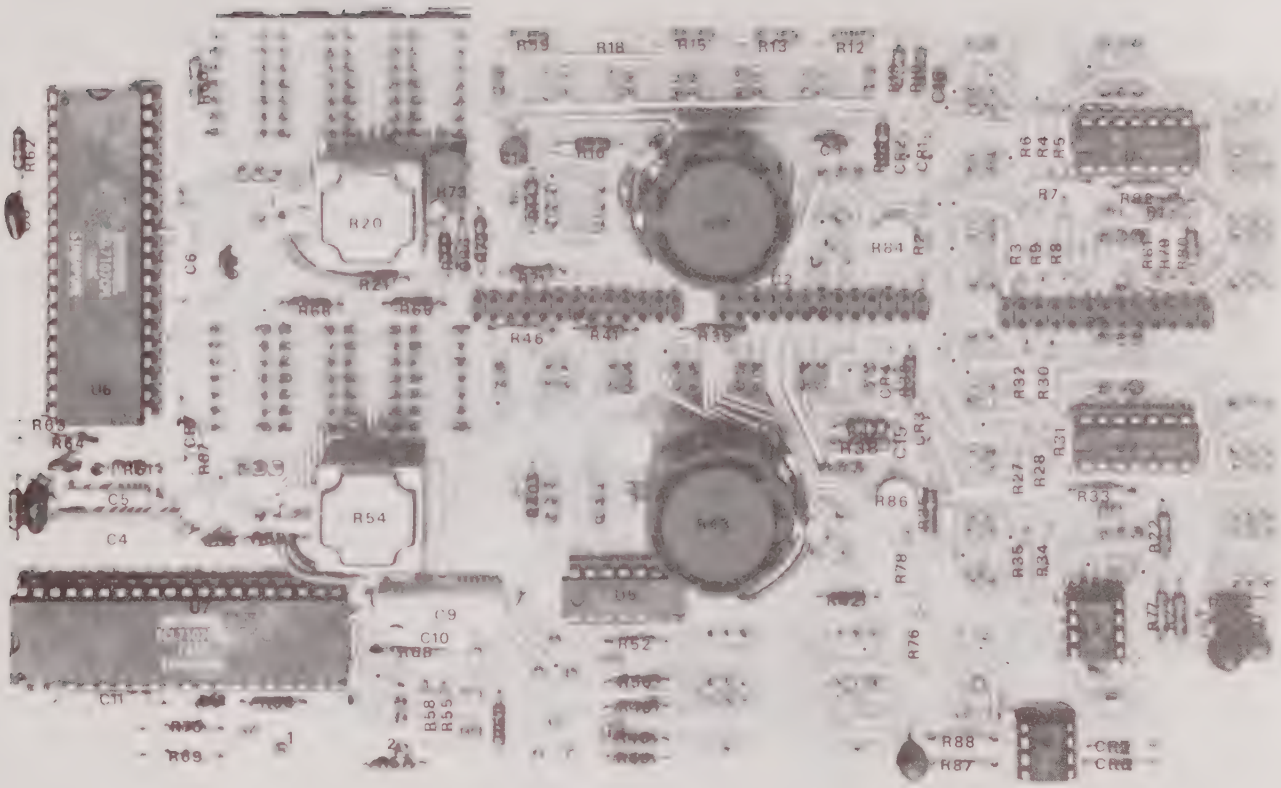
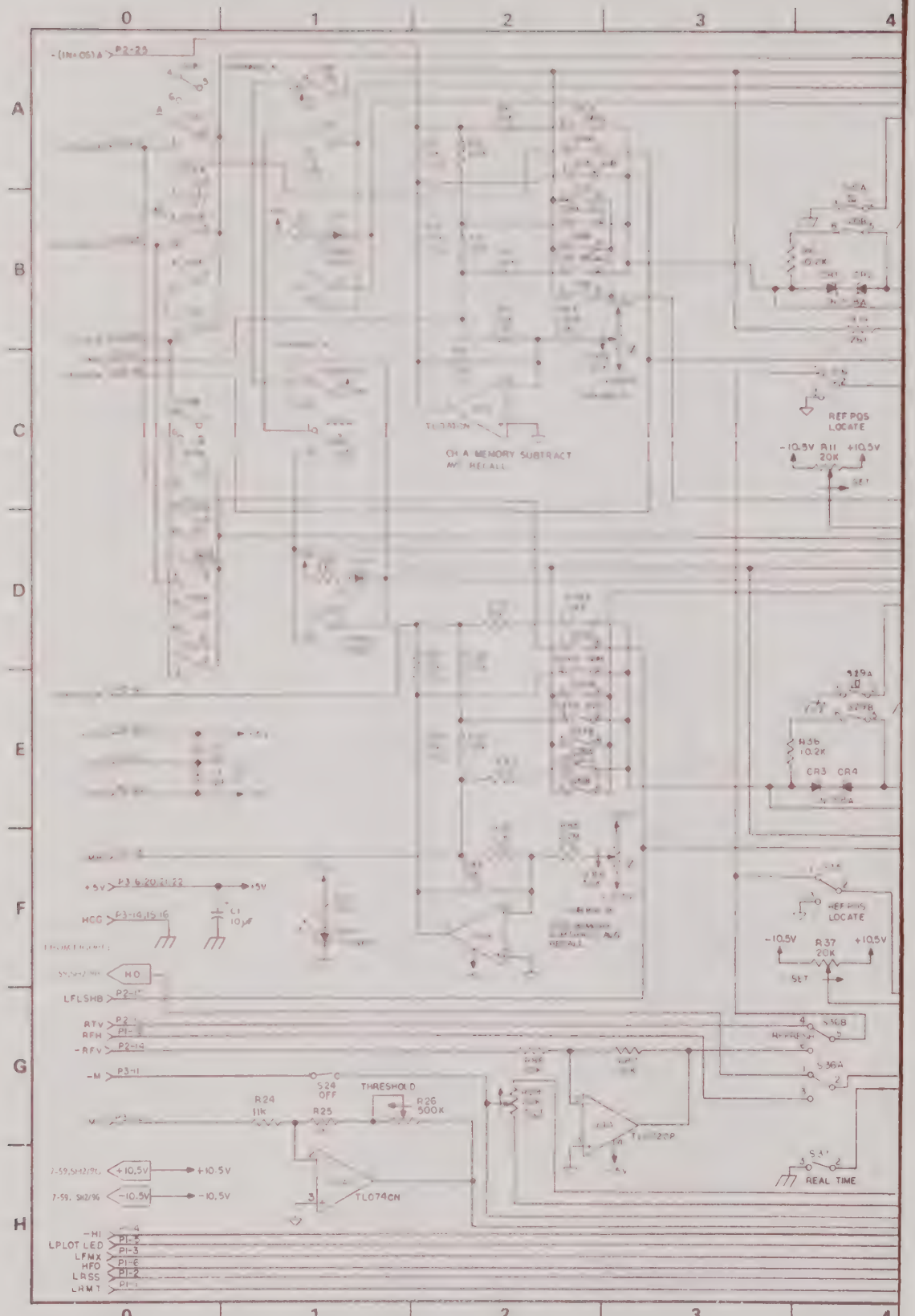


Figure 7-58, Front Panel (A1) PCB Parts Locator Diagram
Sheet 1.


0
1
2
3
4
A
B
C
D
E
F
G
H
CH A MEMORY SUBTRACT
AVG RECALL
REF POS LOCATE
-10.5V R11 +10.5V
20K
SET
R36
10.2K
CR3 CR4
REF POS LOCATE
-10.5V R37 +10.5V
20K
SET
+5V
P3-6-20-21-22
+5V
HCG
P3-14,15-16
C1
10μF
H.O.
LFLSHB
P2-
RTV
RFH
P2-
P1-
-RFV
P2-14
-M
P3-11
S24
OFF
THRESHOLD
R24
11k
R25
R26
500K
S36B
S36A
S37
REAL TIME
+10.5V
+10.5V
-10.5V
-10.5V
TL074CN
-HI
LPLOT LED
LFMX
HFO
LRSS
LRMT
P1-5
P1-3
P1-6
P1-2
P1-
0
1
2
3
4

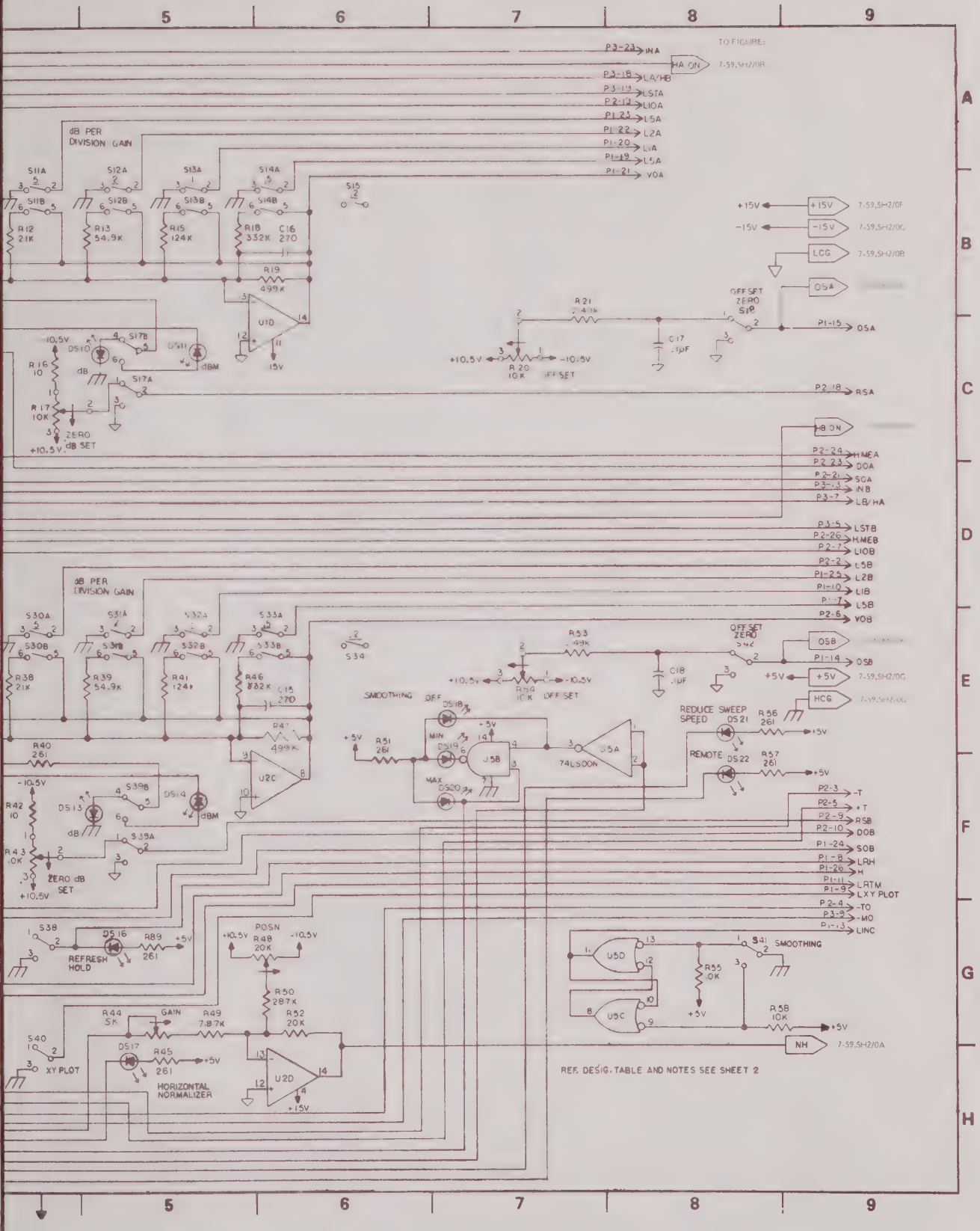


Figure 7-59, Front Panel (A1) PCB Schematic Diagram Sheet 1.

Figure 7-58.

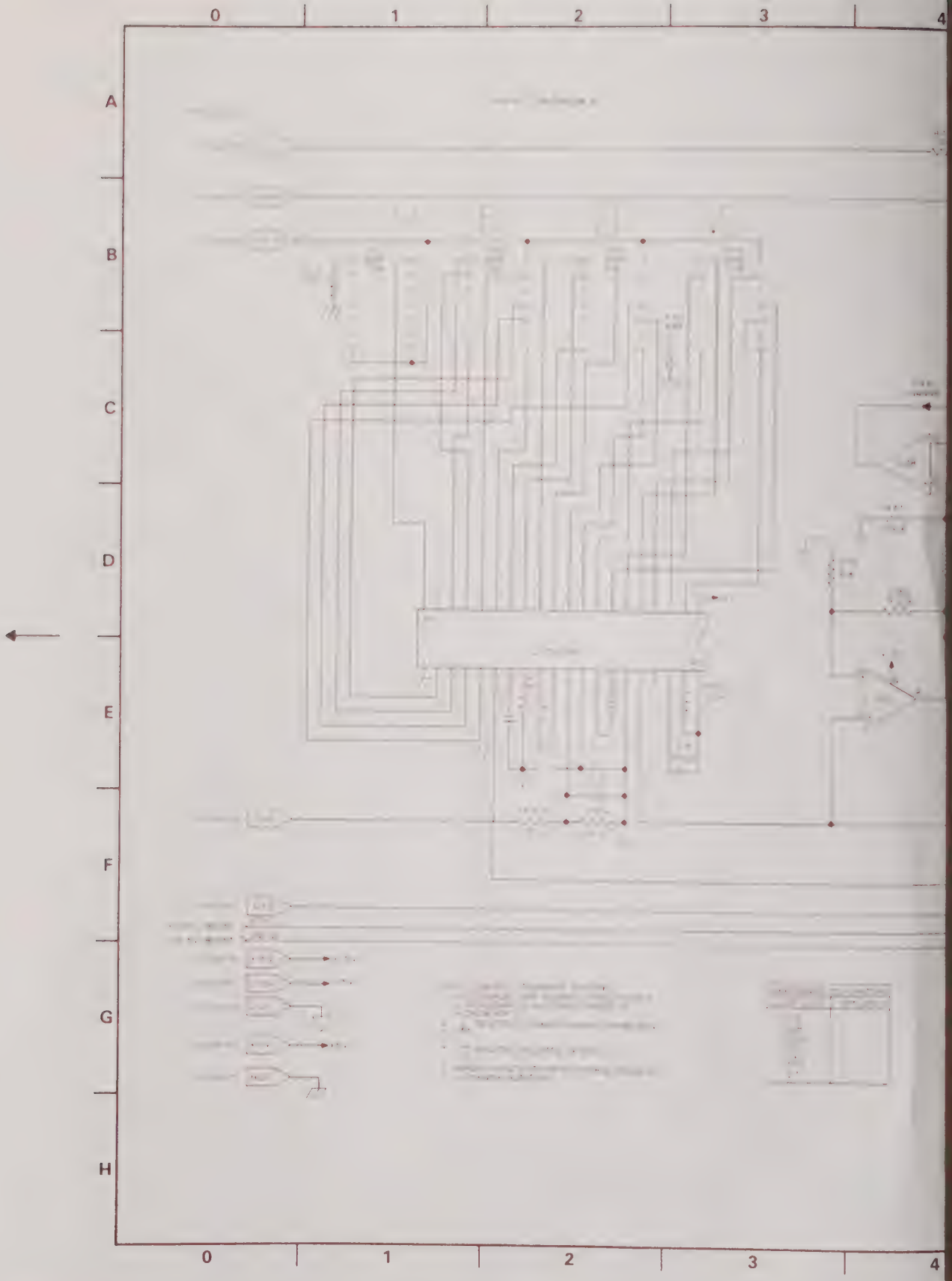
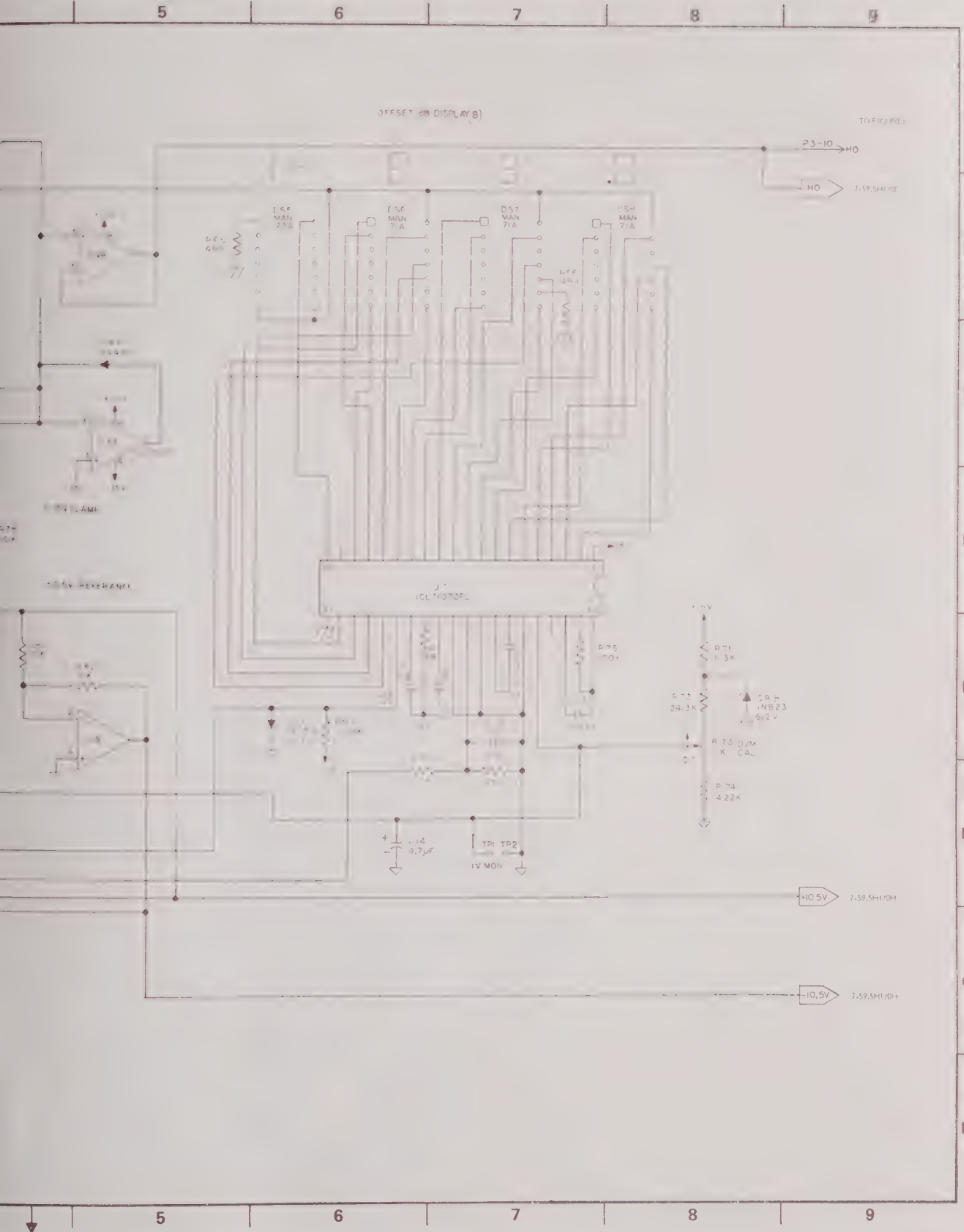


Figure 7-59, Front Panel (A1) PCB Schematic Diagram Sheet 2.


OFFSET dB DISPLAY B)
TO FIGURE
P3-10
M0
7-59,SH1/0F
DS6 MAN 7A
DS6 MAN 7A
DS7 MAN 7A
DS8 MAN 7A
R71 1.3K
R72 24.3K
SR5 1N823
6.2 V
R73 K DVM CAL
R74 4.22K
R75 10K
.14 4.7μF
TP1 TP2
1V MON
+10.5V
7-59,SH1/0H
-10.5V
7-59,SH1/0H

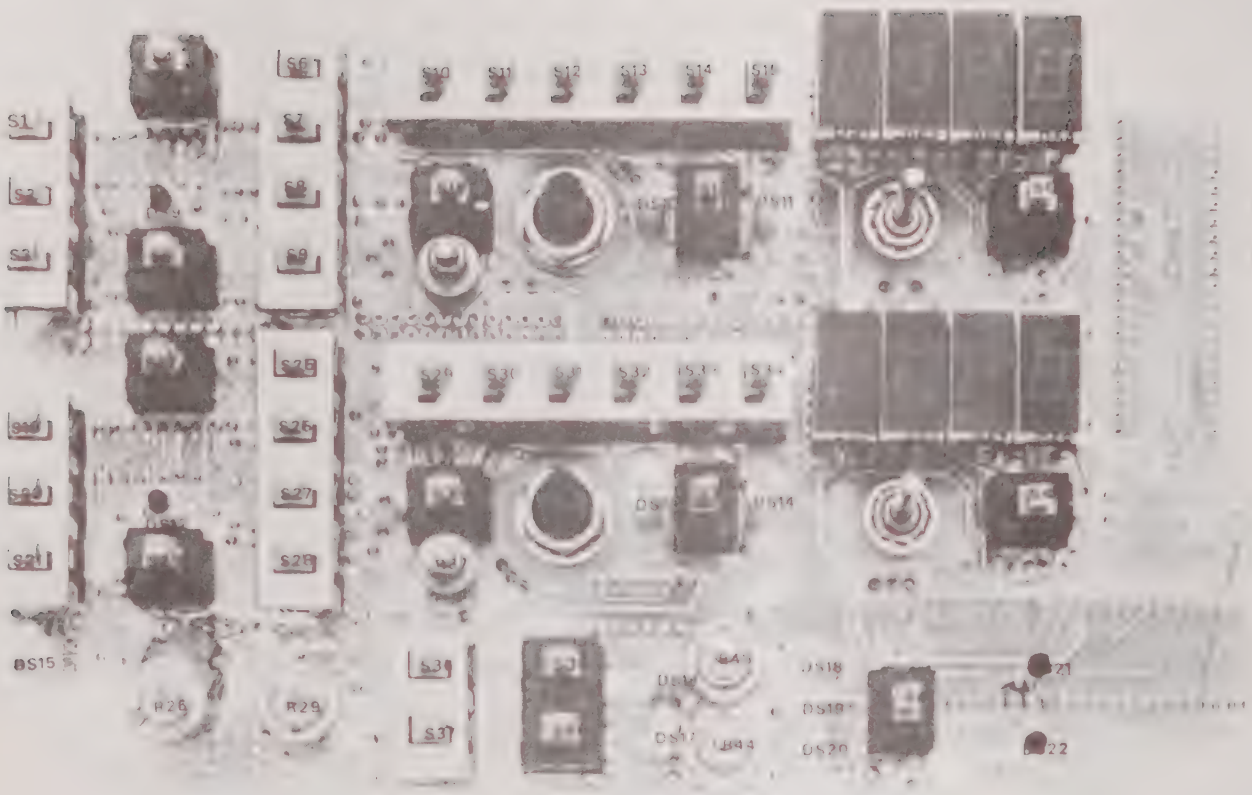


Figure 7-58. Front Panel (A1) PCB Parts Locator Diagram Sheet 2.

Figure 7-59.

7-7.2 Vertical Signal Multiplexing, Hold-During-Bandswitch/Retrace, and Hold-During-Vertical Conversion Circuits

These circuits are described below. A parts locator diagram for the circuits is shown in Figure 7-61, and the schematic is shown in Figure 7-62.

a. Vertical Signal Multiplexing Circuit. This circuit multiplexes the output signal from the Channel A and Channel B dB per division gain circuits, VOA and VOB, so that one group of digital circuits can be used to digitize and store measurement and refresh data. Multiplexing is accomplished by FET switches U1A and U1B. The logic voltages that control these two switches, LINTA and HINTA, come from the A/B Alternating Sweep switching circuit (paragraph 7-7.12). The LINTA control line is LOW when Channel A is on, and the HINTA control line is LOW when Channel B is on. When both channels are on, LINTA and HINTA alternate between a HIGH and a LOW in synchronism with the sweep generator retrace blanking pulse.

b. Hold-During-Bandswitch/Retrace Circuit. This circuit prevents the vertical data from being applied to the vertical A/D converter when either the sweep generator is retracing or its RF oscillator is bandswitching. Vertical signal hold is provided by FET switch U1C. The logic voltage that controls this switch, LDV, originates with the COMP BLANK INPUT signal from the A8 board. The COMP BLANK INPUT signal can be externally supplied via the rear panel Z AXIS INPUT connector or generated internally on the A8 board (paragraph 7-11.1), depending upon the setting of the rear panel Z AXIS SELECT switch. When the sweep generator's sweep retraces or its RF oscillator switches between internal oscillators, this line goes HIGH and opens U1C. U1C remains open until the sweep retrace or dwell period has elapsed.

c. Hold-During-Vertical Conversion Circuit. This circuit holds the vertical data while the converter is in a conversion cycle (the converter takes nine clock cycles to complete a conversion once it has started). Vertical signal hold is provided by FET switch U1D. The line that controls this switch, HHOLD, comes from the Horizontal and Vertical A/D Converter circuits. This line goes HIGH when a conversion cycle starts and stays HIGH until conversion is complete.

7-7.3 REFERENCE dBm Indicator Flash Circuit

This circuit (Figure 7-62) causes the Channel A and the Channel B REFERENCE dBm indicators to flash when the channel is uncalibrated for dBm measurements. The channel is uncalibrated when either the INPUT switch is in A-R (B-R) or when the MEMORY switch is in SUBTRACT, AVG, or RECALL. The astable multivibrator shown in Figure 7-60 is composed of transistors Q8 and Q9 (Figure 7-62) and their associated components. The switches and LEDs shown on the diagram are located on the front panel PCB schematic, Figure 7-59, Sheet 1.

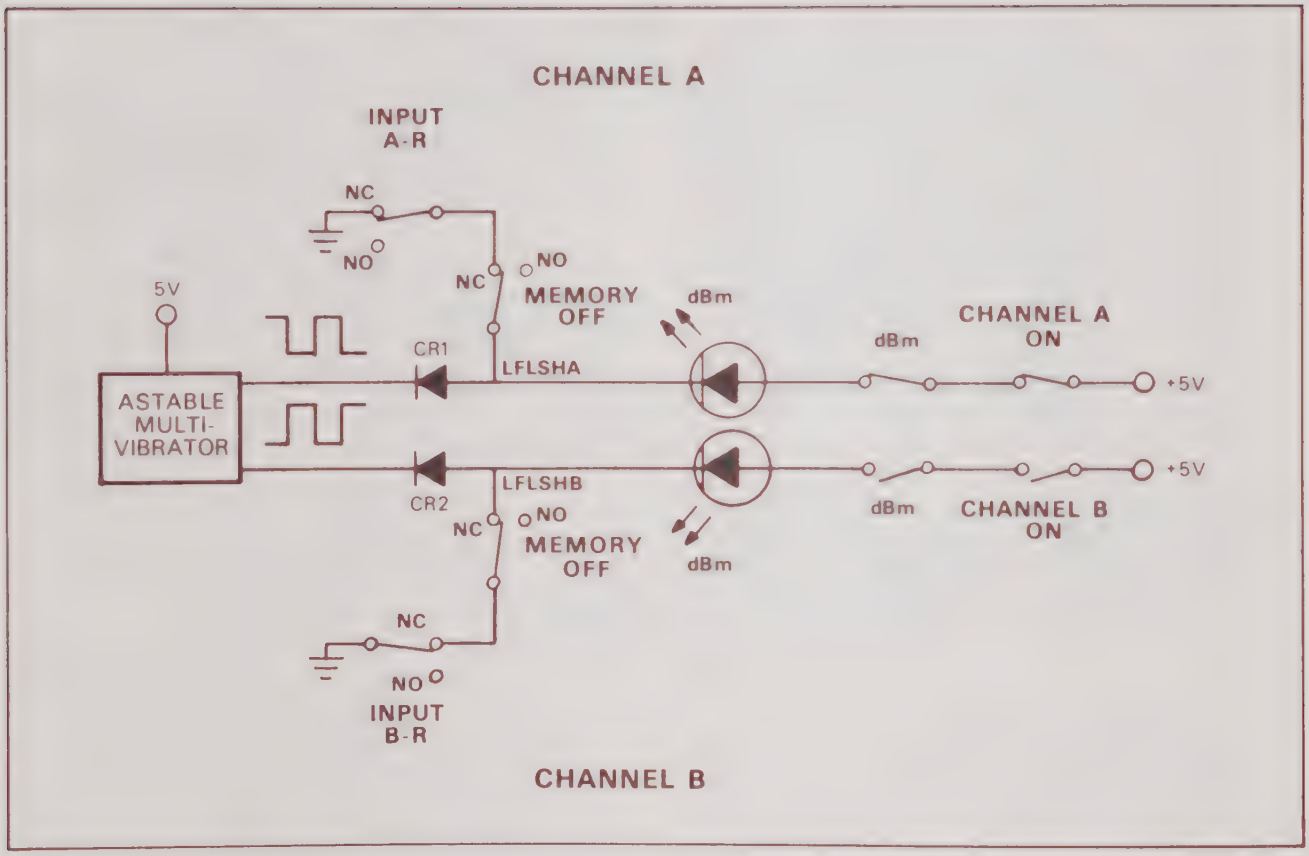


Figure 7-60. Reference dBm Indicator Flash Circuit, Simplified Schematic Diagram

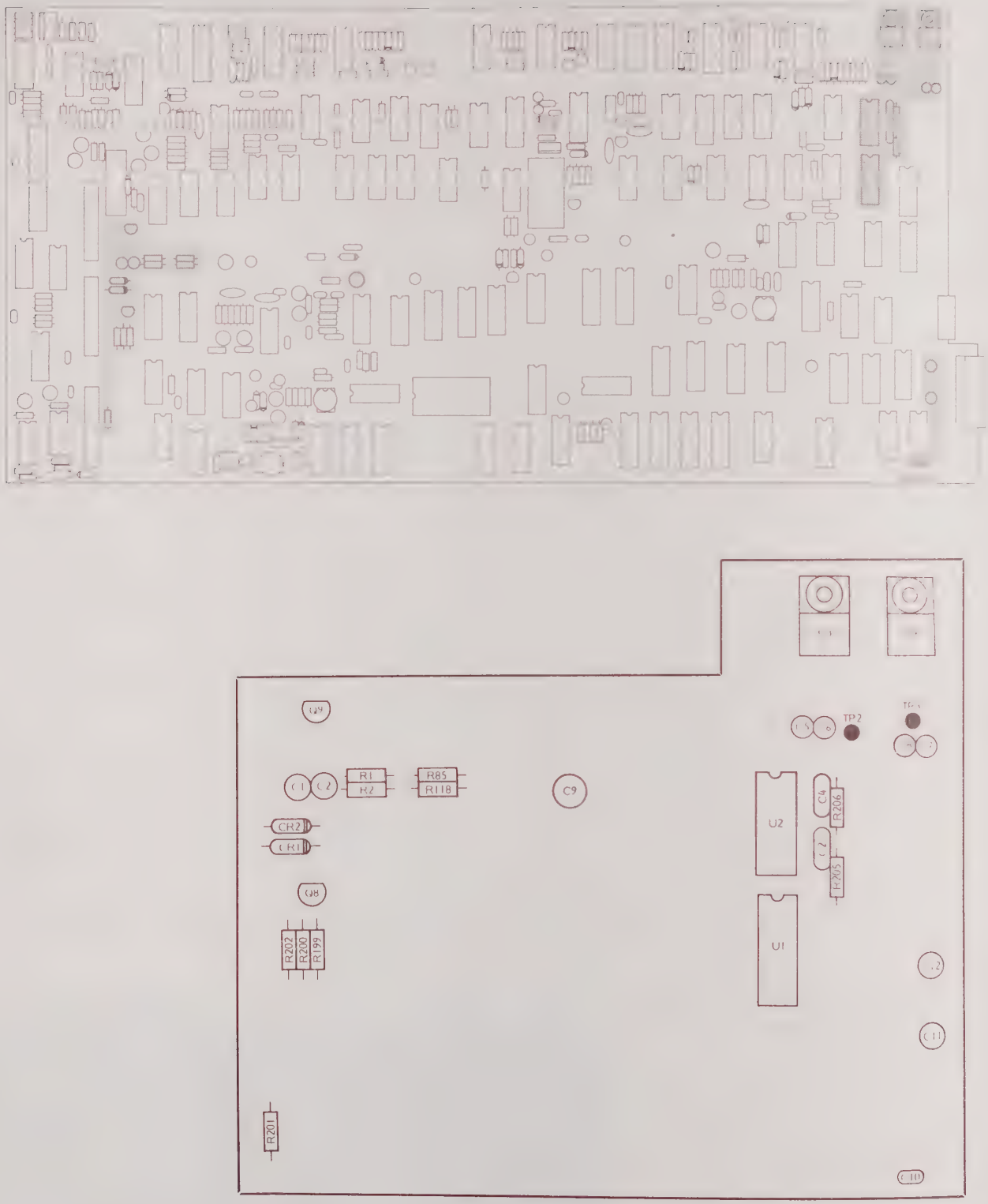
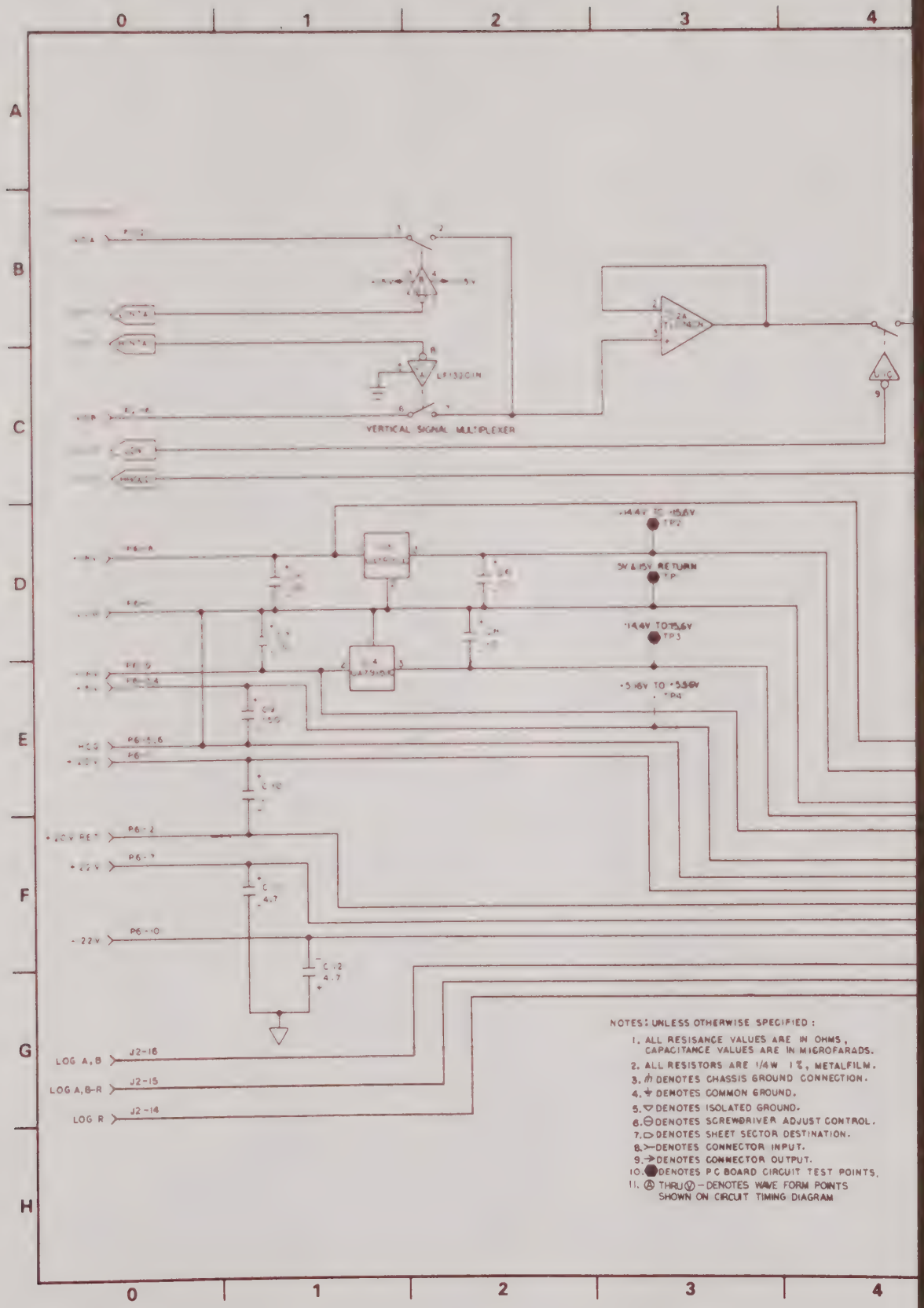
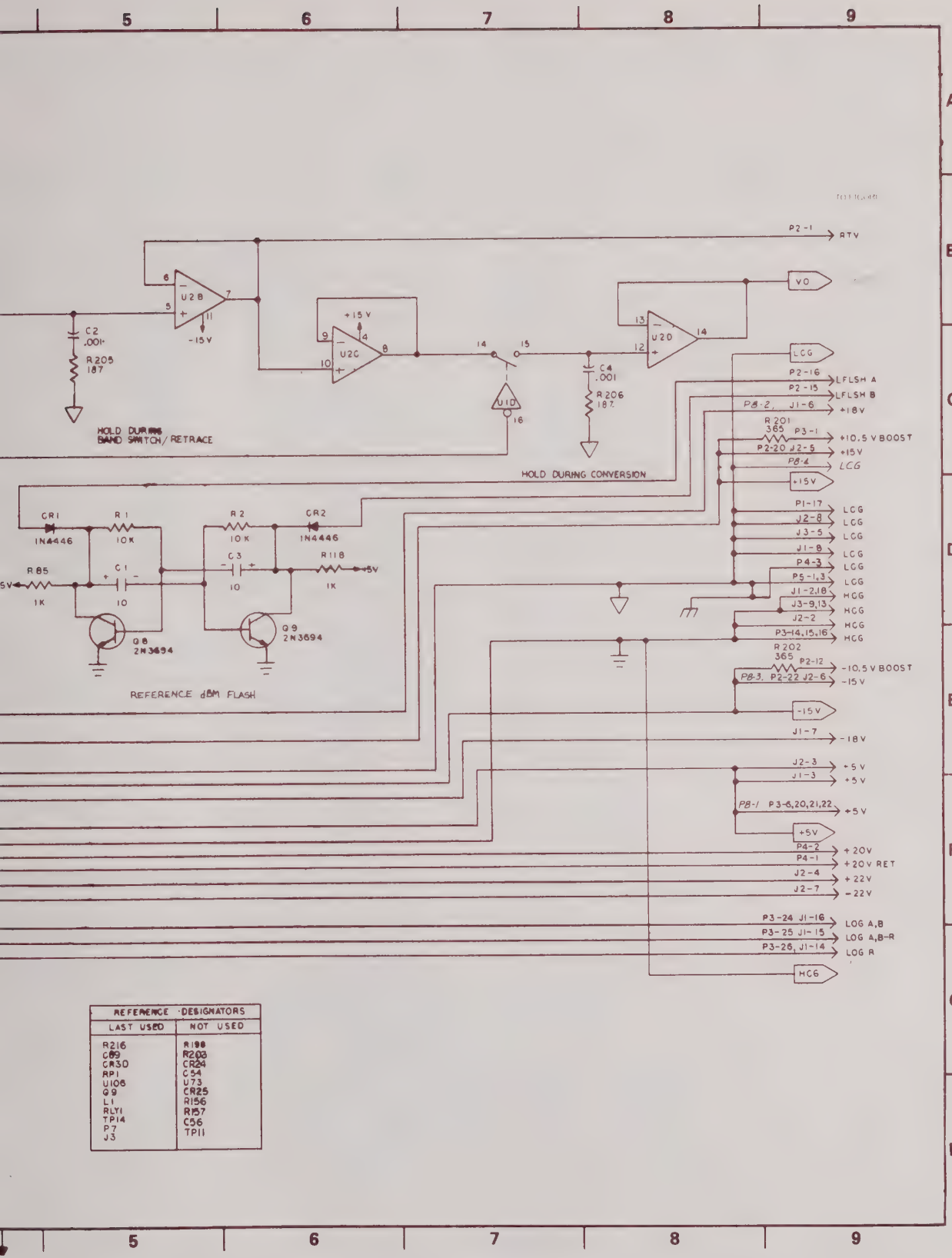


Figure 7-61. Digital (A2) PCB Vertical Signal Multiplexing, Hold-During-Bandswitch/Retrace, and Hold-During-Vertical Conversion Circuits Parts Locator Diagram



NOTES: UNLESS OTHERWISE SPECIFIED :

1. ALL RESISANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W 1%, METALFILM.
3. ⏚ DENOTES CHASSIS GROUND CONNECTION.
4. ⏚ DENOTES COMMON GROUND.
5. ▽ DENOTES ISOLATED GROUND.
6. ⊖ DENOTES SCREWDRIVER ADJUST CONTROL.
7. ▷ DENOTES SHEET SECTOR DESTINATION.
8. >— DENOTES CONNECTOR INPUT.
9. —> DENOTES CONNECTOR OUTPUT.
10. ● DENOTES P C BOARD CIRCUIT TEST POINTS.
11. Ⓐ THRU Ⓥ — DENOTES WAVE FORM POINTS SHOWN ON CIRCUIT TIMING DIAGRAM



REFERENCE DESIGNATORS	
LAST USED	NOT USED
R216	R198
C89	R203
CR30	CR24
RP1	C54
U106	U73
Q9	CR25
L1	R156
RLY1	R157
TP14	C56
P7	TP11
J3	

Figure 7-62. Digital (A2) PCB Vertical Signal Multiplexing, Hold-During-Bandswitch/Retrace, and Hold-During-Vertical Conversion Circuits Schematic Diagram

Figure 7-61.

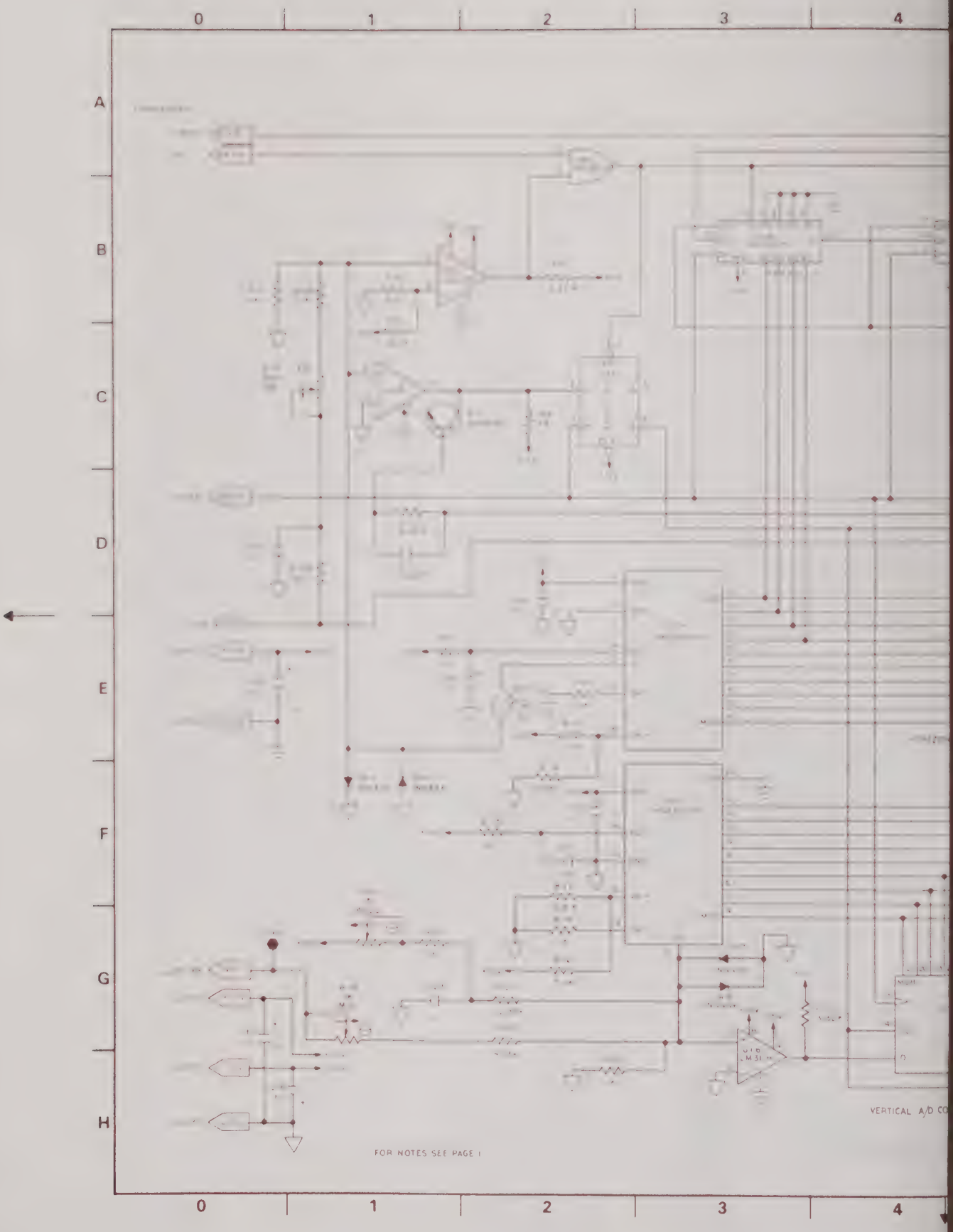
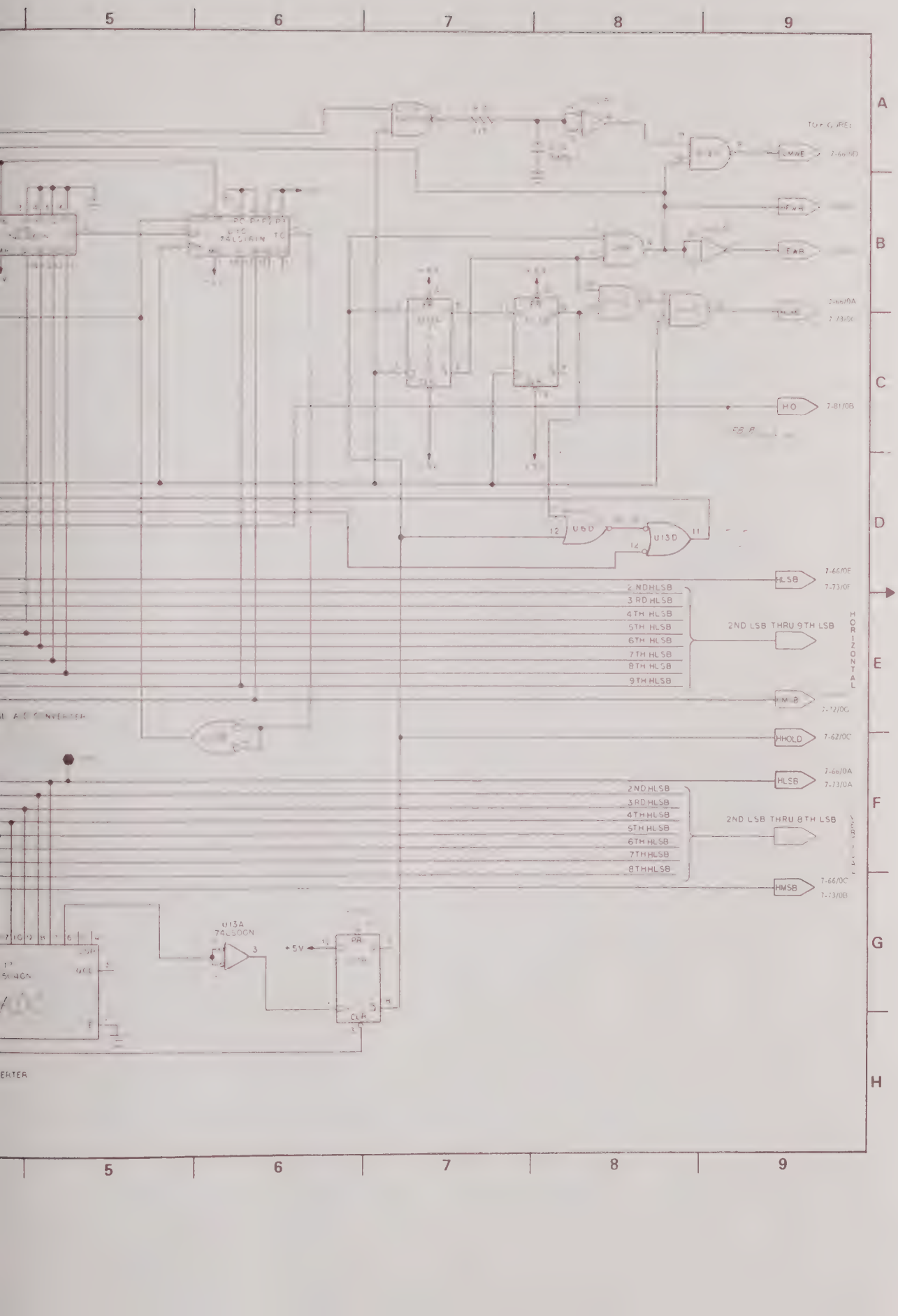
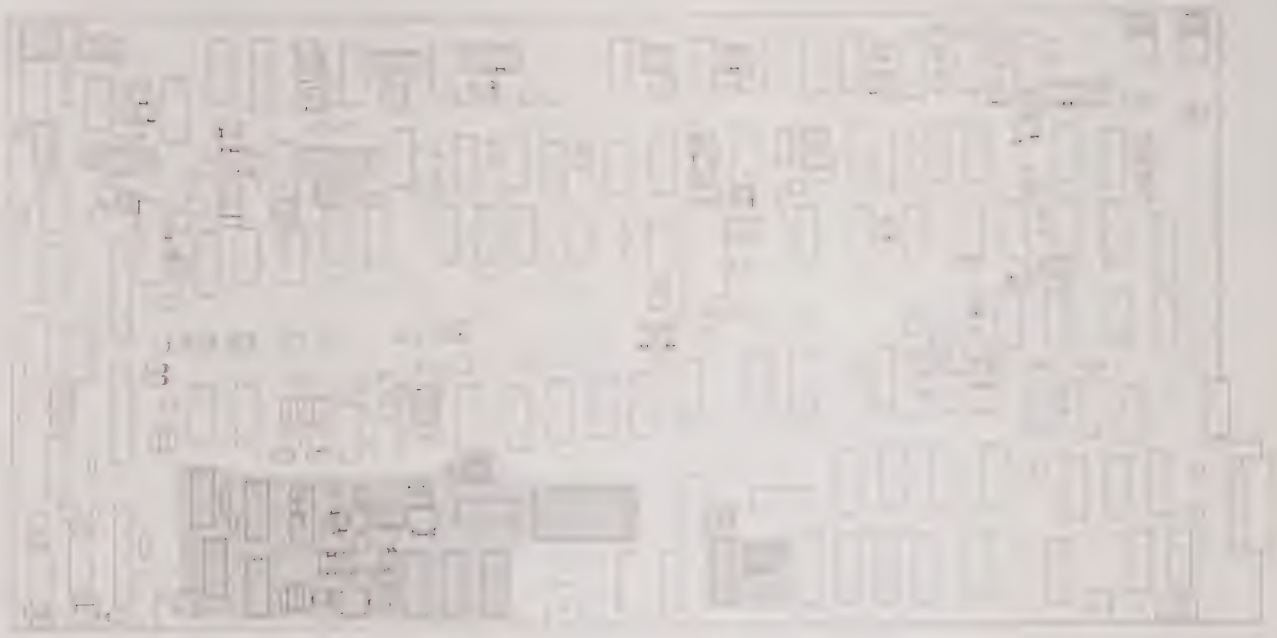
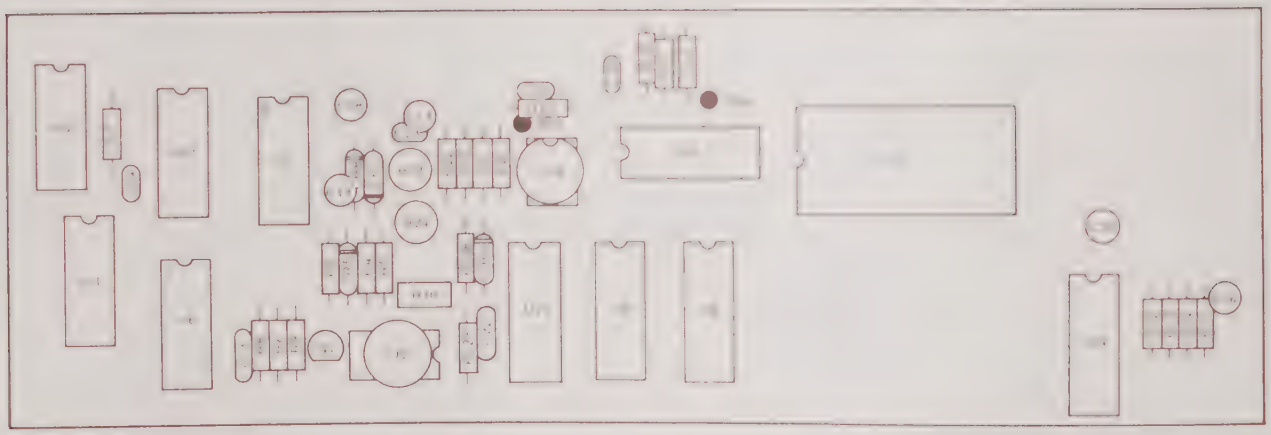


Figure 7-63. Digital (A2) PCB Horizontal and Vertical Converter Circuits Schematic Diagram


5
6
7
8
9
A
B
C
D
E
F
G
H
HO
7-81/0B
U6D
U13D
HLSB
7-66/0E
7-73/0F
2ND HLSB
3RD HLSB
4TH HLSB
5TH HLSB
6TH HLSB
7TH HLSB
8TH HLSB
9TH HLSB
2ND LSB THRU 9TH LSB
HORIZONTAL
HHOLD
7-62/0C
HLSB
7-66/0A
7-73/0A
2ND HLSB
3RD HLSB
4TH HLSB
5TH HLSB
6TH HLSB
7TH HLSB
8TH HLSB
2ND LSB THRU 8TH LSB
VERTICAL
HMSB
7-66/0C
7-73/0B
U13A
74LS00N
+5V
PR
CLR



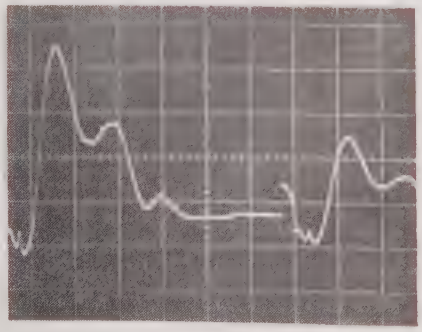


Waveform Conditions

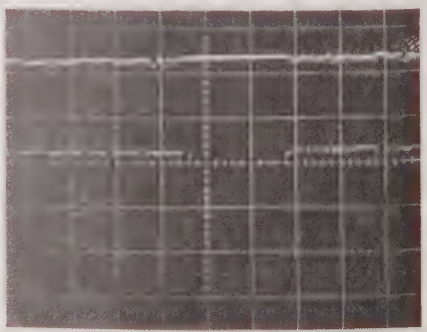
560A Controls:
Channel A – ON
dB PER DIVISION – .5
Channel B – ON
dB PER DIVISION – 1.

6647A Controls:
TRIGGER–AUTO
SWEEP TIME–100ms

Oscilloscope Controls:
Vertical V/division – See waveform
Horizontal Sweep – 5 ms/division
Input – Dc couple
Triggering – Trigger with 560A Channel A signal



TP 5 – V/div. 2



TP 6 – V/div. 5 (ground on centerline)

Figure 7-64. Digital (A2) PCB Horizontal and Vertical Converter Circuits Parts Locator Diagram

Figure 7-63.

7-7.4 Horizontal and Vertical A/D Converter Circuits

These two circuits operate together to convert the analog horizontal and vertical signals into digital words that can be processed by, stored in, and retrieved from the storage memory and that can be used to update the refresh memory. The horizontal sweep ramp is digitized into a 10-bit word that provides 1024 discrete address locations, and the vertical signal is digitized into a 9-bit word that provides 512 points of vertical resolution. The schematic for these circuits is shown in Figure 7-63, and the parts locator diagram is shown in Figure 7-64. The circuits are described below.

a. Horizontal A/D Converter Circuit. This circuit is a tracking A/D converter composed of binary counters U8, U9, and U10; comparator U5B; flip-flop U7A, and associated gates and components. The tracking-type circuit is used because (1) it can be set to begin conversion at the start of each ramp, (2) it can accurately track the horizontal sweep ramp's linear voltage excursion faster than a successive approximation converter, and (3) it can be made to produce a trigger pulse for synchronization of the vertical A/D converter. To set the converter to begin conversion at the start of the horizontal sweep, the binary counters are reset to 0000000000 by the sweep generator's retrace blanking pulse (HRTR control line). To track the linear rise of the horizontal sweep ramp, the binary counters' output count is converted to a voltage and compared to the instantaneous voltage of the horizontal sweep ramp. The output count of the binary counters is converted by U14 to a discrete current. The input horizontal ramp voltage (HO signal line) is converted to a current by the input resistor network, consisting of R129, R10, and R128. When the current of the horizontal ramp exceeds the current produced by the D/A converter, the control circuitry consisting of U5B, U7A, and U13D produces a negative-going trigger. The leading edge of this trigger starts the vertical A/D conversion cycle; this trigger pulse leading edge also sets the HHOLD control line HIGH. A HIGH on the HHOLD line opens U1D in the Hold-During-Conversion circuit (Figure 7-62) and prevents the vertical A/D converter from changing until conversion of the present signal is complete. After nine clock pulses the vertical A/D conversion cycle is complete, and the end of conversion detector generates a pulse from its $\overline{Q}$ output that causes the binary counters to increment their count on the leading edge of the next clock pulse from the system and Output Counter Clock circuit (paragraph 7-7.17). This sequence of events is repeated 1024 times for each horizontal sweep ramp input.

b. Vertical A/D Converter Circuit. This circuit consists of two subcircuits: converter and output control. The converter, a successive approximation type, is composed of successive approximation register U17, D/A converter U15, comparator U16, flip-flop U17B, and associated gates and components. This type of circuit is used because it needs the same number of clock cycles (9) for each conversion, regardless of the amplitude of the input analog voltage. The input to this converter is the VO signal from the Hold-During-Conversion circuit. The voltage excursions of this signal are between plus and minus 10 volts. The conversion of the VO signal takes nine clock cycles (9 μs); at the beginning of the tenth clock pulse, the end-of-conversion detector U7B-$\overline{Q}$ output goes LOW to produce a positive pulse (U7B-$\overline{Q}$ was set HIGH by the $\overline{Q}$ trigger pulse from U7A).

The output control circuit is composed of flip-flops U11A, U11B, gates U12A, U6B, U13C, U6C, and inverters U12B and U12D. This circuit generates signals that are used for both storage and refresh memory control. A timing diagram that shows the timing relationship between these signals is shown in Figure 7-65.

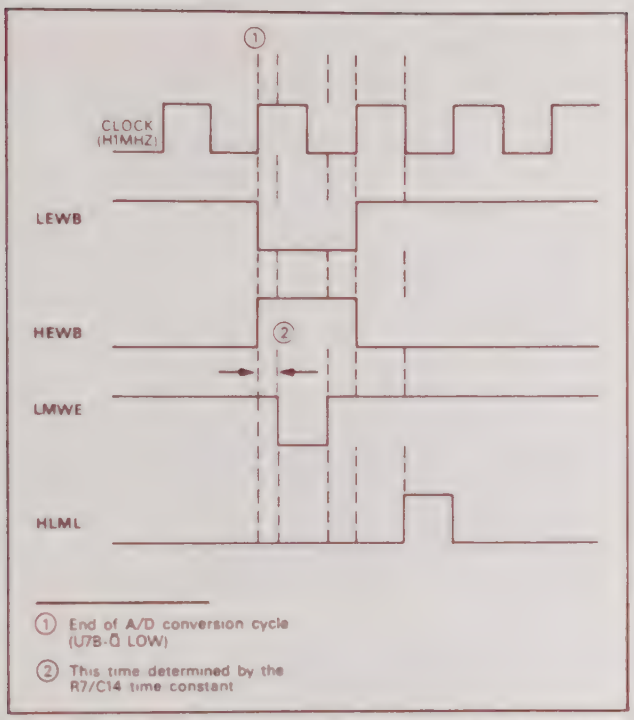


Figure 7-65. Timing Diagram for LEWB, HEWB, LMWE, and HLML Signals

7-7.5 Storage Memory and Memory D/A Circuits

These circuits are described below. Their parts locator diagram is shown in Figure 7-66, and their schematic is shown in Figure 7-67.

a. Storage Memory Circuit. This circuit has two functions: (1) it provides storage locations for the vertical and horizontal measurement data, and (2) it provides continuous readout of vertical data to the memory D/A circuit.

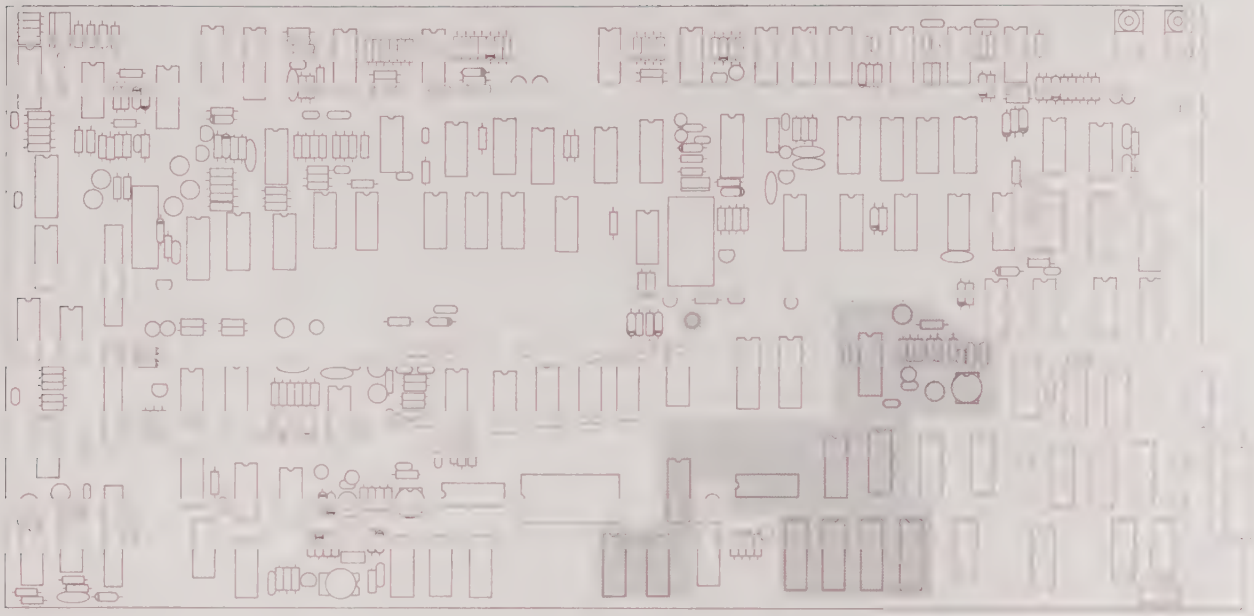
The storage memory is partitioned into two separate 9 x 1k memory circuits--one circuit for storing Channel A data and the other circuit for storing Channel B data. Control lines HINTA and LINTA determine which memory bank is enabled. When LINTA is LOW, the Channel A memory bank is enabled. This memory bank consists of 4k random-access memories (RAMs) U24, U25, and 1k RAM U105. Conversely, when HINTA is LOW, the Channel B memory bank is enabled. This memory bank consist of 4k RAMS U26, U27, and 1k RAM U104.

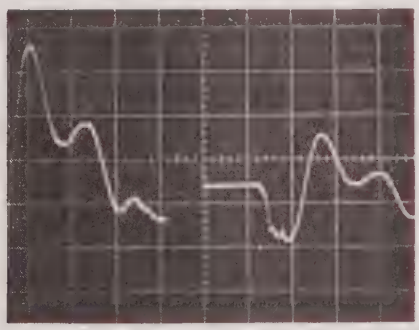
Data inputs to the storage memory are the 10-bit horizontal word and 9-bit vertical word from the Horizontal and Vertical A/D Converter circuits. The horizontal word is applied to the address lines of the six RAM chips; the vertical word is applied to tri-state buffers U18 and U19.

Storage memory is continually read because the read (HLML) control line is set to a logic 1 upon completion of each vertical conversion cycle (paragraph 7-4.4b). This logic 1 clocks the vertical data pointed to by the horizontal address word into temporary storage latches U20 and U21 and then into D/A converter U22. (Remember from the discussion on horizontal conversion, vertical data conversion starts when the instantaneous voltage of the horizontal sweep ramp exceeds the binary counters' output count, which is the horizontal address. Consequently, the horizontal address is always one count behind and points to the vertical data.)

To write into storage memory, the STORE TRACE pushbutton is depressed. When this occurs, the LWME signal goes LOW. This signal gates the vertical data through the tri-state buffers at the same time that it enables the write enable ($\overline{WE}$) pin on the six RAM chips. Vertical data is then written into either the Channel A or the Channel B memory-bank, at an address corresponding to the voltage of the horizontal sweep ramp.

b. Memory D/A Converter Circuit. This circuit converts the vertical data bits into an analog current via D/A converter U22 and associated components, then it converts the analog current into a voltage via operational amplifier U23 and associated components. The current-to-voltage converter U23 is adjusted by Gain and Offset potentiometers R31 and R34, respectively, so that its output voltage is normalized to ±10 volts. The output of this circuit, MEM OUT, goes to the Sensitivity Storage circuit.





TP 7

Waveform Conditions

560A Controls:
Channel A — ON
dB PER DIVISION — .5
STORE TRACE — Depressed
Channel B — ON
dB PER DIVISION — 1.
STORE TRACE — Depressed

6647A Controls:
TRIGGER—AUTO
SWEEP TIME—100ms

Oscilloscope Controls:
Vertical V/division — 2
Horizontal Sweep — 5 ms/division
Input — Dc couple
Triggering — Trigger with 560A
Channel A signal

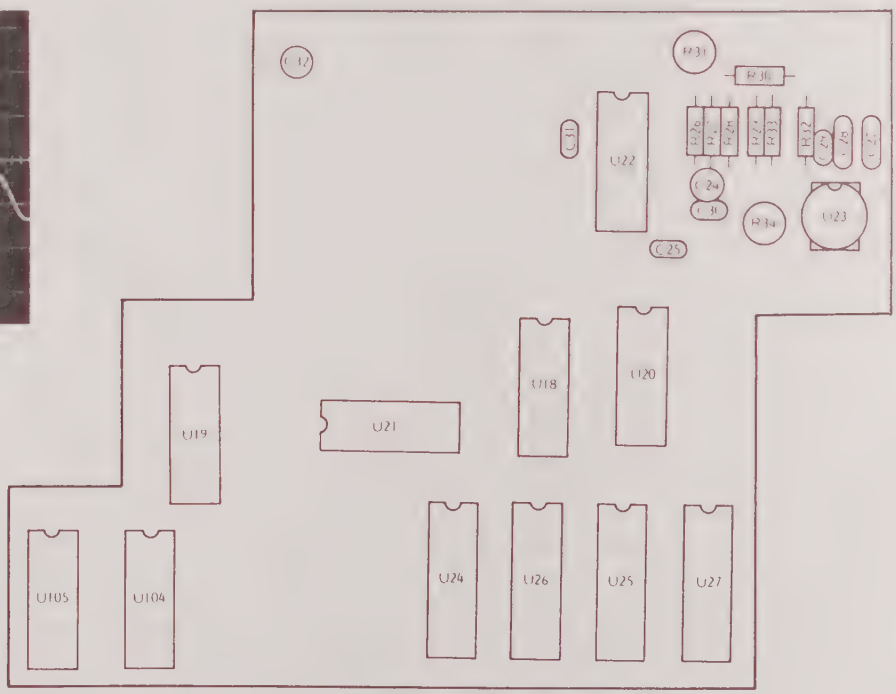
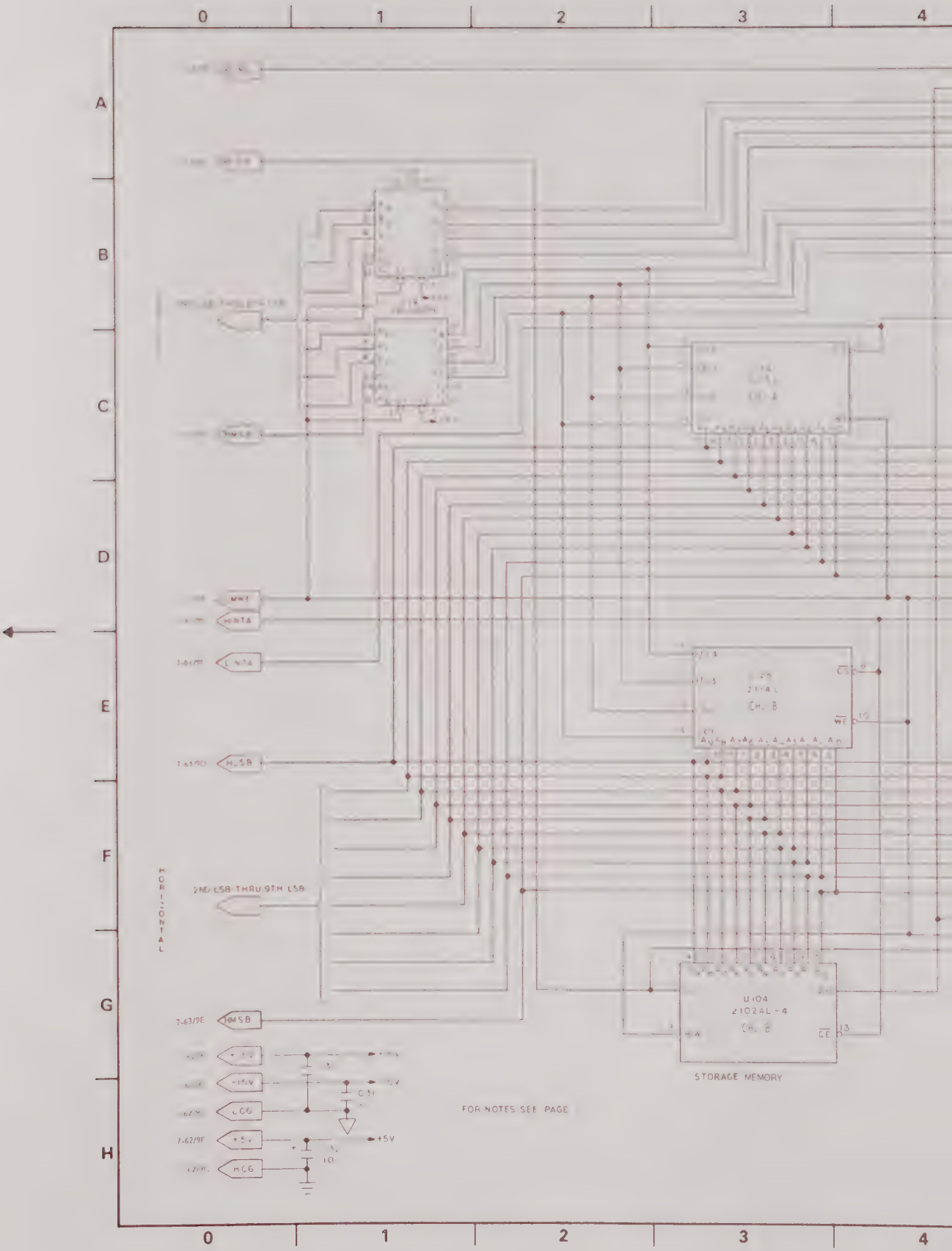


Figure 7-66. Digital (A2) PCB Storage Memory and Memory D/A Circuits Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
MWRT
MINTA
LINTA
MSB
2ND LSB THRU 5TH LSB
HORIZONTAL
MMSB
+5V
-15V
LOG
+5V
MOG
+5V
U104
Z102AL-4
CH. B
STORAGE MEMORY
FOR NOTES SEE PAGE

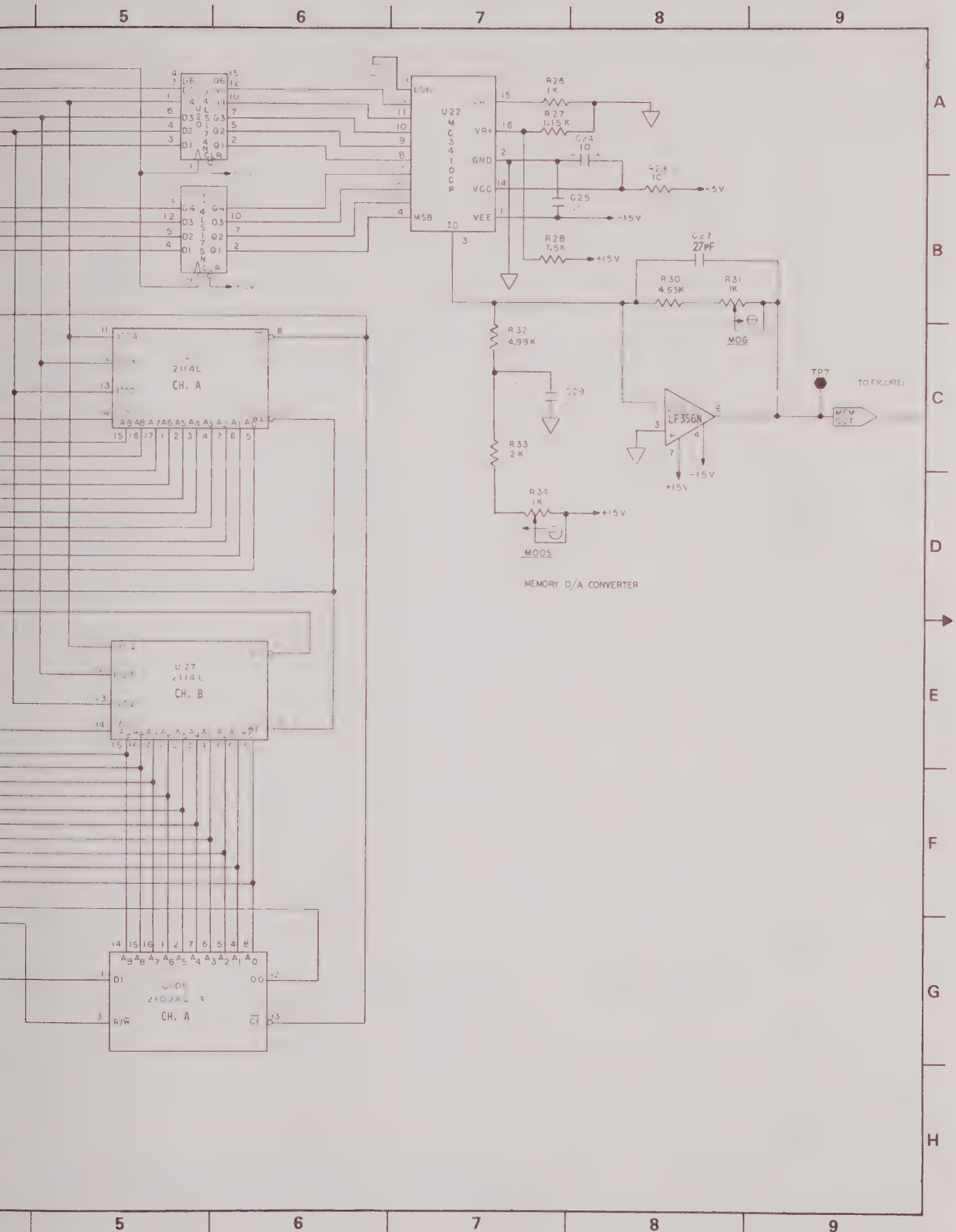


Figure 7-67. Digital (A2) PCB Storage Memory and Memory D/A Circuits Schematic Diagram

Figure 7-66.

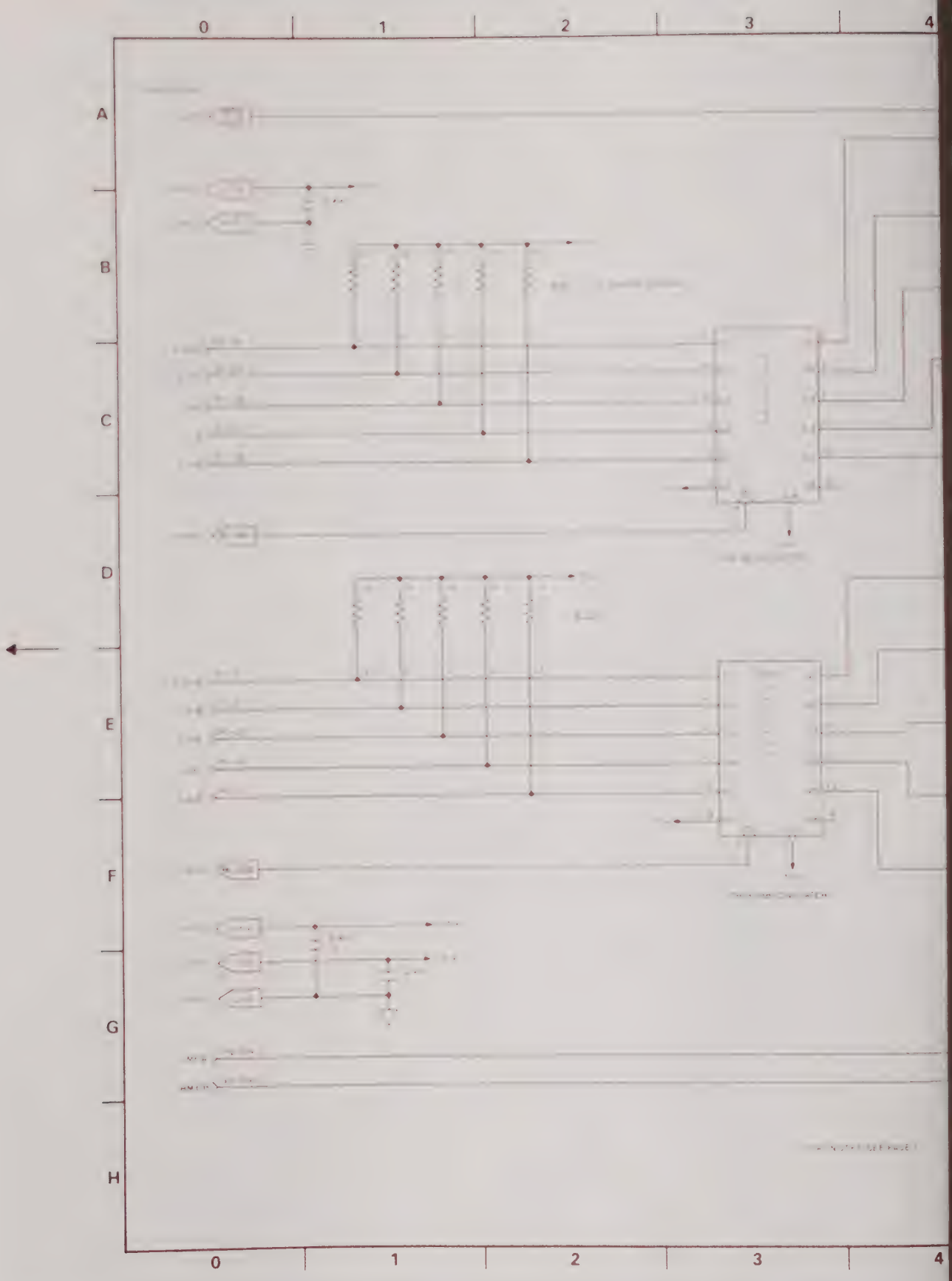


Figure 7-68. Digital (A2) PCB Sensitivity Storage Circuit Schematic Diagram

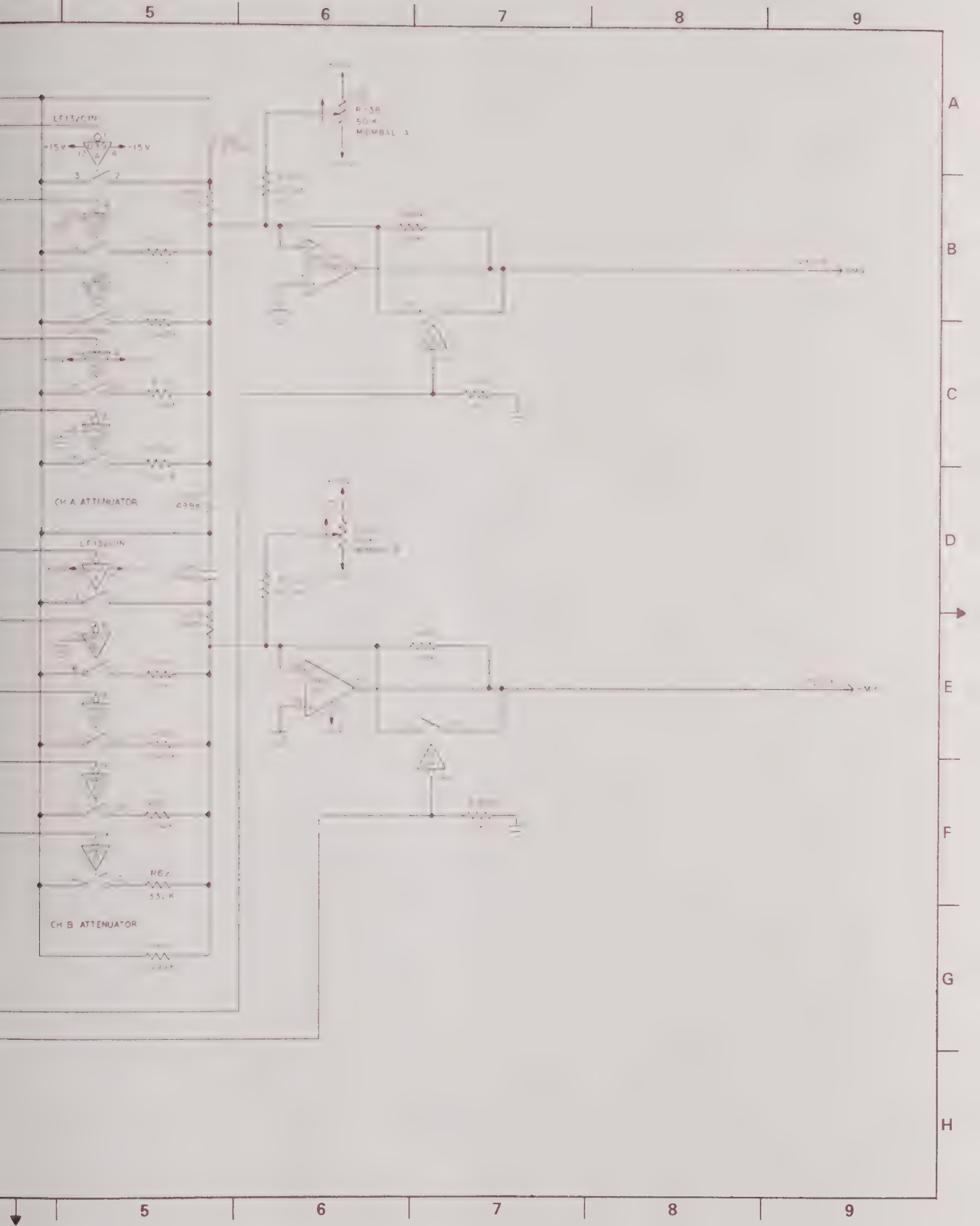

5
6
7
8
9
A
B
C
D
E
F
G
H
LF132CIN
+15V
-15V
CH A ATTENUATOR
CH B ATTENUATOR
R67
55.K
50.K

Figure 7-69. Digital (A2) PCB Sensitivity Storage Circuit Parts Locator Diagram

Figure 7-68.

7-7.6 Sensitivity Storage Circuit

This circuit performs the following three functions: (1) it memorizes the dB PER DIVISION switch setting(s) at which the vertical data is stored, (2) it attenuates the memory output (MEM OUT) signal by exactly the same amount as the memory input signal was amplified by the dB per division gain circuit, and (3) it effectively reduces the memory output signal to zero when the MEMORY OFF switch is selected. The circuitry for accomplishing these three functions is identical for Channels A and B. In the following paragraphs, the Channel A circuits are described. The schematic for this circuit is shown in Figure 7-68, and the parts locator diagram is shown in Figure 7-69.

Switch memorization is accomplished using hex latch U37. When one or more dB PER DIVISION pushbuttons are depressed, a logic 0 is applied to the applicable D1 thru D5 input(s). This logic 0, which is used to energize the associated FET switch, is clocked thru the latch when HLDBA (load dB A) goes HIGH. HLDBA goes HIGH at the end of the store trace cycle. (A store trace cycle is initiated when the STORE TRACE pushbutton is depressed.)

Memory output signal attenuation is accomplished using the FET switches, operational amplifier, and components associated with hex latch U37. This circuitry is a mirror image of the dB per division gain circuit contained on the A1 PCB (see the simplified diagram in Figure 7-70). This function allows the memory signal to be manipulated (subtracted, averaged, or recalled) at any dB per division switch setting. If this circuit were not included, memorized data could only be used at the dB PER DIVISION switch setting(s) at which it was stored; every time the dB PER DIVISION switches were changed, the input data would have to be rememorized at the new switch setting(s).

Reduction of the memory output signal to zero is accomplished by FET switch U39. When the MEMORY OFF switch is depressed, U39 closes and shunts R64, thereby reducing the U42A operational amplifier's gain to zero.

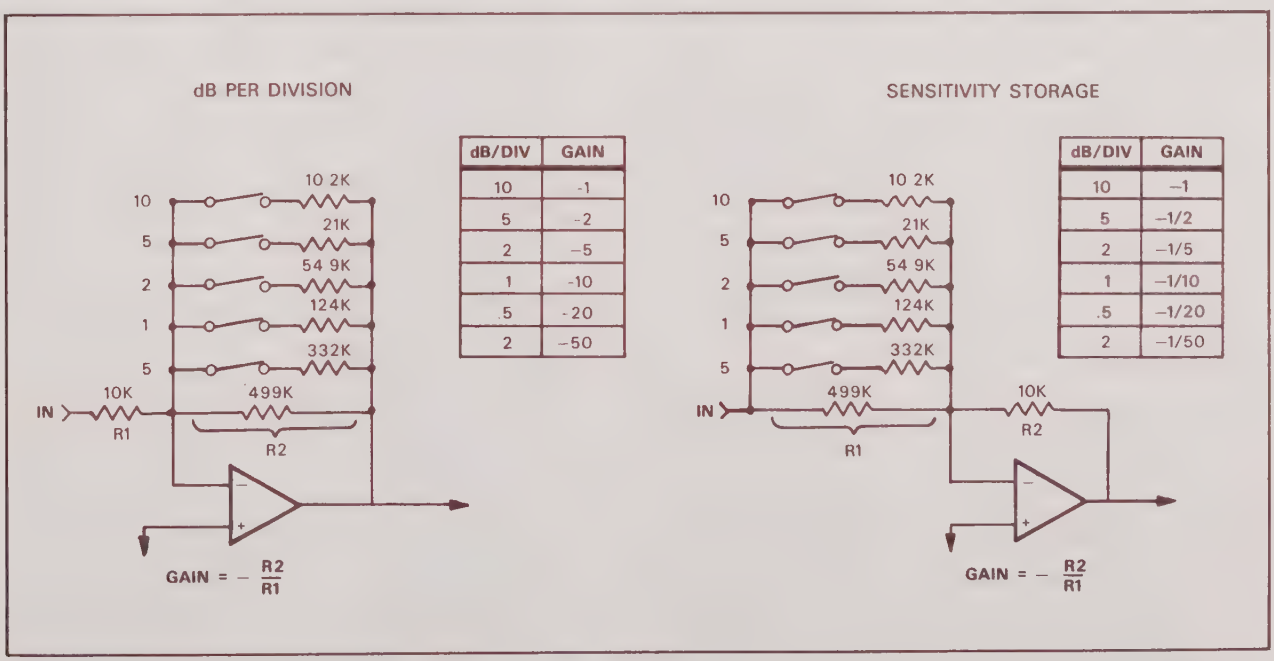


Figure 7-70. dB PER DIVISION Gain and Sensitivity Storage Attenuation Circuits

7-7.7 Refresh Address Control Circuits

These circuits consist of an output counter circuit, a multiplexer circuit, and a time-slot generator circuit. The parts locator diagram for these circuits is shown in Figure 7-71, and the schematic is shown in Figure 7-72.

a. Output Counter Circuit. This circuit generates the horizontal refresh address bits. The circuitry consist of binary counters U43, U44, U45, and U46. U43 is configured as a divide by 14 counter: its count output (CO) pin goes HIGH on the 14th count. U43 is enabled by the HOCEN line from the X-Y Plot Control Circuit (paragraph 7-7.22) and clocked by the HOCCLK line from the System and Output Counter Clock circuit (paragraph 7-7.17). If the 560A is not engaged in a plotting operation, the HOCCLK line is changing states at a 1 MHz rate. If the 560A is engaged in a plotting operation during refresh (X-Y PLOT and REFRESH pushbuttons depressed), HOCCLK is changing states at either a 488.3 or a 244.1 Hz rate. This HOCCLK rate depends on whether the 560A is in single or dual-channel sweep (paragraph 7-7.12). The output of U43 enables the refresh address counter circuit, which is composed of U44, U45, and U46. The refresh address counter circuit provides a 10-bit horizontal address that goes from 0 to 1023 (0000000000 to 1111111111) in 14.3 ms, in the refresh mode; 0 to 1023 in approximately 30 seconds, in the X-Y plot/refresh, single-sweep mode; or from 0 to 1023 in approximately 60 seconds, in the X-Y plot/refresh, dual-sweep mode.

b. Multiplexer Circuit. This circuit provides two functions:

- In single-channel operation, the circuit multiplexes between real time and refresh address bits to provide the refresh memory with real time addresses during memory update (i.e., writing new vertical data in the memory).
- In dual-channel operation, the circuit multiplexes between real time and refresh address bits in such a manner that Channel A real time address bits are mapped into memory locations 0 thru 511 and Channel B real time address bits are mapped into memory locations 512 thru 1023.

The circuitry for multiplexing the refresh address bits onto the refresh horizontal address bus consists of tri-state buffer U55 and the A1 thru A4 inputs of tri-state buffer U54. These two buffers are switched to their "on" state when the HERWB control line is LOW. This switching occurs when the vertical A/D converter's end of conversion detector output (U78-$\overline{Q}$) is inactive (no new vertical data available). Conversely, when the vertical A/D converter has completed a conversion and new data is available, U55 and U54 are in their "off" state. The real time horizontal address bits are then multiplexed onto the bus.

The circuitry for multiplexing the real time horizontal address bits onto the bus consist of tri-state buffers U51, U52, U53, the A5, A6 inputs of U54, and NAND gates U48A, U48B (configured as an inverter), U49B, and U49C. When either (but not both) Channel A or Channel B is on, U53 and the A5 and A6 inputs of U51 and U54 are switched "on;" this puts the 10 real time address bits from the horizontal A/D converter onto the address bus. When both channels are on, U52 and the A1 thru A4 inputs of U51 are switched "on;" this puts the nine most significant real time address bits, plus the LINTA control line bit onto the address bus. When Channel A is being displayed, LINTA is a logic 0; this holds the MSB LOW, which causes data to be loaded in memory locations 0 thru 511. Conversely, when Channel B is being displayed, LINTA is a logic 1; this holds the MSB HIGH, which causes data to be loaded in memory locations 512 thru 1023.

c. Timeslot Generator Circuit. This circuit generates the refresh memory read (HLRL) pulse, plus a three-clock-pulse-wide pulse used in the dot connector D/A converter circuit. The circuit is composed of hex latch U50, gates U47A, U47B, U47C, U79B, U47D, U48C, and inverters U49D and U48D. Hex latch U50 is configured as a shift register; it is enabled by the HOCEN control line and clocked (shifted) by the HOCCLK control line. The input to the first register, D2-Q2, is from U43.

On the 14th count of U43, the high state of the CO output is serially shifted thru U50 on the rising edges of the succeeding five clock pulses. The output of the Q2 register, along with that of the Q3 register, is ANDed with the LERWB control signal to produce the HLRL pulse. The LERWB line is HIGH when the vertical A/D converter's end of conversion detector output (Q78-$\overline{Q}$) is inactive, which means no new vertical data is available for writing into the refresh memory. Conversely, when new data is available, LERWB is LOW. The LOW state of LERWB inhibits an HLRL pulse from being generated. The logic state of the LERWB control line is synchronous with the logic state of the HOCCLK control line; therefore, the use of two shift register pulses that occur at different times insures the refresh memory is read out with each count from the output counter.

The three-clock-pulse-wide pulse supplied to the dot connector D/A converter is produced by the A4 thru A6 shift register outputs of U50 being gated by U47D and U48C.

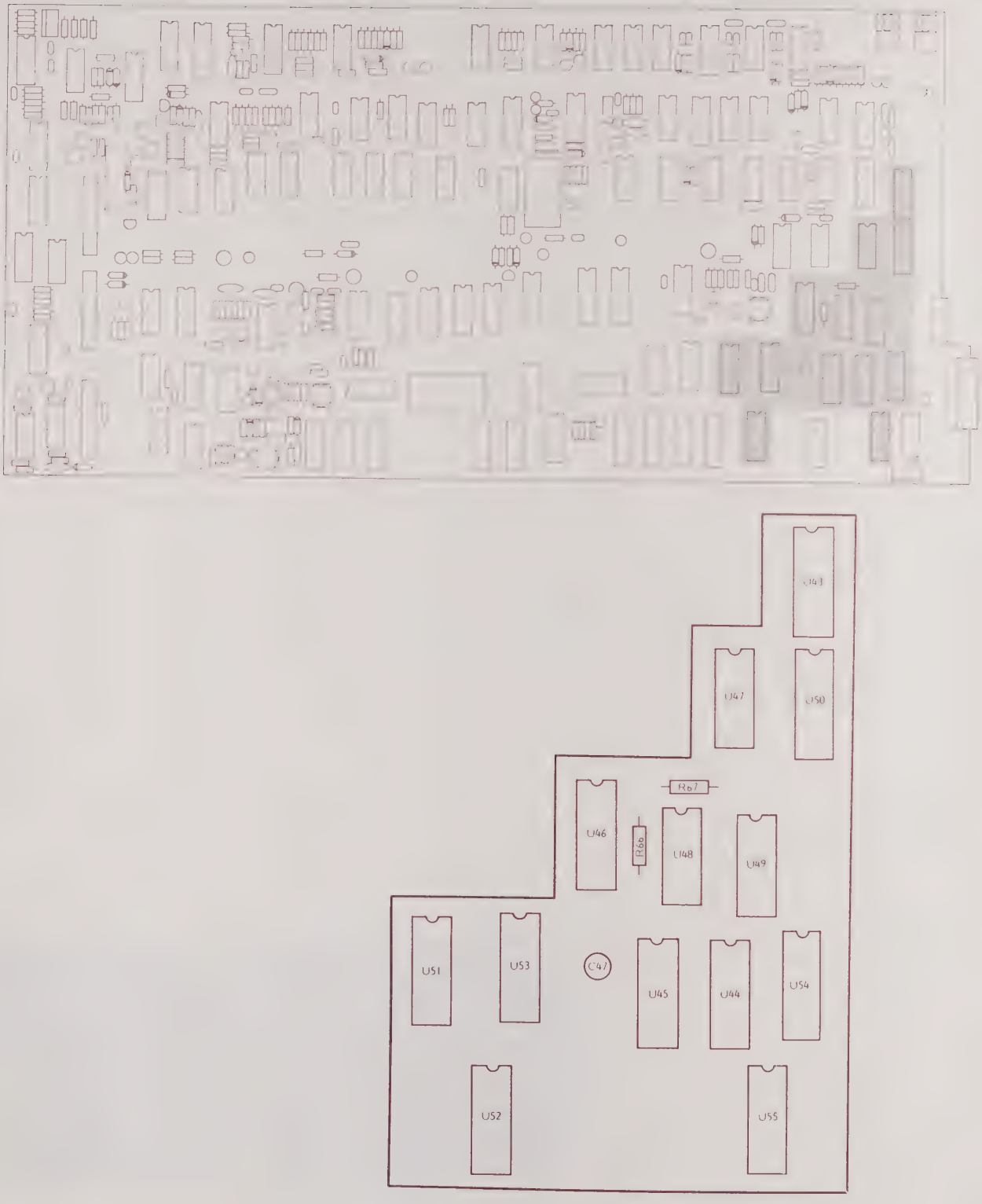
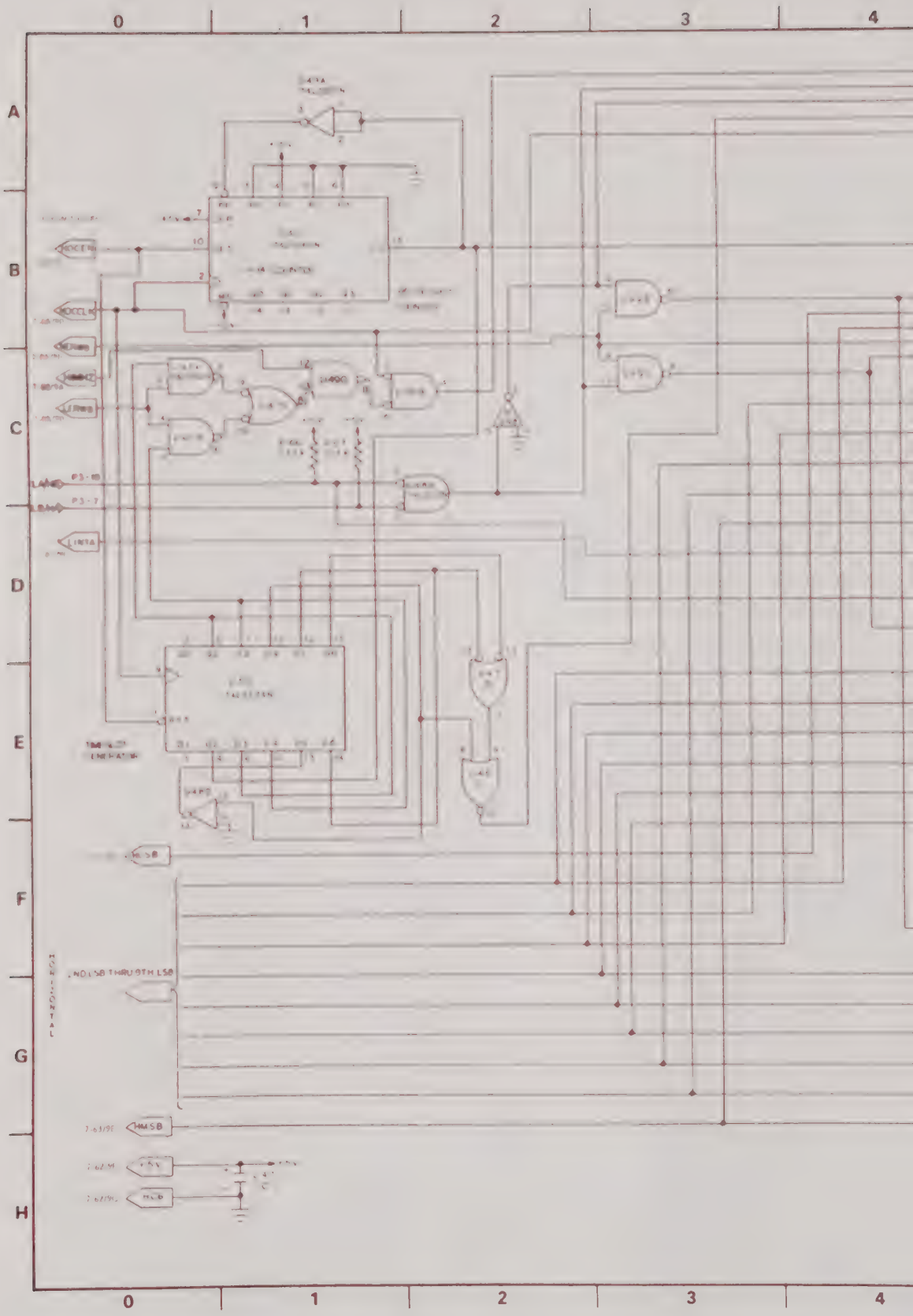


Figure 7-71. Digital (A2) PCB Refresh Address Control Circuits Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
P3-10
P3-7
LINT1A
MSB
LSB THRU 9TH LSB
HMSB
+5V
GND

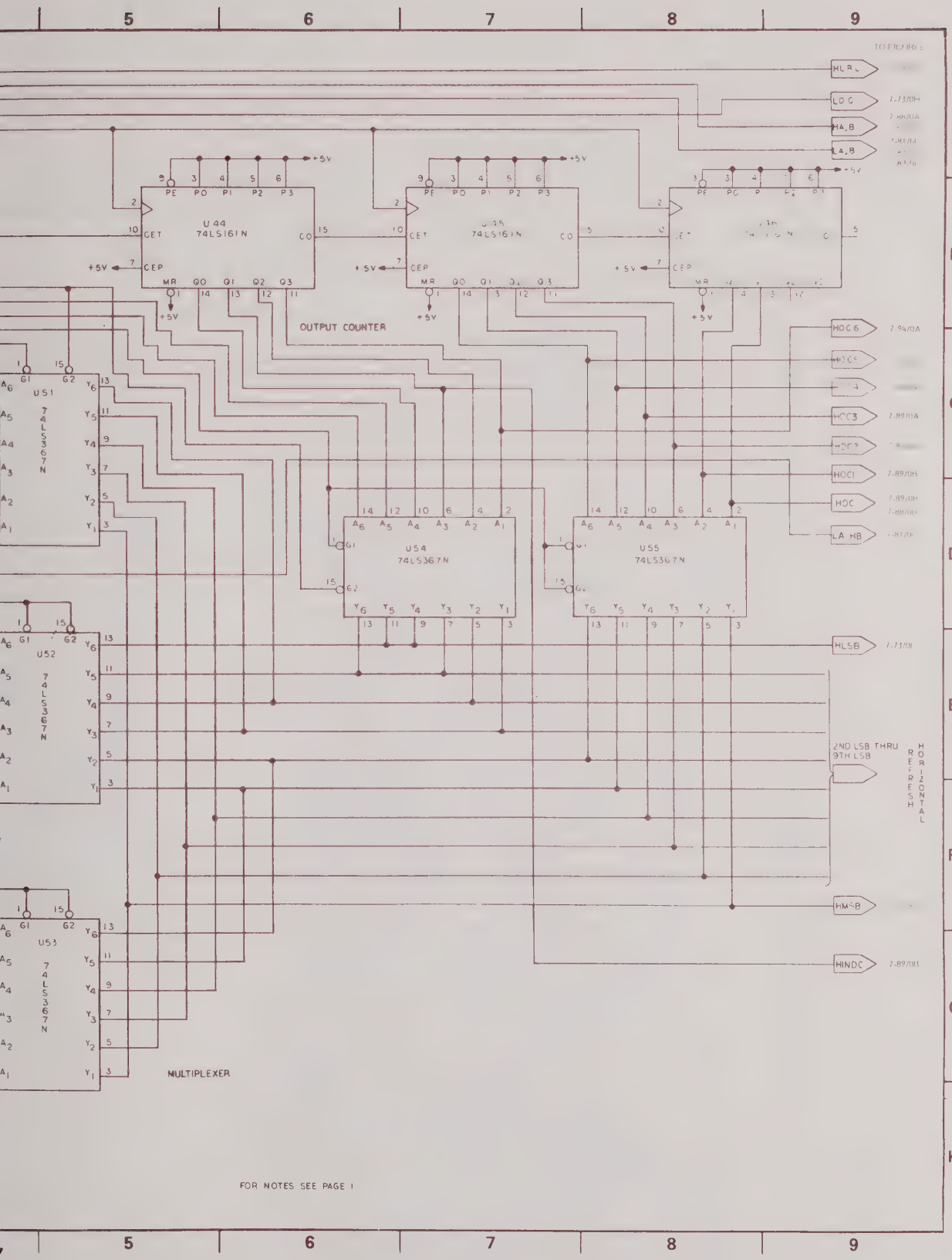


Figure 7-72. Digital (A2) PCB Refresh Address Control Circuits Schematic Diagram

Figure 7-71.

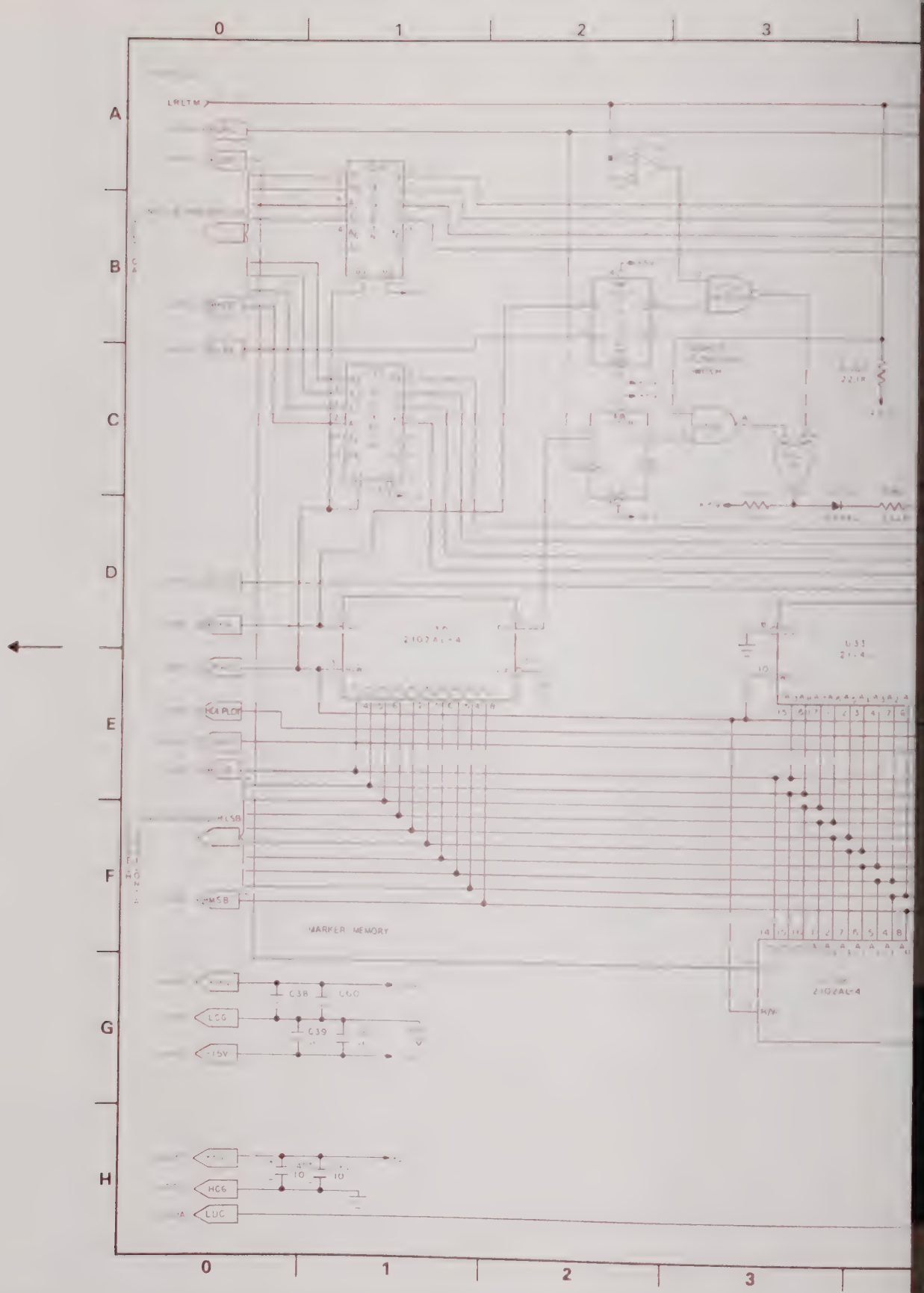
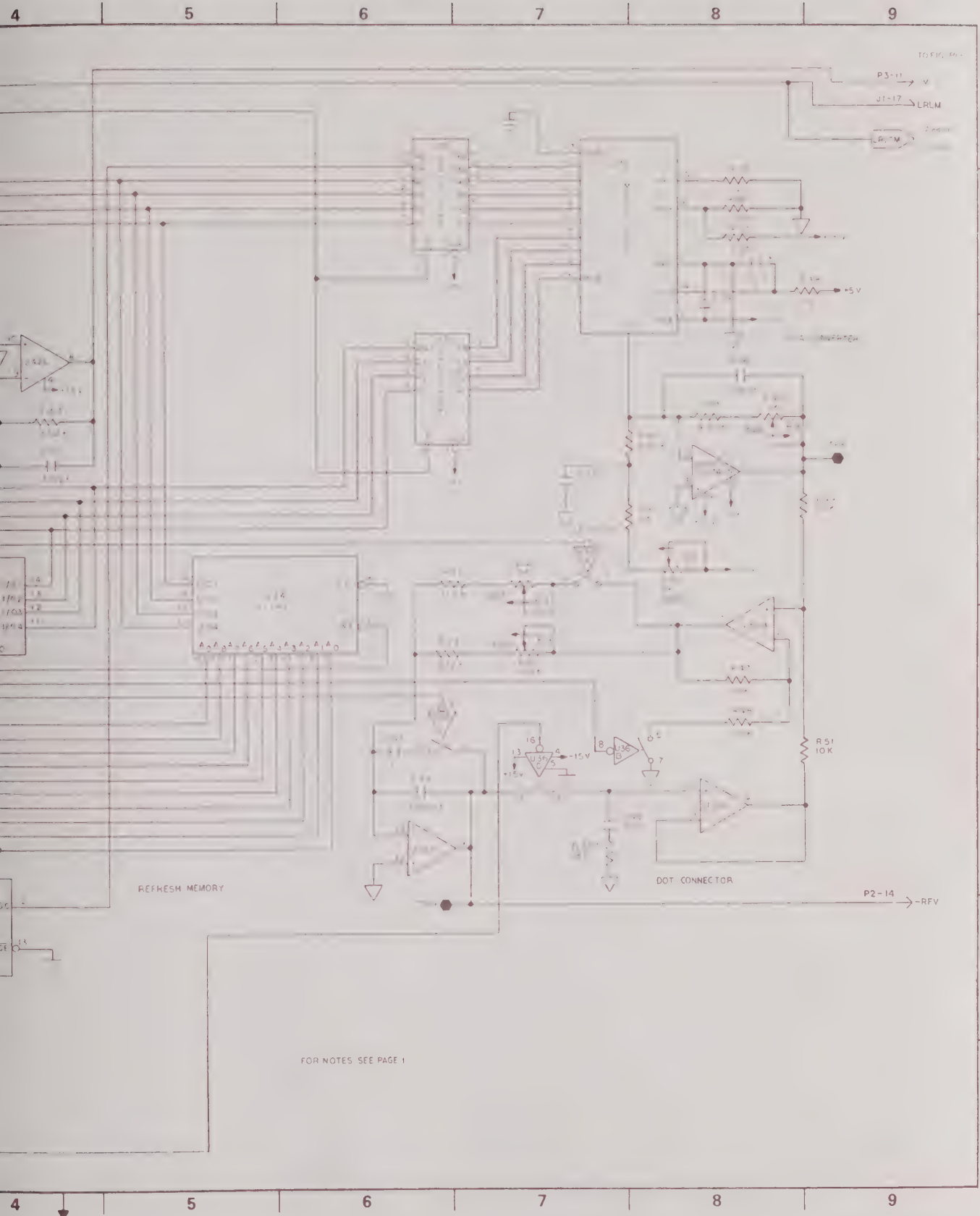
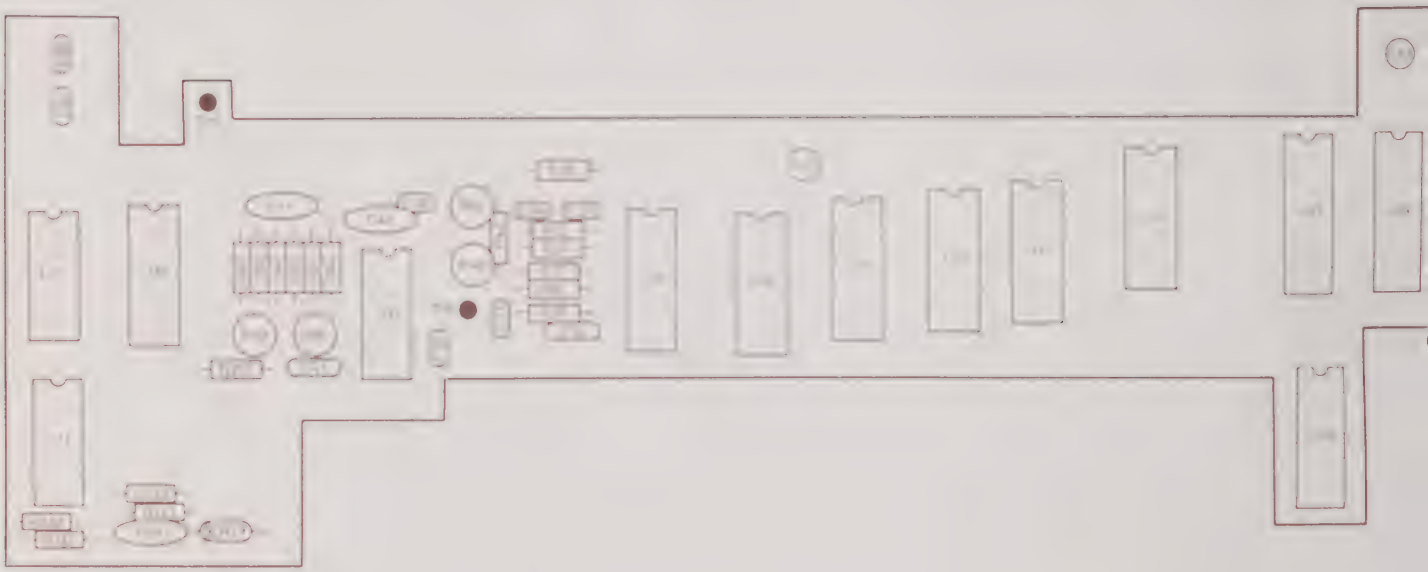


Figure 7-73. Digital (A2) PCB Refresh Vertical Memory, Marker Refresh Memory and Dot Connector D/A Converter Circuits Schematic Diagram


P3-11
V
J1-17
LRLM
+5V
+15V
-15V
R51
10K
REFRESH MEMORY
DOT CONNECTOR
P2-14
-RFV
FOR NOTES SEE PAGE 1



Waveform Conditions

560A Controls:
Channel A – ON
dB PER DIVISION – .5
Channel B – ON
dB PER DIVISION – 1

6647A Controls:
TRIGGER–AUTO
SWEEP TIME–100ms

Oscilloscope Controls.
Vertical V/division – 2
Horizontal Sweep – 2 ms/division
Input – Dc couple
Triggering – Trigger with 560A Channel A signal

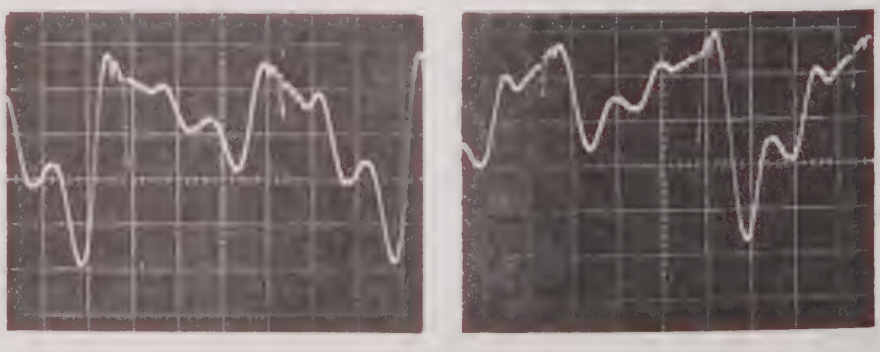


Figure 7-74. Digital (A2) PCB Refresh Vertical Memory, Marker Refres Memory and Dot Connector D/A Converter Circuits Parts Locator Diagram

Figure 7-73.

7-7.8 Refresh Vertical Memory, Marker Refresh Memory, and Dot Connector D/A Converter Circuits

These circuits are described below. The schematic for the circuit is shown in Figure 7-73, and the parts locator diagram is shown in Figure 7-74.

a. Refresh Vertical Memory Circuit. This circuit temporarily stores the digital output of the vertical A/D converter to provide the CRT with a flicker-free display when the REFRESH display mode is selected.

The circuit is composed of 4k RAMs U33, U34, and 1k RAM U106. Inputs to these RAMS are the 10-bit horizontal address word from the Refresh Address Control circuit, and the 9-bit vertical data word from tri-state buffers U28 and U29. These two buffers are in their "off" state except when gated "on" by the LRWE control line from the Refresh Write Enable Control circuit (paragraph 7-7.19). LRWE is gated LOW at the end of a vertical A/D conversion provided that (1) the X-Y PLOT pushbutton is not depressed, (2) the REFRESH HOLD pushbutton is not depressed, and (3) the sweep generator is not providing a retrace blanking pulse.

Except when being written into, refresh memory is continually being scanned (addressed) and the vertical data stored therein being applied to latch circuits U30 and U31 at a 14.3 ms rate. When U30 and U31 are clocked by the HLRL pulse from the Refresh Address Control circuit, the vertical data is applied to D/A converter U32.

b. Marker Refresh Memory Circuit. This circuit synchronizes the output of the marker normalizer circuit for use during the refresh display mode, and it multiplexes between real time (RLTM) and refresh (RFSH) markers for CRT display.

The Marker Refresh Memory circuit consists of 1k RAM U70. Inputs to this RAM are the 10-bit horizontal address word from the Refresh Address Control circuit and the 1-bit vertical data word from the Marker Normalizer circuit. Except when the LRWE control line is LOW and data is being written into the memory, U70 is continuously being read out at a 14.3 ms rate. The output of U70, Pin 12, is applied to the real time/refresh switch circuit.

The real time/refresh switch circuit consists of D flip-flops U71A, U71B, gates U72A, U72B, U72C, and operational amplifier U42C. When the real time display mode is selected, Pin 2 of U72A is enabled and real time markers are gated through U72A and U72B, inverted by U42C, and supplied to the front panel PCB via the -M signal line. When the refresh mode is selected, pin 10 of U72 is enabled and refresh markers are gated as described above.

NOTE

The provisions for writing into the marker memory, and subsequently updating refresh markers, are the same as those specified for the refresh memory; that is, (1) the X-Y PLOT pushbutton is not de depressed, (2) the REFRESH HOLD pushbutton is not depressed, and (3) the sweep generator is not providing a retrace blanking pulse.

c. Dot Connector D/A Converter Circuit. This circuit performs three interdependent functions. These functions and the order in which they occur are given below. The circuit:

1. Converts the refresh vertical data bits into discrete current levels via D/A converter U32 and associated components.

2. Converts the discrete output current levels of U32 into discrete voltage levels (dots) via operational amplifier U35A and associated components.

U35A is adjusted by Gain and Offset potentiometers R40 and R43, respectively, so that its output voltage is normalized to ±10 volts.

3. Connects the output voltage dots of U35A together. The circuitry for connecting the dots together consists of operational amplifiers U35B, U35C, and U35D and their associated components. Connecting the voltage dots together provides the CRT or X-Y plotter with a vertical display that is contiguous rather than separated into dots.

The output of the dot connector circuit, -RFV, goes to the front panel PCB. On the front panel PCB, the -RFV signal is routed through the REFRESH switch and out to the vertical output circuit (paragraph 7-7.10).

7-7.9 Refresh Ramp Generator Circuit

This circuit, in synchronization with the refresh address control circuit's output counter, produces four distinct CRT horizontal sweep voltage ramps: REFRESH, single-channel; REFRESH, dual-channel; X-Y PLOT/REFRESH, single-channel; and X-Y PLOT/REFRESH, dual-channel. (Refer to paragraph 7-7.12 for the discussion on single-channel and dual-channel sweep.) These four output ramps are shown in Figure 7-75. A simplified schematic of the refresh ramp generator

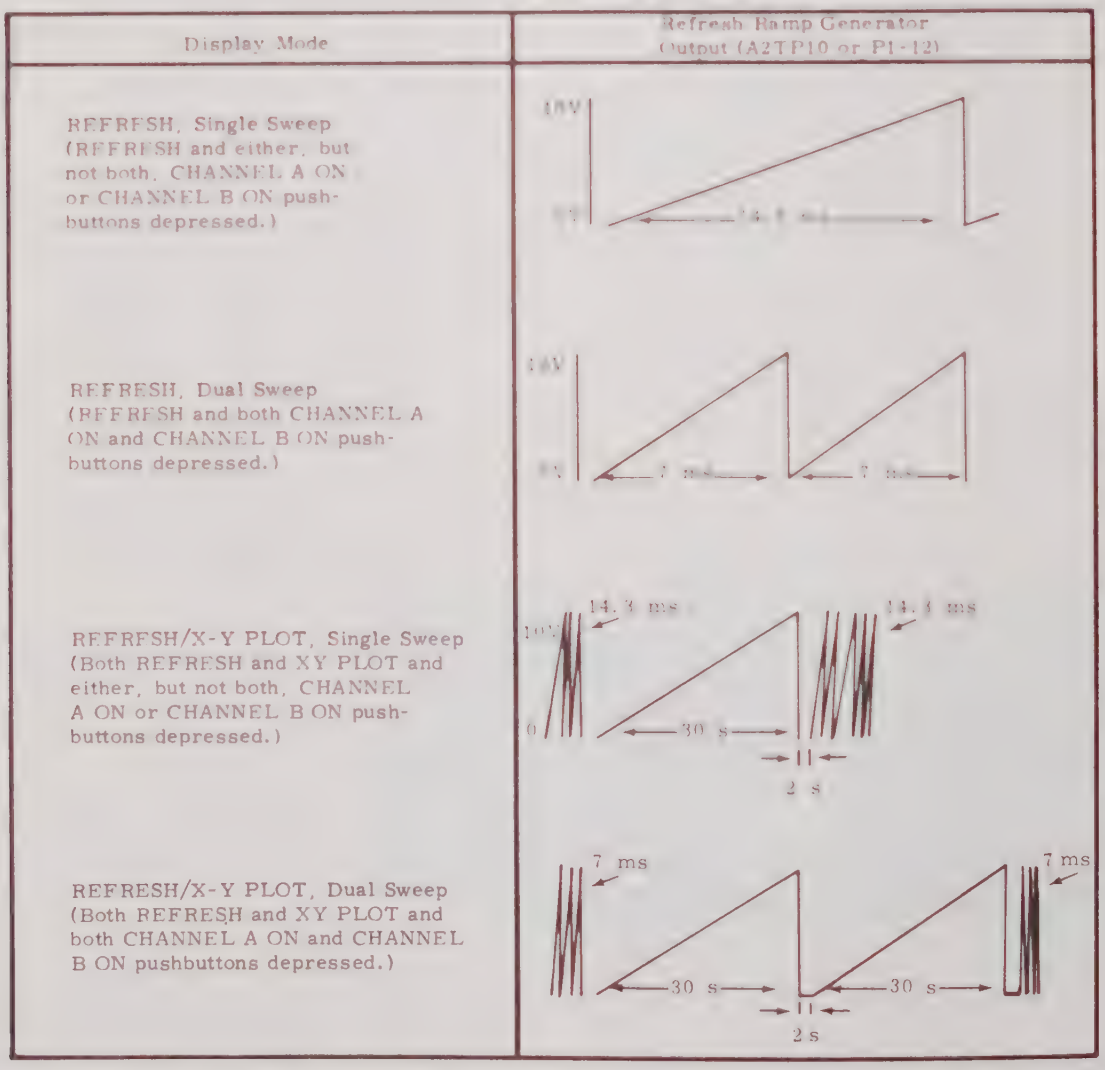

Display Mode
Refresh Ramp Generator Output (A2TP10 or P1-12)
REFRESH, Single Sweep (REFRESH and either, but not both, CHANNEL A ON or CHANNEL B ON push-buttons depressed.)
REFRESH, Dual Sweep (REFRESH and both CHANNEL A ON and CHANNEL B ON push-buttons depressed.)
REFRESH/X-Y PLOT, Single Sweep (Both REFRESH and XY PLOT and either, but not both, CHANNEL A ON or CHANNEL B ON push-buttons depressed.)
REFRESH/X-Y PLOT, Dual Sweep (Both REFRESH and XY PLOT and both CHANNEL A ON and CHANNEL B ON pushbuttons depressed.)
14.3 ms
30 s
2 s
7 ms

Figure 7-75. Refresh Ramp Generator Circuit, Output Ramp Waveforms

is shown in Figure 7-76, a parts locator diagram is shown in Figure 7-79, and the full schematic is shown in Figure 7-80. In the simplified schematic, the component reference designators enclosed in parenthesis relate to the actual circuit components.

The refresh ramp generator (Figure 7-76) uses different combinations of voltage, resistance, and capacitance to develop the four output ramps. In the refresh mode (both single and dual-channel), S3 is open and S2 is closed, placing resistances R1 and R2 in parallel. In the refresh, single-channel mode, S1 is closed, placing -5 volts at point A. In the refresh, dual-channel mode, S1 is open, placing 10 volts at point A. In the X-Y plot/refresh mode (either single or dual-channel), S1 is open, S2 is open, and S3 is closed. This places -10 volts at point A and capacitors C1 and C2 in parallel. When S3 is open, the diode path from C2 to ground maintains a constant 10 volts across C2. This diode path minimizes dielectric absorption problems in C2.

In all four modes (refresh, single-channel; refresh, dual-channel; Y-Y plot/refresh, single-channel; and X-Y plot/refresh, dual-channel), the ramp generator is reset by the LRST control line from the X-Y Plot Control circuits (paragraph 7-7.22). In both single-channel modes, refresh and X-Y plot/refresh, reset occurs between output counter counts 1016 and 1023. In both dual-channel modes, reset occurs between counts 504 and 511 and again between counts 1016 and 1023. The ramp generator output, RFH, is applied to the front panel PCB, and from there via the REFRESH switch to the horizontal/marker summing circuit (Figure 7-80).

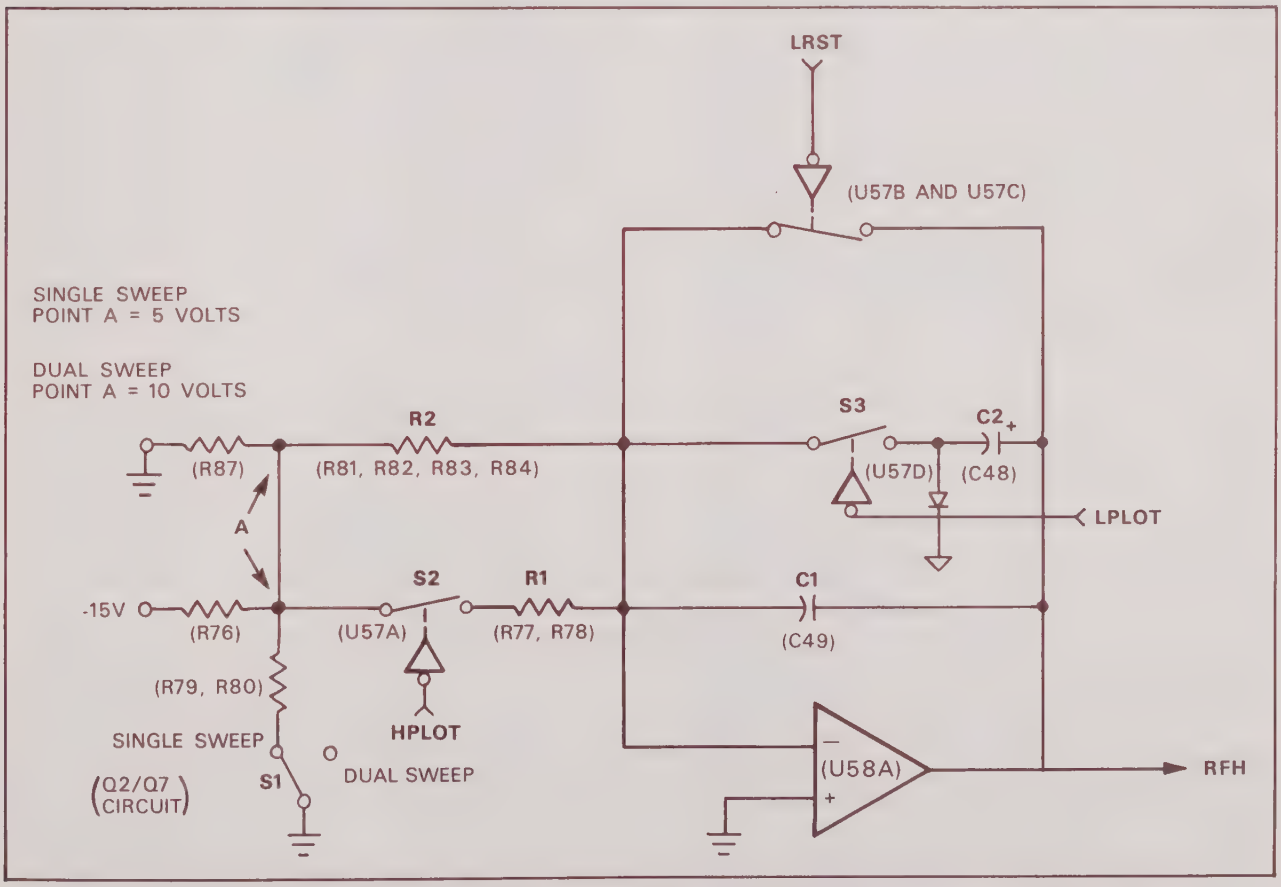


Figure 7-76. Refresh Ramp Generator Circuit, Simplified Schematic Diagram

7-7.10 Vertical Output Circuits

These circuits serve two functions: (1) they sum the vertical output signal, either real time or refresh, with both a reference voltage from the REF POS SET potentiometer and with markers, and (2) they route the vertical output signal to the CRT vertical deflection circuits, GPIB interface (A6) PCB, and rear panel VERTICAL OUTPUT connector. The vertical output circuits, which are located on both the A1 and the A2 PCBs, are described using the block diagram in Figure 7-77. This block diagram indicates the figure number of the schematic where the circuits are diagrammed. To correlate between the blocks on the block diagram and the circuits on the schematic, use the mnemonic symbols; these symbols, which identify control lines, point to the circuits. A parts locator diagram for the Vertical Output circuits is presented in Figure 7-79.

As shown in Figure 7-77, the real time vertical (RTV) and refresh vertical (RFV) signals come together at the front panel REFRESH switch, where one of them is selected for output processing. The selected vertical signal is applied to both A and B REF POS LOCATE switches. If the A and B REF POS LOCATE switches are in their normal (non-depressed) position, the vertical signal applied to each is routed to the A2 PCB where it is summed with a voltage from the respective A or B SET potentiometer. This summing action produces a vertical signal whose positive and negative excursions are referenced to the voltage from the SET potentiometer. The outputs of the two summing circuits are applied to FET switches U59C and U59D, where channel selection is accomplished. U59C and U59D are controlled by the LCA and HCA control lines, respectively, from multiplexer U80.

When LCA is LOW, Channel A is selected; conversely, when HCA is LOW, Channel B is selected. From the junction of U59C and U59D, the vertical output signal is routed to

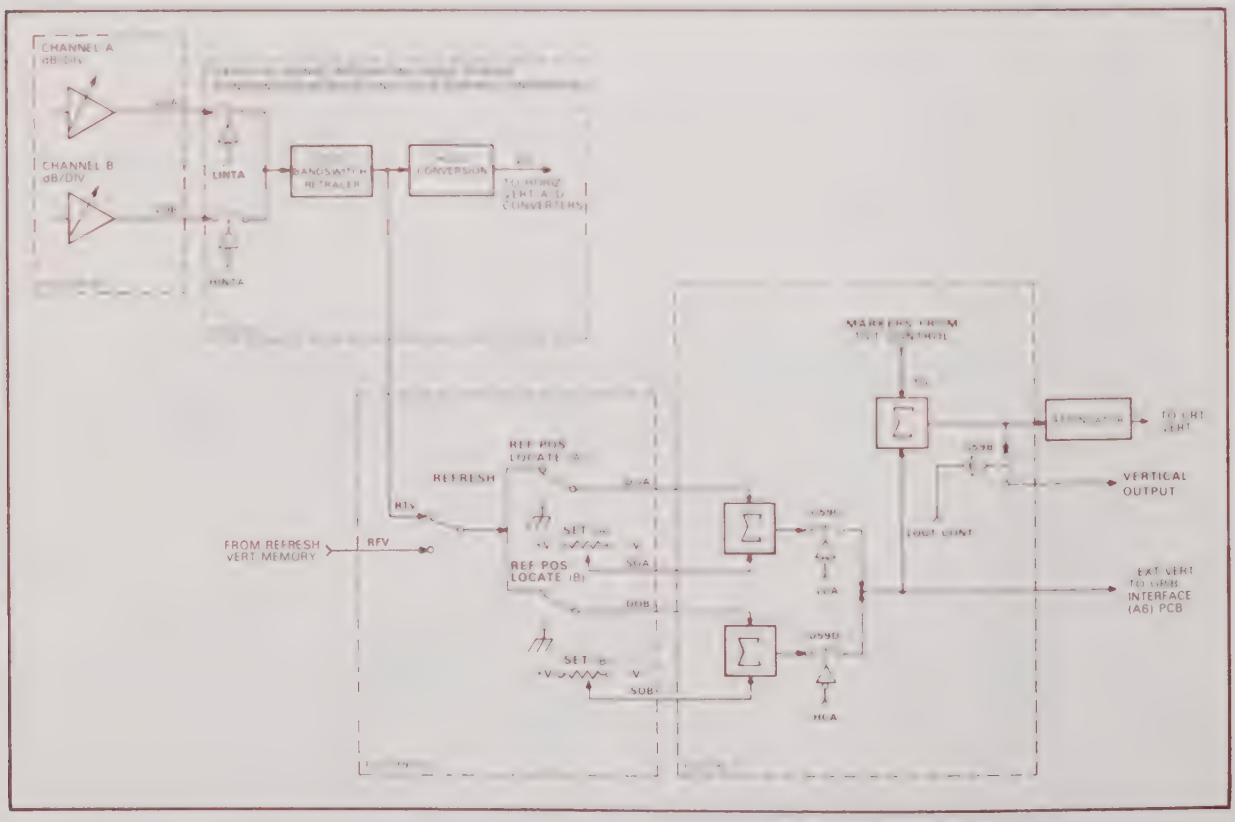


Figure 7-77. Vertical Output Circuits, Block Diagram

another summing circuit where it is summed with markers. The output of this second summing circuit is applied via an attenuator to the CRT vertical deflection circuits and via FET switch U59B to the rear panel VERTICAL OUTPUT connector. U59B is controlled by the LOUT CONT line from the X-Y Plot Control circuits (paragraph 7-7.22). When the rear panel OUTPUT MODE switch is in the CRT position, the vertical output signal is continually applied to the VERTICAL OUTPUT connector. When the OUTPUT MODE switch is in the RCDR position, the vertical output signal is applied to the VERTICAL OUTPUT connector only during an X-Y plotting operation. The third output from this circuitry is -EXT VERT, which goes to the A6 PCB.

7-7.11 Marker Input, Marker Output, and Seq Sync Normalizer Circuits

These circuits are shown in the block diagram of Figure 7-78. This block diagram indicates the figure number where the actual circuits are diagrammed. The circuit descriptions given below are referenced to the block diagram. Use the mnemonic symbols to correlate between the block diagram and the schematic. The mnemonic symbols indicating control and signal lines point to circuit components. A parts locator diagram for these circuits is presented in Figure 7-79.

a. Marker Input Circuit. The marker input, or normalizer, circuit performs the following functions:

- Buffers (x 1 gain) or amplifies (x 10 gain) input markers that are less than +0.7 volts or greater than -0.7 volts.
- Provides front panel threshold control for input markers.
- Changes markers which have both positive- and negative-going alternations into all positive-going markers.
- Filters the markers.
- Translates the markers into sharply-defined TTL voltage levels.
- Provides an OR function that enables markers to be input to the 560A on either of two rear panel connectors: MARKER INPUT or Z AXIS INPUT.

b. Marker Output Circuit. This circuit (1) selects between real time or refresh markers, (2) provides on/off control for markers, and (3) routes markers to the vertical/marker summing circuit and, via the front panel TILT control, to the horizontal/marker summing circuit. The vertical/marker summing circuit sums markers with the vertical data and applies the resulting signal to the CRT vertical deflection circuit. The horizontal/marker summing circuit sums the +T and -T voltages from the TILT control with the horizontal signal to provide up to ± 45 degrees of marker tilt. The output of the horizontal/marker summing circuit is applied, via an attenuator, to the CRT horizontal deflection circuit and, via U59A, to the rear panel HORIZONTAL OUTPUT connector. U59A is controlled by the LOUT CONT line from the X-Y Plot Control circuits (paragraph 7-7.22). When the rear panel OUTPUT MODE switch is in the CRT position, the horizontal output signal is continually applied to the HORIZONTAL OUTPUT connector. When the OUTPUT MODE switch is in the RCDR position, the horizontal output signal is applied to the HORIZONTAL OUTPUT connector only during an X-Y plotting operation.

c. Seq Sync Normalizer Circuit. This circuit provides accommodation for two different types of sweep generators--those that use a composite bandswitch blanking and marker output circuit (e.g., the HP 8620) and those that use a separate bandswitch blanking output circuit (e.g., the WILTRON 6600A. The markers and bandswitch blanking pulses from the composite blanking and marker-type sweep generator, after buffering, are each processed through a different signal path. The markers are inverted, translated to a TTL level, and routed via the OR gate to the marker output circuit. The bandswitch blanking pulses, whether stripped from the composite signal or provided by the separate blanking-type generator,

are translated to a TTL level and then

1. applied to the hold-during-bandswitch/retrace circuit (paragraph 7-7.2),

and

2. inverted and applied to multiplexer A2U80 (Figure 7-88).

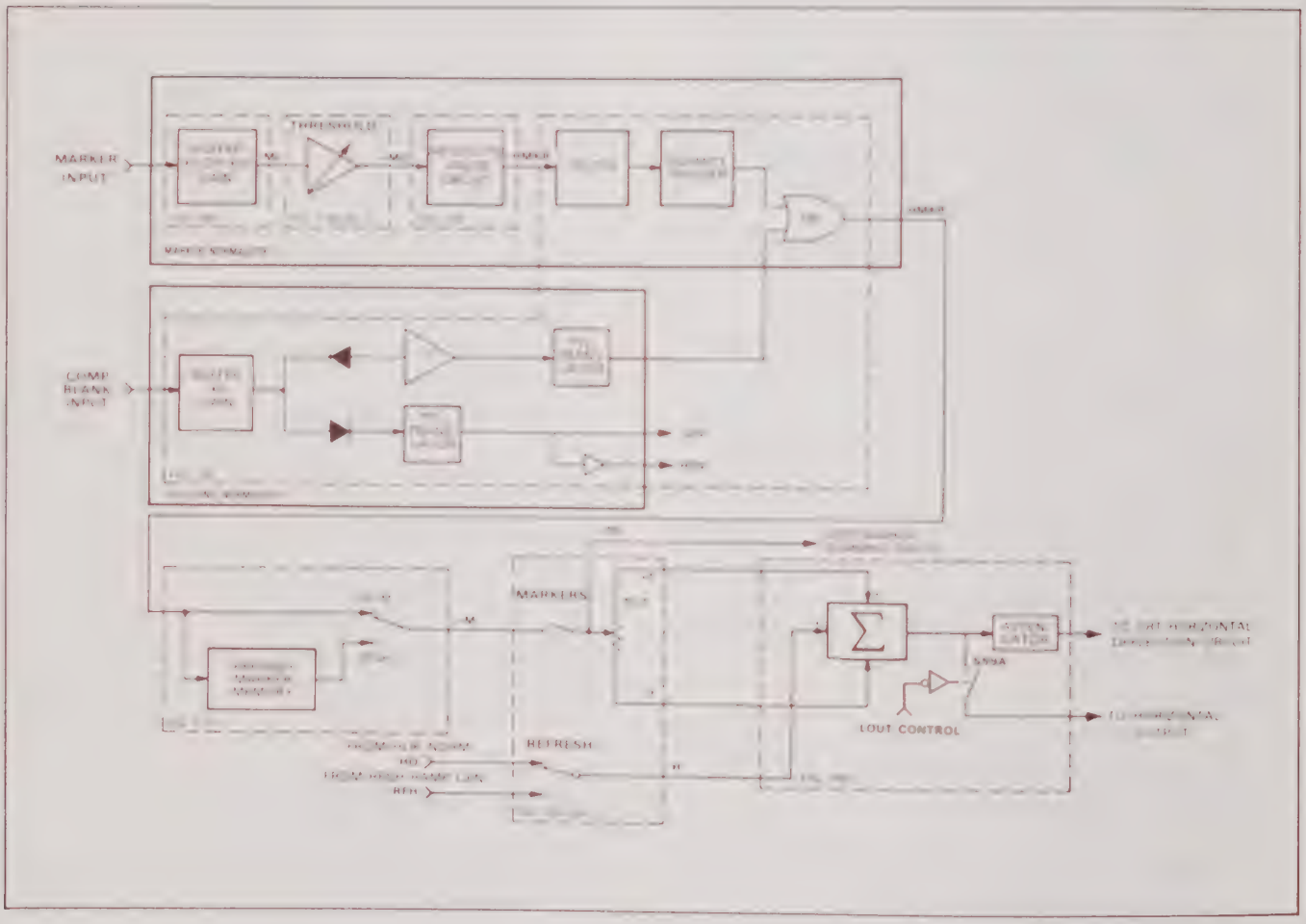
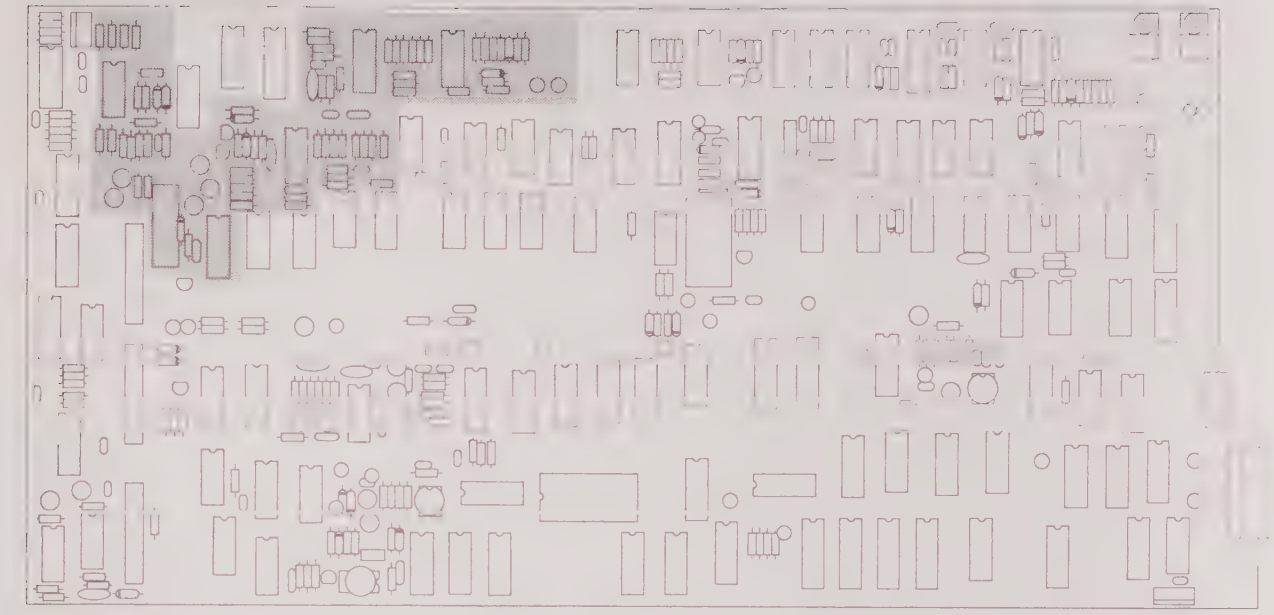
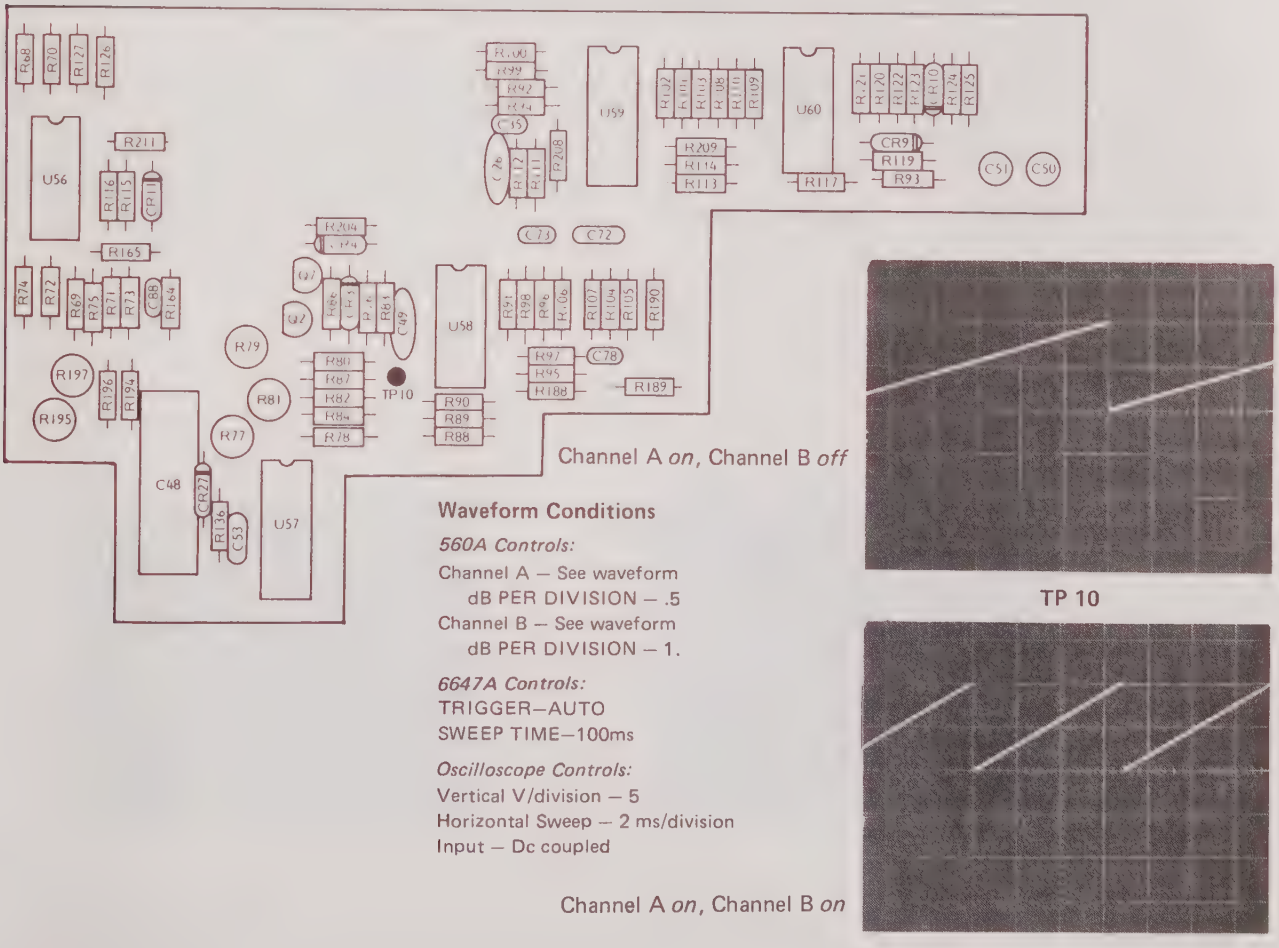


Figure 7-78. Marker Input, Marker Output, and Seq Sync Normalizer Circuits, Block Diagram





Channel A *on*, Channel B *off*

Waveform Conditions

560A Controls:

Channel A — See waveform
dB PER DIVISION — .5
Channel B — See waveform
dB PER DIVISION — 1.

6647A Controls:

TRIGGER—AUTO
SWEEP TIME—100ms

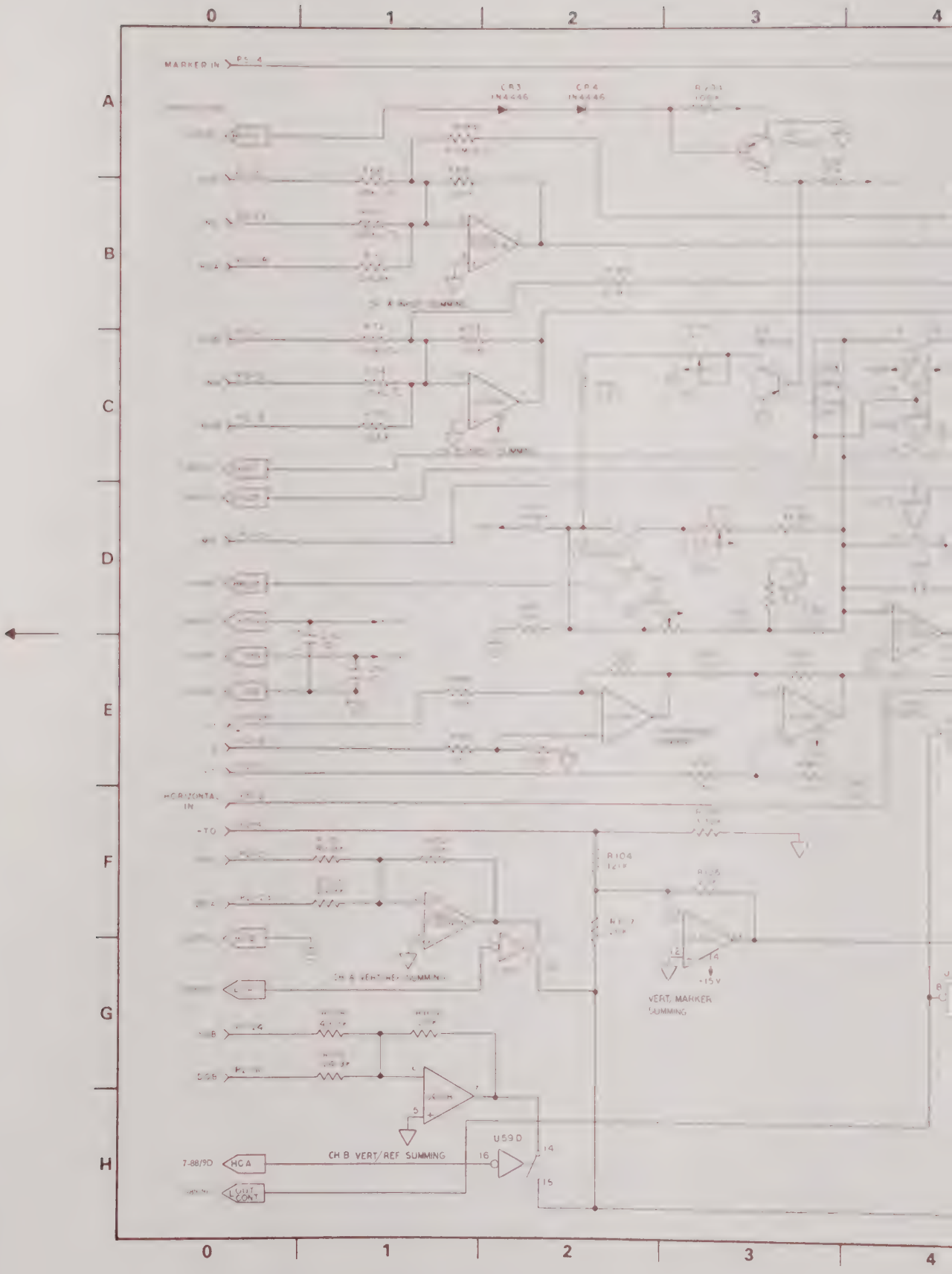
Oscilloscope Controls:

Vertical V/division — 5
Horizontal Sweep — 2 ms/division
Input — Dc coupled

TP 10

Channel A *on*, Channel B *on*

Figure 7-79. Digital (A2) PCB Refresh Ramp Generator; Vertical Output; and Marker Input, Marker Output, etc. Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
MARKER IN
CR3
1N4446
CR4
1N4446
HORIZONTAL IN
-TO
R104
VERT. MARKER SUMMING
-15 V
CH B VERT/REF SUMMING
U59D
7-88/9D
HCA
LOUT CONT
14
15
16

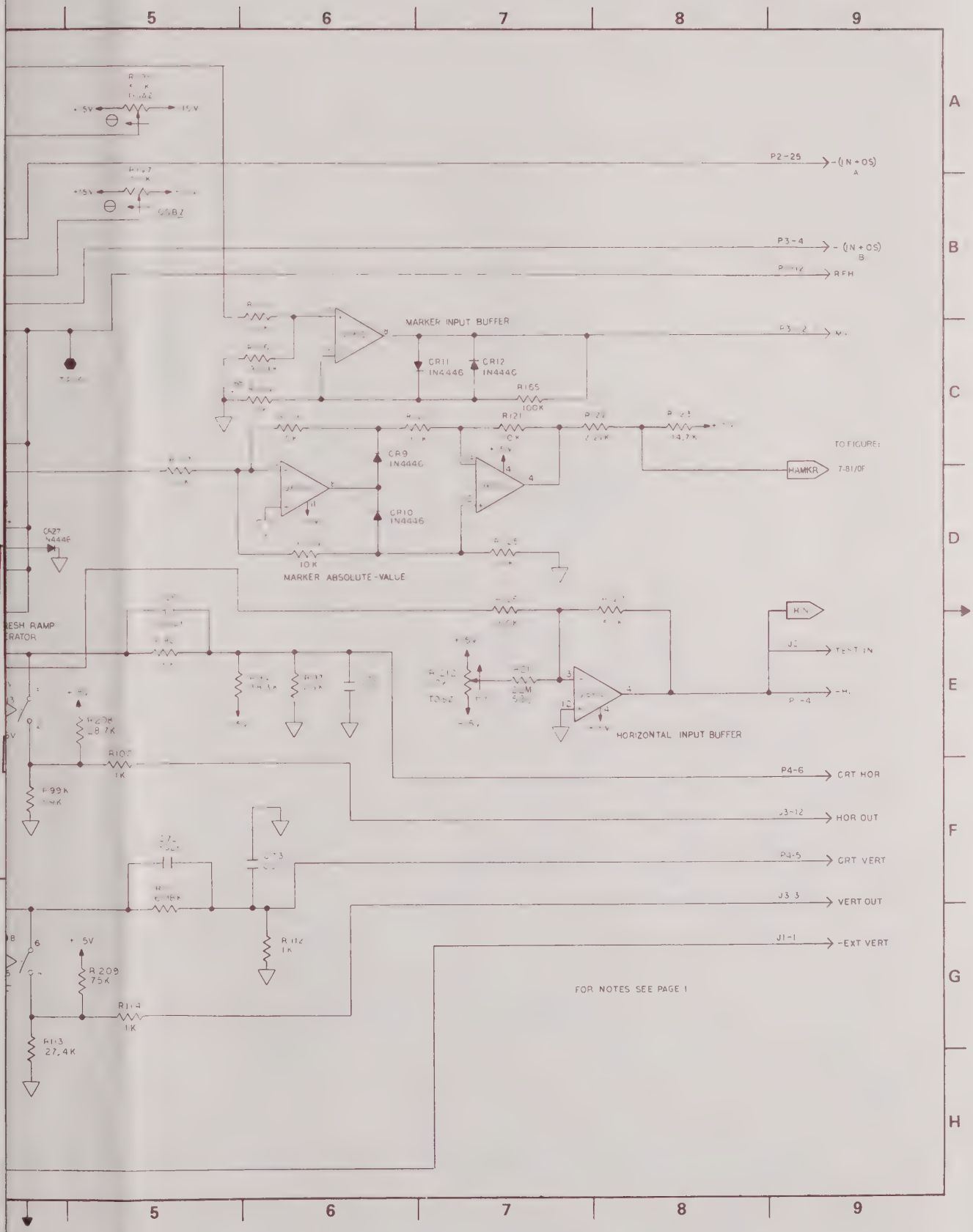


Figure 7-80. Digital (A2) PCB Refresh Ramp Generator; Vertical Output; and Marker Input, Marker Output, etc. Schematic Diagram

Figure 7-79.

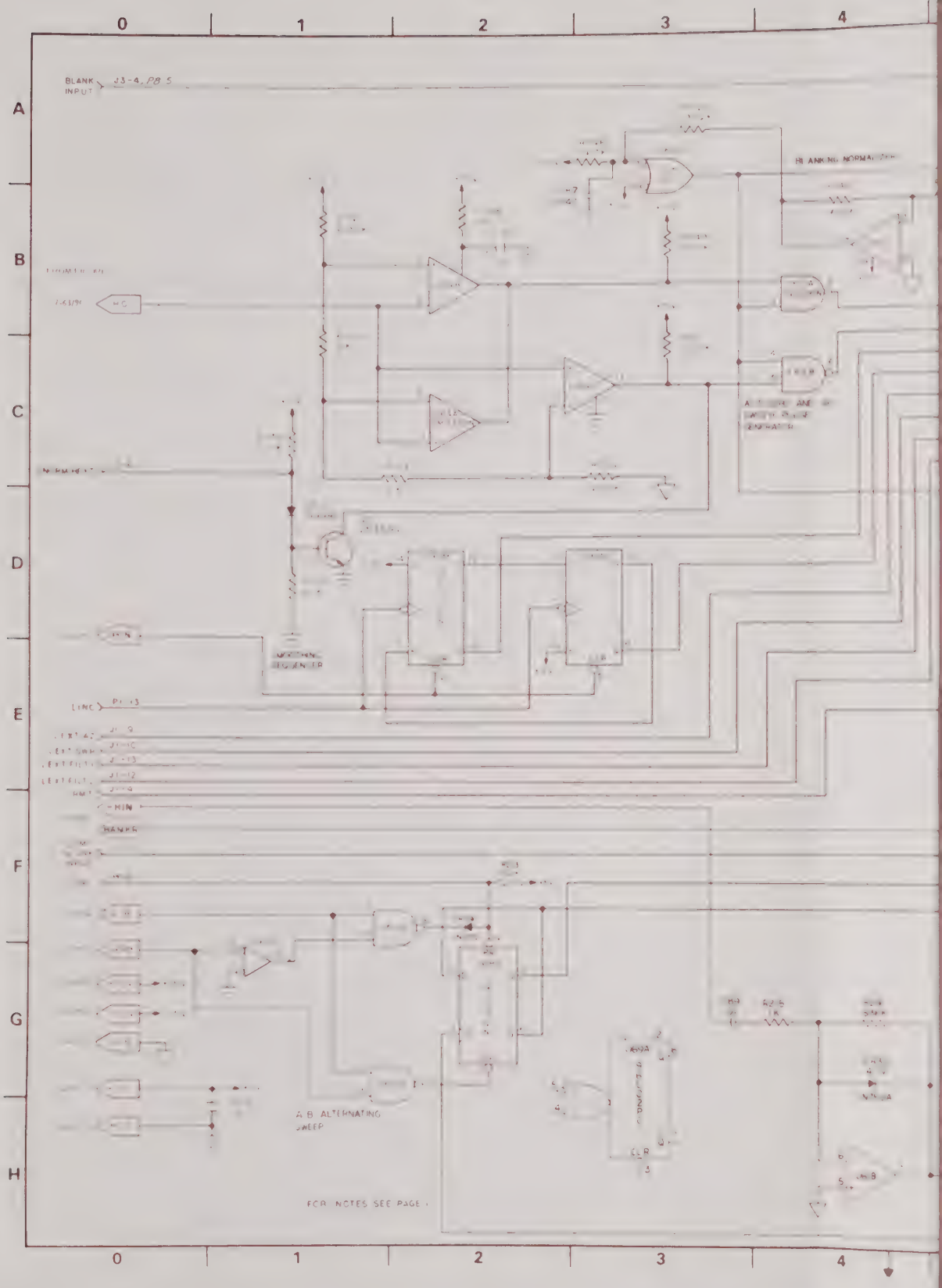
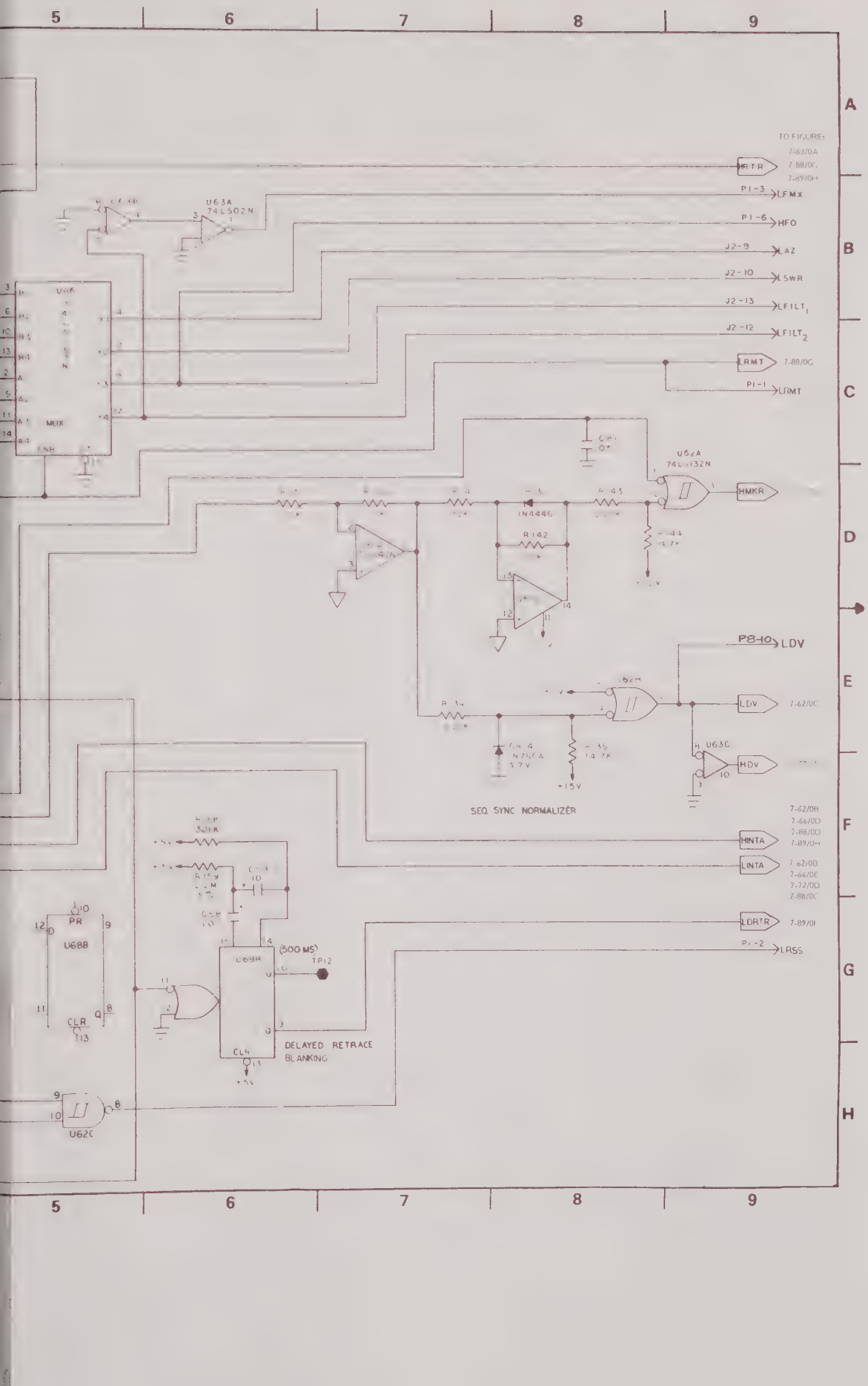
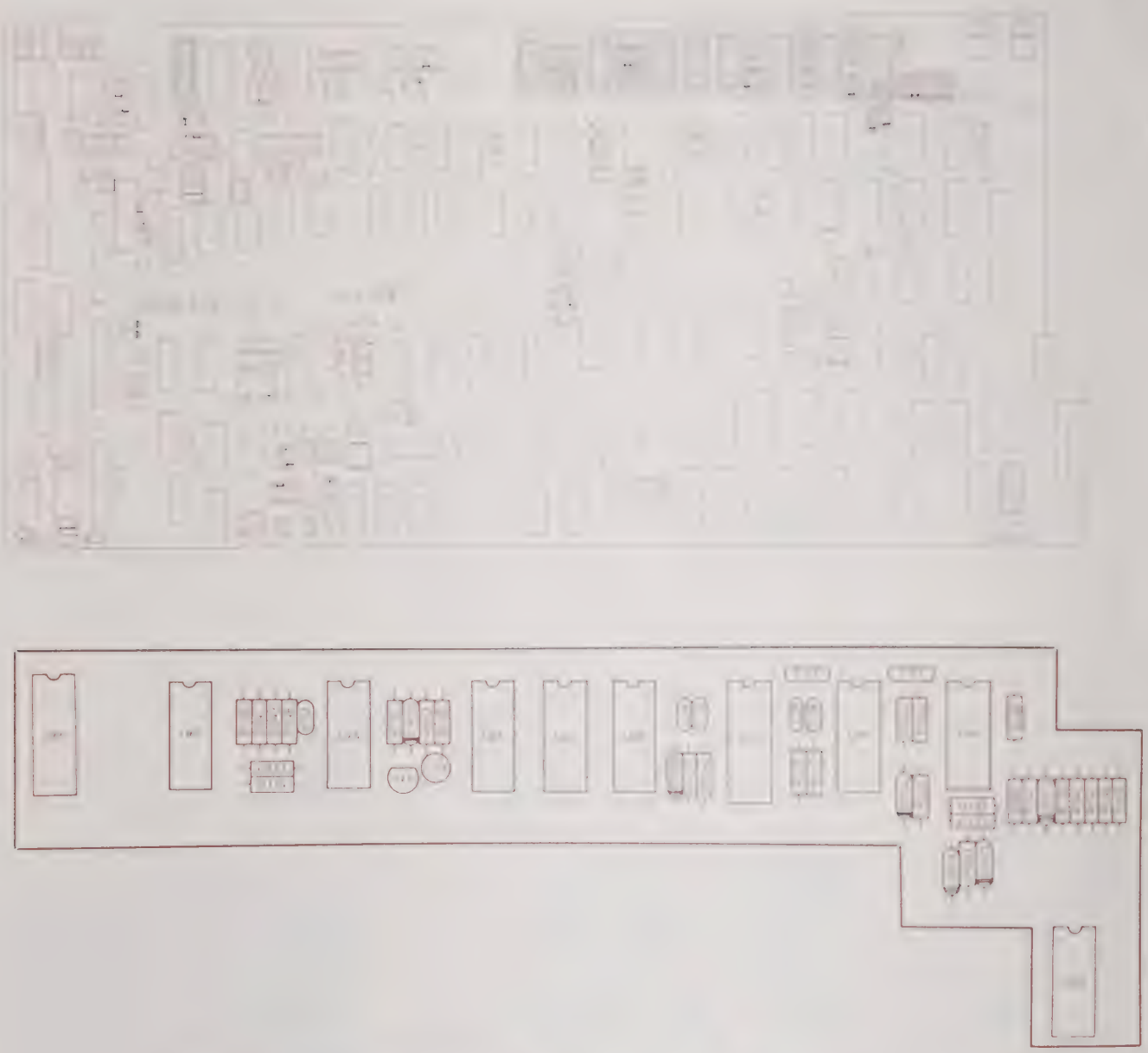
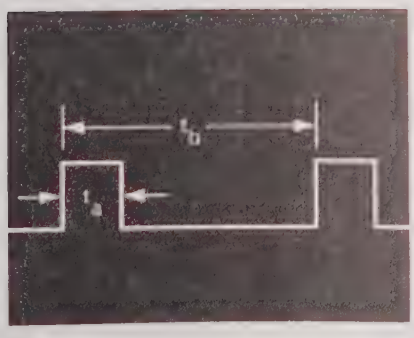


Figure 7-81. Digital (A2) PCB Channel A/B Alternating Sweep; Smoothing Sequencer etc.; Blanking Normalizer; Reduce Sweep Speed; and Log Amplifier Autozeroing etc. Circuits Schematic Diagram


5
6
7
8
9
A
B
C
D
E
F
G
H
TO FIGURE:
7-63/0A
7-88/0C
7-89/0H
MRTR
P1-3
LFMx
U63A
74LS02N
P1-6
HFO
J2-9
AZ
J2-10
SWR
J2-13
LFILT1
J2-12
LFILT2
LRMT
7-88/0G
P1-1
LRMT
U66
MUX
U62A
74LS132N
HMKR
IN4446
R142
P8-10
LDV
LDV
7-62/0C
HDV
U63C
+15V
SEQ SYNC NORMALIZER
7-62/0H
7-66/0D
7-88/0D
7-89/0H
HINTA
LINTA
7-62/0B
7-66/0E
7-72/0D
7-88/0C
LDRTR
7-89/0F
P1-2
LRSS
U68B
PR
CLR
U69A
(500 MS)
TP12
DELAYED RETRACE
BLANKING
U62C

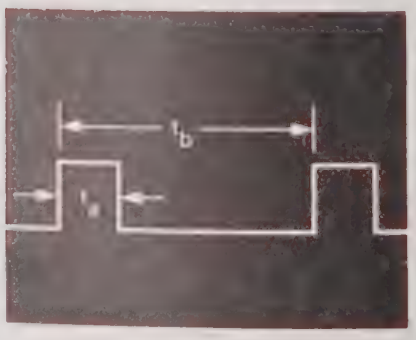


t_a = 54-62ms
t_b = Sweep Generator Sweep Time



TP 11

t_a = 200ms
t_b = Sweep Generator Sweep Time



TP 12

Figure 7-82. Digital (A2) PCB Channel A/B Alternating Sweep; Smoothing Sequencer etc.; Blanking Normalizer; Reduce Sweep Speed; and Log Amplifier Autozeroing etc. Circuits Parts Locator Diagram

Figure 7-81.

7-7.12 Channel A/B Alternating Sweep Circuit

This circuit reads the front panel CHANNEL A ON and B ON switches and generates control signals that indicate either the single or dual-channel mode. It also can read an alternate sweep control signal from the rear panel AUX I/O connector. The single-channel mode has been selected when either, but not both, the CHANNEL A ON or B ON switch is depressed. In this mode, the input signals applied to the selected channel's front panel connector (A or B) are applied to the Log Amplifier (A3) PCB, Front Panel/Digital (A1/A2) PCB, and CRT Mainframe circuits. The dual-channel mode has been selected when both CHANNEL A ON and B ON switches are depressed. In this mode, the input signals applied to both front panel connectors (A and B) are alternately applied to the A3 PCB, A1/A2 PCB, and CRT Mainframe circuits (see the parts locator diagram, Figure 7-82.) This circuit is split between two circuit boards, A1 and A2. Refer to the simplified schematic (Figure 7-83) while reading the following circuit description.

If only the CHANNEL A ON switch is on, U65C applies an enabling LOW to the preset (PR) input of U68A. The PR input, when enabled, prevents U68A from changing states, and sets the HINTA (U68A-Q) output line HIGH.

If only the CHANNEL B ON switch is on, U65D applies an enabling LOW to the clear (CLR) input of U68A. The CLR input, when enabled, prevents U68A from changing states, and sets the LINTA (U68A-$\overline{Q}$) output line HIGH.

If both switches are on, U65C and U65D apply an inhibiting HIGH to the PR and the CLR inputs, respectively, of U68A. The PR and CLR inputs, when inhibited, allow the rising edge of the retrace blanking pulse from the Blanking Normalizer circuit (paragraph 7-7.14) to clock U68A. When clocked, the U68A-Q and -$\overline{Q}$ output lines (HINTA and LINTA, respectively) alternately change logic states at the end of each forward sweep. Channel A signals are processed and displayed during one forward sweep; Channel B signals are processed and displayed during the next forward sweep.

In the alternate sweep mode, the alternate sweep line, ALT1/SYNC, from the AUX I/O connector is applied to the preset input (PR) of U68A. When it is low, U68A resets LOW its Q output (HINTA), which causes the Channel B input to be processed and displayed. When the line is HIGH, U68A sets HIGH its Q output (HINTA), which causes Channel A to be processed and displayed. Refer to paragraph 7-7.21 for a further explanation of the alternate sweep mode.

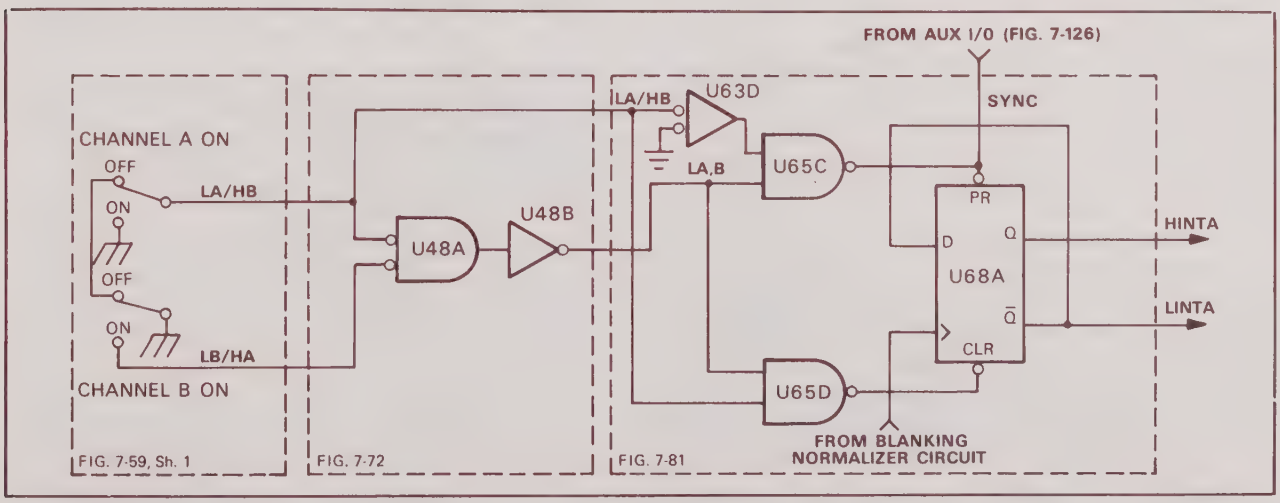


Figure 7-83. A, B Alternating Sweep Circuit, Simplified Schematic Diagram

7-7.13 Smoothing Sequencer, Smoothing Local/Remote Multiplexer, and Smoothing Indicator LED Circuits

This group of circuits is described below. A parts locator diagram for circuits is shown in Figure 7-82, and a simplified schematic is shown in Figure 7-84. The circuit is split between the A1 and A2 PCBs; the simplified schematic indicates where individual circuits are diagrammed.

a. Smoothing Sequencer Circuit. This circuit sets the SMOOTHING control to the OFF position each time power is applied to the 560A and allows a single momentary-type switch to control between the three SMOOTHING levels: OFF, MIN, and MAX. The circuit consists of the front panel SMOOTHING switch, contact-debounce circuit U5C-U5D, and flip-flops U67A, U67B. The circuit has three distinct output states: (1) U67A-$\overline{Q}$ HIGH, U67B-$\overline{Q}$ HIGH; (2) U67A-$\overline{Q}$ LOW, U67B-$\overline{Q}$ HIGH, and (3) U67A-$\overline{Q}$ LOW, U67B-$\overline{Q}$ LOW. When the 560A is turned on, the smoothing sequencer circuit comes up in state 1. Thereafter, each time the SMOOTHING switch is depressed the circuit sequences to its next state, i.e., from state 1 to state 2, from state 2 to state 3, and from state 3 back to state 1.

b. Smoothing Local/Remote Multiplexer Circuit. This circuit gates either the front panel-generated or the GPIB controller-generated smoothing commands onto a single pair of output control lines. The circuit consists of the A3-B3, A4-B4 inputs and the Y3, Y4 outputs of multiplexer U66. When the 560A is being operated from the front panel, the U66 B3 and B4 inputs are gated to their respective Y3 and Y4 outputs. Conversely, when the 560A is being operated on the bus, the U66 A3 and A4 inputs are gated to the Y3 and Y4 outputs.

c. Smoothing Indicator LED Circuit. This circuit indicates which level of smoothing (OFF, MIN, or MAX) has been selected. Indicators light in either the local (front panel) or remote (GPIB) modes of operation. The circuit consists of inverters U63A, U63B, U5A, NAND gate U5B, and the three indicator LEDs. When LFILT 1 and LFILT 2 output lines are HIGH, the OFF indicator is lit. When LFILT 1 is LOW and LFILT 2 is HIGH, the MIN indicator is lit, and when LFILT 1 and LFILT 2 are LOW, the MAX indicator is lit.

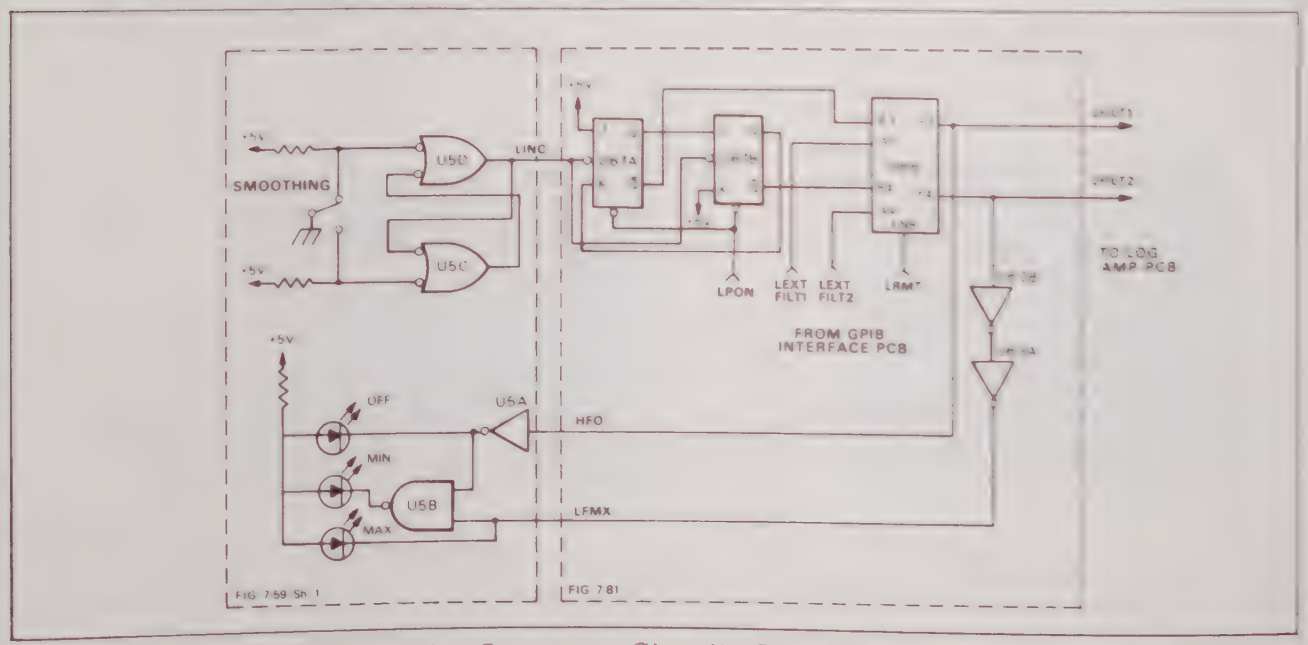


Figure 7-84. Smoothing Sequencer Circuit, Simplified Schematic Diagram

7-7.14 Blanking Normalizer Circuit

This circuit translates the positive-going retrace blanking pulse from the sweep generator into a positive-going, sharply-defined TTL logic level pulse. The circuit schematic is shown in Figure 7-81, and the parts locator diagram is shown in Figure 7-82. The circuit consists of buffer-inverter operational amplifier U61C, Schmitt trigger U62D, and associated components.

7-7.15 Reduce Sweep Speed Circuit

This circuit operates the LRSS control line to light the front panel UNCAL REDUCE SWEEP SPEED indicator. The circuit schematic is shown in Figure 7-81, and the parts locator diagram is shown in Figure 7-82. The circuit consists of one-shot multivibrator U69A, latch U68B, and associated components. The circuit output, LRSS, is LOW when the sweep generator frequency sweep is occurring faster than the 560A digital circuits can process the data.

7-7.16 Log Amplifier Autozeroing Pulse Generator, Log Amplifier Reference-Switch Pulse Generator, and Local/Remote Multiplexer Circuits

These circuits are described below. The schematic for these circuits is shown in Figure 7-81, and the parts locator diagram is shown in Figure 7-82.

a. Log Amplifier Autozeroing Pulse Generator and Log Amplifier Reference-Switch Pulse Generator Circuits. These two circuits operate together to produce the log amplifier autozeroing (LAZ) pulse and the log amplifier reference-switch (LSWR) pulse. (Refer to the circuit description for the log amplifier, paragraph 7-6, for a discussion of these two pulses.)

The autozeroing circuit consists of comparator U64B, NAND gate U65A, and associated components. The reference switch circuit consists of comparators U64A, U64C, NAND gate U65B, transistor Q3, and associated components.

The comparators used in these two circuits compare the horizontal ramp voltage, HO, with a voltage that has been applied to either their + or their - input. U64B has +8V applied to its + input; U64A and U64C have +6V and +4V, respectively, applied to their - input. A timing diagram that relates the pulse outputs from these two circuits to the input horizontal ramp voltage is shown in Figure 7-85. It is important to note that the timing of the LAZ and LSWR pulses is directly proportional to the timing of the sweep ramp. That is, the LSWR pulse starts coincident with the start of sweep retrace and the LAZ pulse starts some time later, depending upon the length (time) of the retrace.

An additional function of the reference switch circuit is to inhibit the generation of a reference switch pulse when the rear panel LOW LEVEL CAL switch is in the EXT position. When the LOW LEVEL CAL switch is in the EXT position, the LNORM/HEXT control line is HIGH. This HIGH logic state causes Q3 to become saturated, which inhibits U65B and places the output of U64 at ground potential.

b. LAZ-LSWR Local/Remote Multiplexer Circuit. This circuit gates either the locally-generated or the GPIB controller-generated LAZ and LSWR pulses onto a single pair of output control lines. The circuit consists of the A1-B1, A2-B2 inputs and the Y1, Y2 outputs of multiplexer U66. When the 560A is being operated locally using front panel controls, the B1 and B2 inputs are gated to their respective Y1 and Y2 outputs. When the 560A is being operated remotely under GPIB control, the A1 and A2 inputs are gated to the Y1 and Y2 outputs.

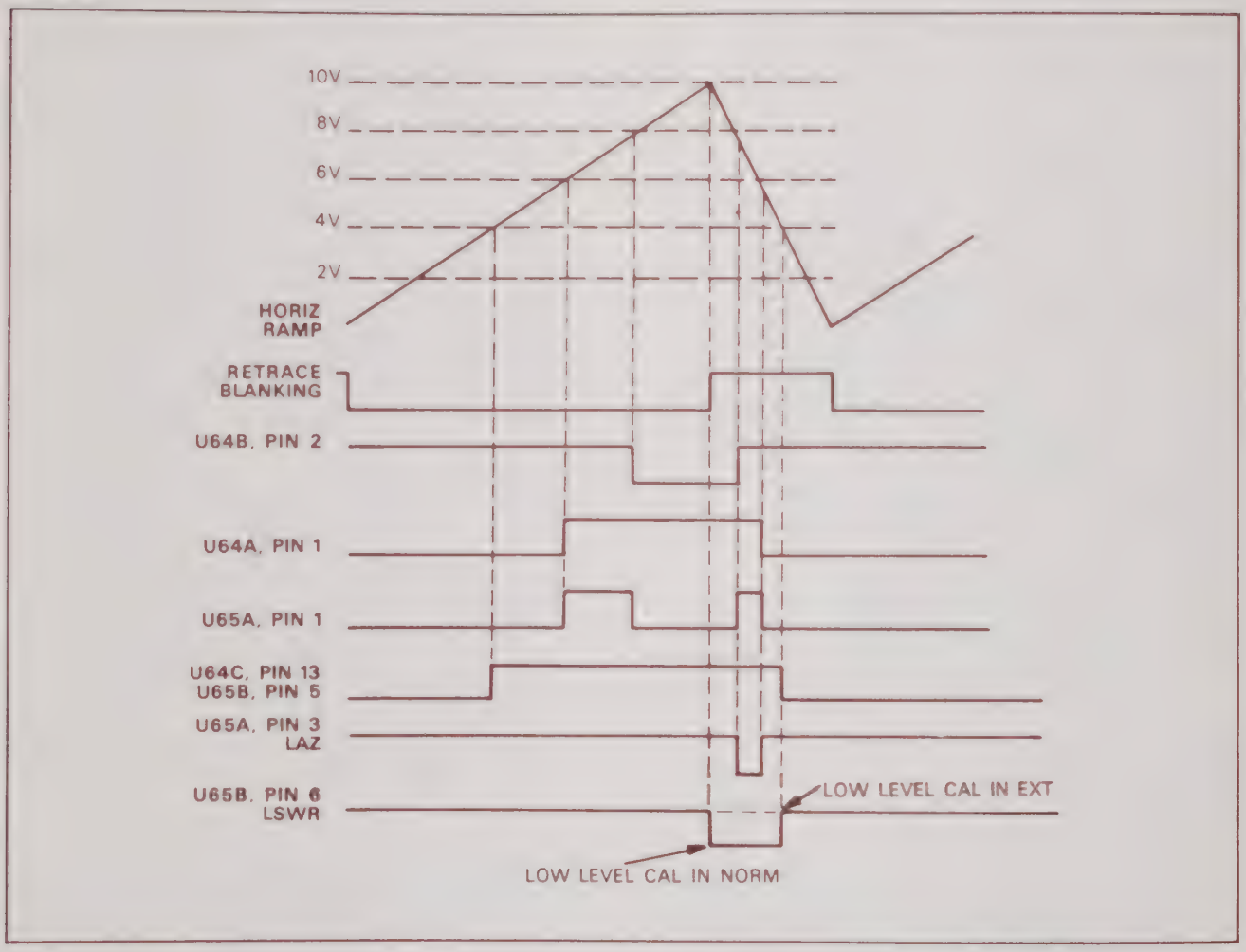


Figure 7-85. LAZ and LSWR Timing Diagram

7-7.17 System and Output Counter Clock Circuit

This circuit generates three clock frequencies: (1) a 1 MHz frequency that provides both the system clock and the output counter clock when the 560A is in the refresh display mode, (2) a 488.3 Hz (1 MHz/2048) frequency that provides the output counter clock when the 560A is in the X-Y plot/refresh, single-channel display mode (paragraph 7-7.12), and (3) a 244.1 Hz (1 MHz/4096) frequency that provides the output counter clock when the 560A is in the X-Y plot/refresh, dual-channel display mode. A parts locator diagram for this circuit is shown in Figure 7-87, and the schematic is shown in Figure 7-88. The circuit is composed of transistor Q4 and its associated components (a modified Colpitts oscillator), 14-stage counter U75, and gates U76A, U77A, U77B, and U77C.

Counter U75 is clocked by the 1 MHz signal from the oscillator circuit. The counter is reset and prevented from counting (inhibited) by the HIGH state of the HCH control line. The HCH line goes HIGH and stays HIGH for 1.2 seconds following the depression of the X-Y PLOT pushbutton. NAND gate U76A, which is fed by the 1 MHz clock pulse, is enabled by the HIGH state of the LPLOT control line. This line is HIGH when plotting is not in progress. NAND gate U77A, which is fed by the 488.3 Hz clock pulse, is enabled when both the HPLOT and the LDLPLOT lines are HIGH. These two lines are both HIGH at the same time only during the X-Y plot/refresh, single-channel mode. NAND gate U77B, which is fed by the 244.1 Hz clock pulse, is enabled when both the HPLOT and the HDLPLOT control lines are HIGH. These two lines are both HIGH at the same time only during the X-Y plot/refresh, dual-channel mode. The four control lines mentioned in this paragraph (HCH, LPLOT, HPLOT, and LDLPLOT) are generated in the Refresh X-Y Plot Control circuit (paragraph 7-7.22b).

7-7.18 Store Trace A (STA) and Store Trace B (STB) Circuits

These circuits generate a pulse that causes the storage memory write pulse (LMWE) to be generated when either the Channel A STORE TRACE pushbutton is depressed (STA circuit) or the Channel B STORE TRACE pushbutton is depressed (STB circuit). When the applicable STORE TRACE pushbutton is depressed, the pulse generated by these circuits, HWM, is coincident with the sweep generator's forward frequency sweep.

The STA and STB circuits are identical in layout and operation. A simplified schematic, with timing diagram, of the STA circuit is presented in Figure 7-86. A parts locator diagram of these circuits is shown in Figure 7-87, and their schematic is shown in Figure 7-88.

The timing diagram in Figure 7-86 shows the logic states, and pulses, present throughout the circuit when an STA cycle is initiated. The LOW states of U81A-1 and U82A-2 are caused by the U81A-U81B latch circuit. The respective logic states of U82A-5 and U83C-8 are caused by the sweep generator retrace blanking pulse (LRTR) clocking the U82A flip-flop. The width of the U83C-10 pulse is a result of U82A being clocked by LRTR pulse #1 and U82B being clocked by LRTR pulse #2. This pulse width is equal to the length of the entire horizontal sweep ramp, i.e., forward sweep and retrace.

The width of the U79D-13 pulse, which is the the circuit output, results from U79D-12 being inhibited by the positive level of the RTR pulse. (When the LRTR pulse goes away, the LOW state of the line enables the U79C pulse to pass through the gate.) The U79D-13 pulse width is equal to the length of the forward sweep only, as opposed to being equal to the length of both the forward and reverse sweeps.

The STA cycle is terminated by the logic state of U82B-8. This logic state is caused by the rising edge of LRTR pulse #2; its width is set by the time constant of the R187 C75 RC network. The U82B-8 pulse resets the latch and causes the STORE TRACE indicator to go off.

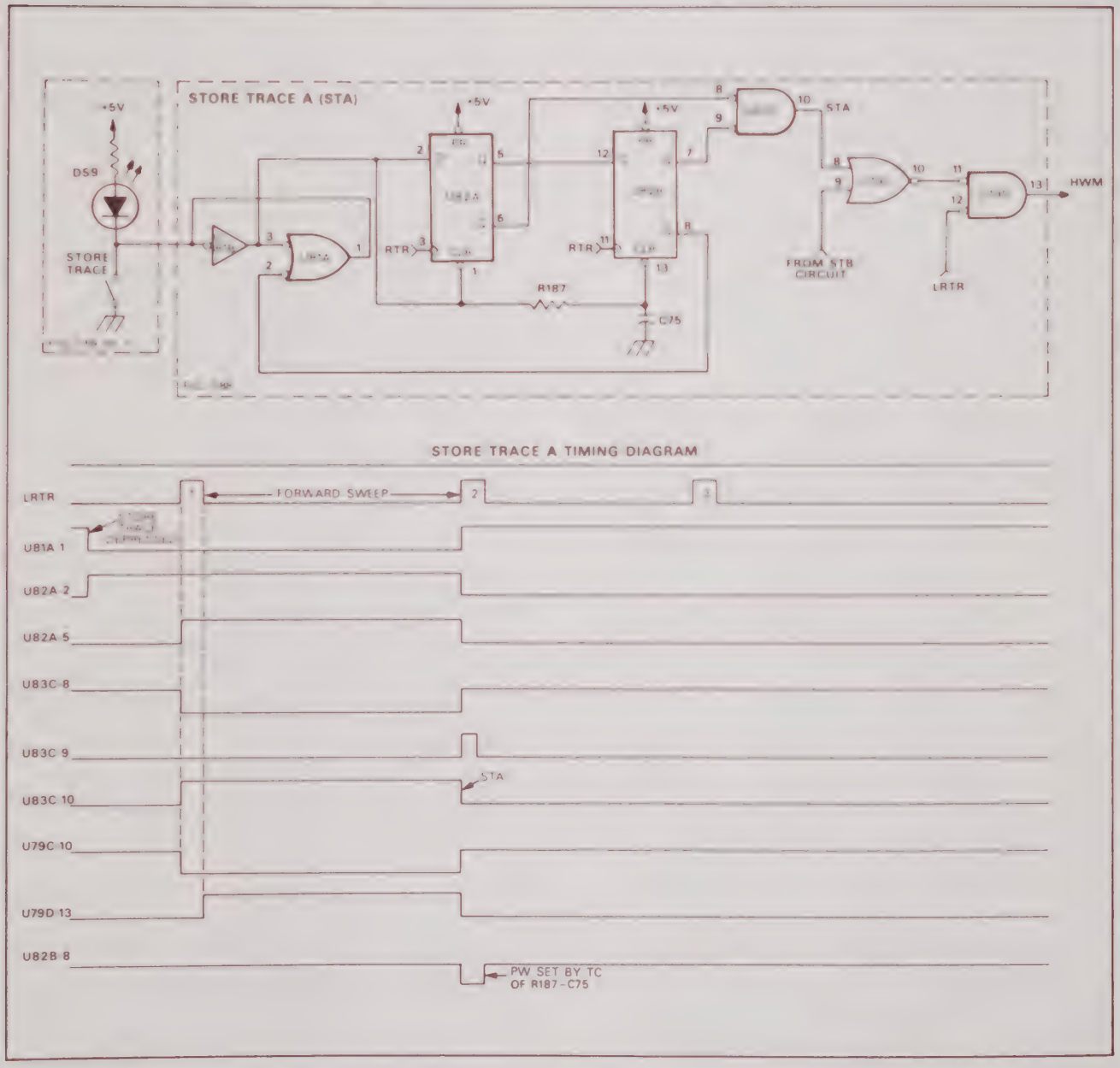


Figure 7-86. Store Trace A, Simplified Schematic and Timing Diagram

7-7.19 Refresh Write Enable Control Circuit

This circuit (Figure 7-88) controls the logic state of the HERWB, LERWB, and LRWE control lines. These control lines are put in their active states as shown below.

- The HERWB control line goes HIGH and the LERWB control line goes LOW when the HEWB control line is HIGH (new vertical data is available) and when the LPLOT control line is HIGH (X-Y plot not in progress).

- The LRWE control line goes LOW when (1) the 560A is not engaged in an X-Y plotting operation, (2) the 560A is not in in the REFRESH HOLD display mode, (3) the sweep generator is not supplying a retrace blanking pulse, (4) the 1 MHz system clock pulse delayed by the R186/C74 RC network is HIGH, and (5) new vertical data is available (vertical A/D converter has completed a conversion cycle).

A parts locator diagram for this circuit is shown in Figure 7-87, and the schematic diagram is shown in Figure 7-88. The circuit consists of flip-flop U78A, NAND gates U76D, U76B, U84D and U79A, and inverter U74E.

7-7.20 Refresh-Real Time Channel A/B Alternating Sweep, Pen-Lift Relay, CRT Blank, and X-Y Plot Multiplexer Circuit

This circuit multiplexes between refresh and real time control signals for the Channel A/B alternating sweep logic (LCA/HCA control lines), pen-lift (pen-drop) relay control, CRT BLANK/BLANK OUT signal lines, and X-Y plot LED (PLOT ON) control line. A parts locator diagram for this circuit is shown in Figure 7-87, and the schematic is shown in Figure 7-88.

The circuit consists of multiplexer U80 and associated components. Channel A/B alternating sweep uses the multiplexer's A1-B1-Y1 section, the pen-lift relay uses the A2-B2-Y2 section, CRT blanking uses the A3-B3-Y3 section, and X-Y plot LED control uses the A4-B4-Y4 section.

U80 multiplexer control is provided by the LRLTM control line applied to the SELB control input. When the 560A is in the REAL TIME display mode (LRLTM logic 0), the signals on the A input pins are applied to the Y output pins. Conversely, when the 560A is in the REFRESH display mode (LRLTM logic 1), the signals on the B input pins are applied to the Y output pins.

7-7.21 Remote-Local Channel Select Multiplexer Circuit

This circuit multiplexes between the locally-generated LINTA signal and the GPIB-generated LEXT DETA signal to supply channel-select logic (DETA control signal) to the A3 PCB. On the A3 PCB the DETA control signal is used to switch the A, B log amplifier's input to either the A or B front panel input connector.

This circuit also looks at the state of the LA control line from the Interface Control (A8) PCB. The LA control line informs the circuit (1) whether the rear panel INPUT switch is in the A ONLY position, and (2) whether the sweep generator is in the alternate-sweep mode.

When the INPUT switch is in the A ONLY position, it causes a LOW (HCG) to be placed on the LA control line. A LOW condition on the LA line causes U86A to reset the LDETA line LOW. When the LDETA line is LOW, it causes only the Channel A input to be connected to the log amplifier. For more information on the INPUT switch, refer to paragraph 7-12.1.

A sweep generator in the alternate-sweep mode sends two control signals to the 560A via the rear panel AUX I/O connector. One of the control signals from the sweep generator - alternate sweep (LALTE) - is sent to the A2 board over the LA control line. When the sweep generator resets the LALTE control line LOW, U86A resets the

LDETA control line LOW to connect only the Channel A input to the log amplifier.

For more information on alternate sweep, refer to paragraph 7-11.3.

A parts locator diagram for this circuit is shown in Figure 7-87, and the schematic is shown in Figure 7-88. The multiplexer circuit consists of gates U86A, U86B, and U86C and inverter U86D.

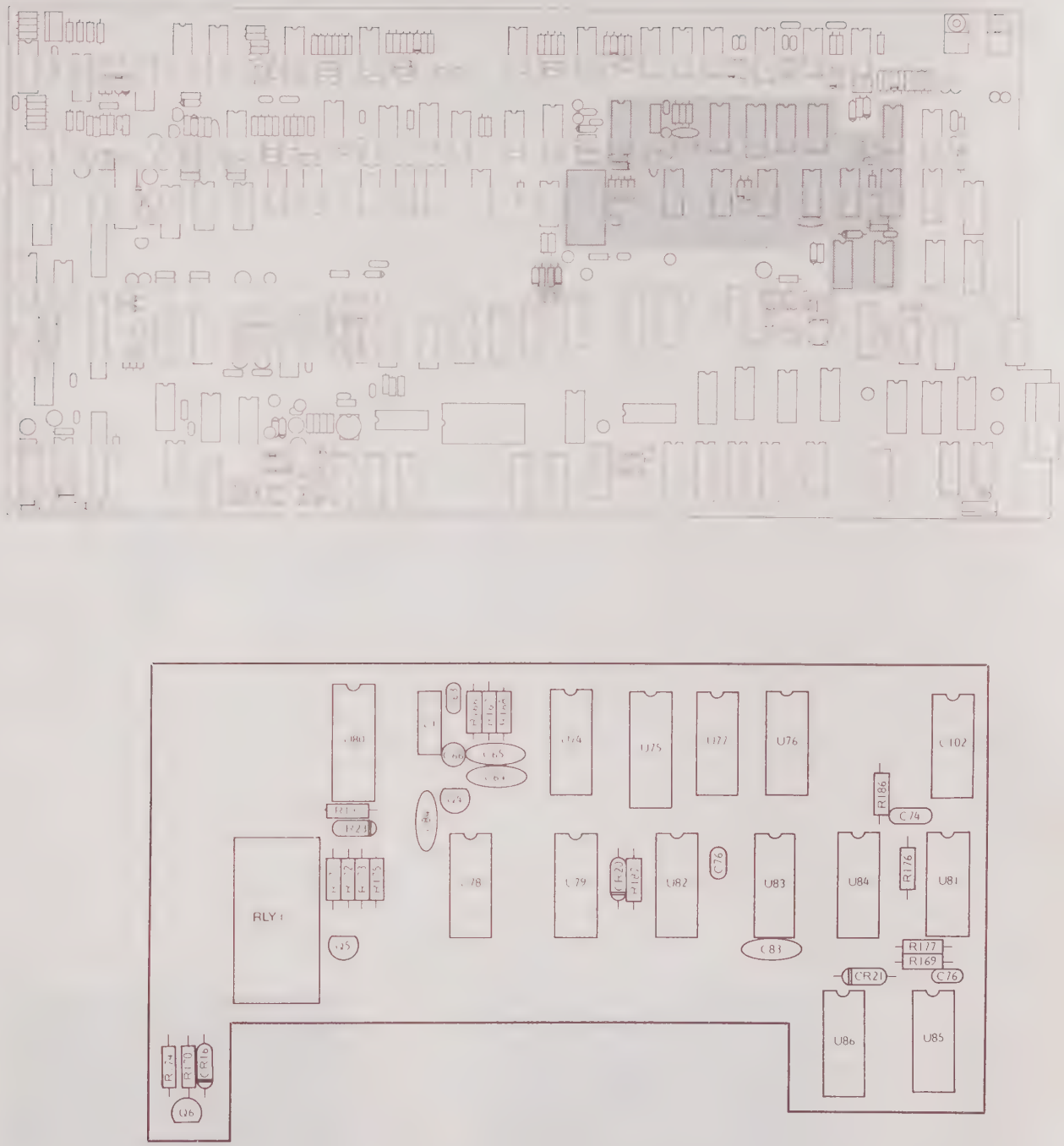
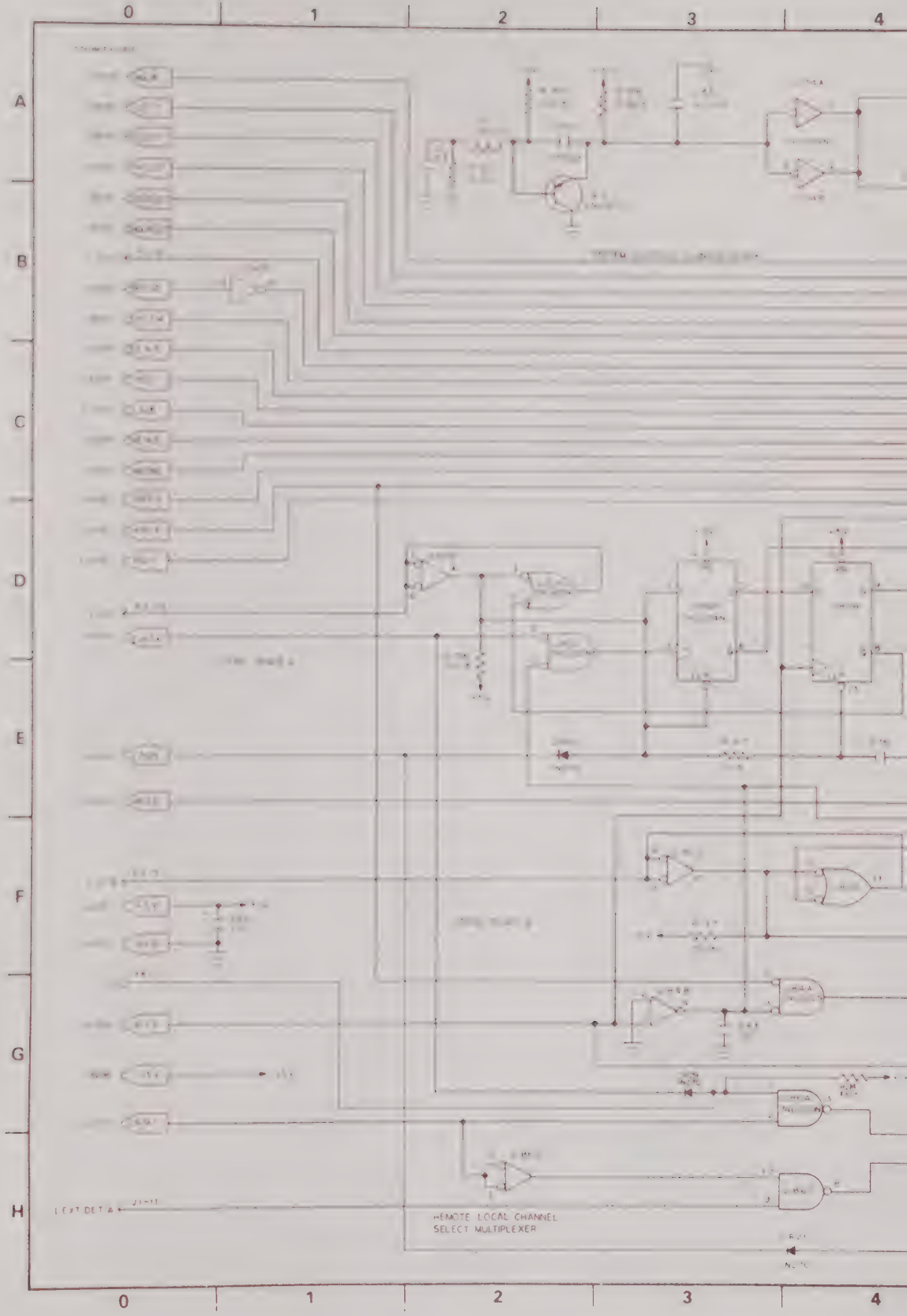


Figure 7-87. Digital (A2) PCB System and Output Counter Clock; Store Trace A etc.; Refresh Write Enable Control; Refresh-Real Time etc.; Remote-Local Channel Select etc. Circuits Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
REMOTE LOCAL CHANNEL
SELECT MULTIPLEXER

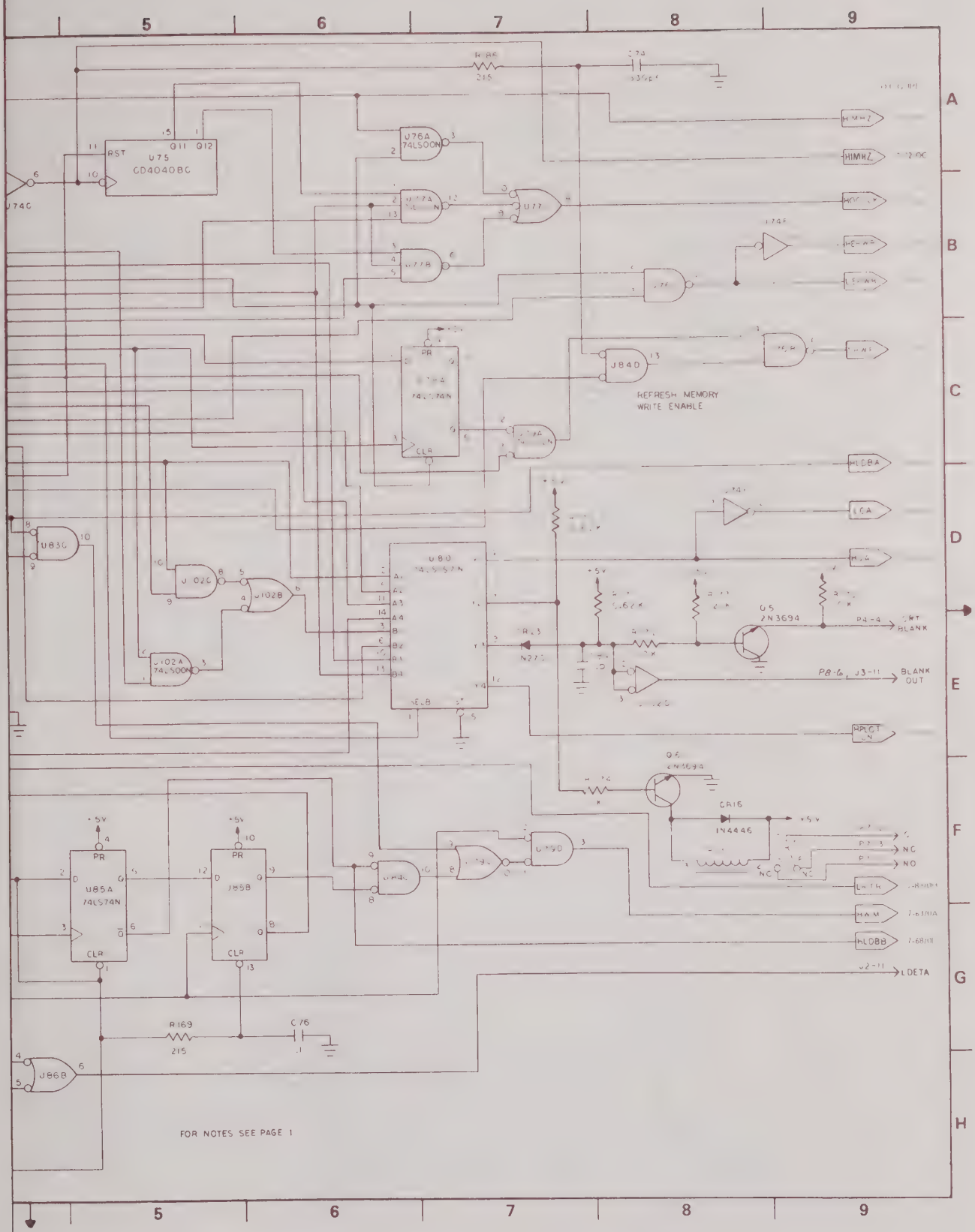


Figure 7-88. Digital (A2) PCB System and Output Counter Clock; Store Trace A etc.; Refresh Write Enable Control; Refresh-Real Time etc.; Remote-Local Channel Select etc. Circuits Schematic Diagram

Figure 7-87.

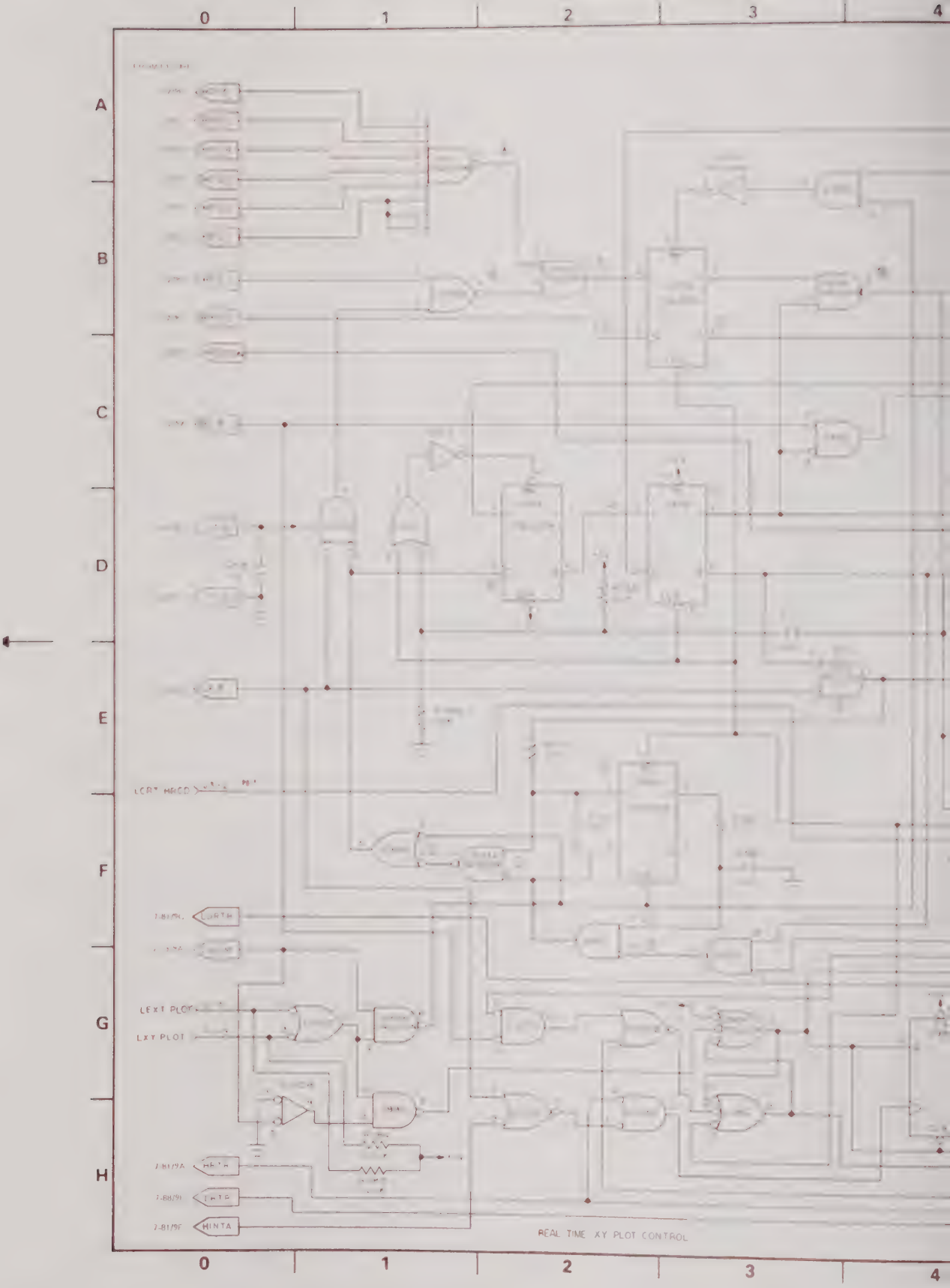
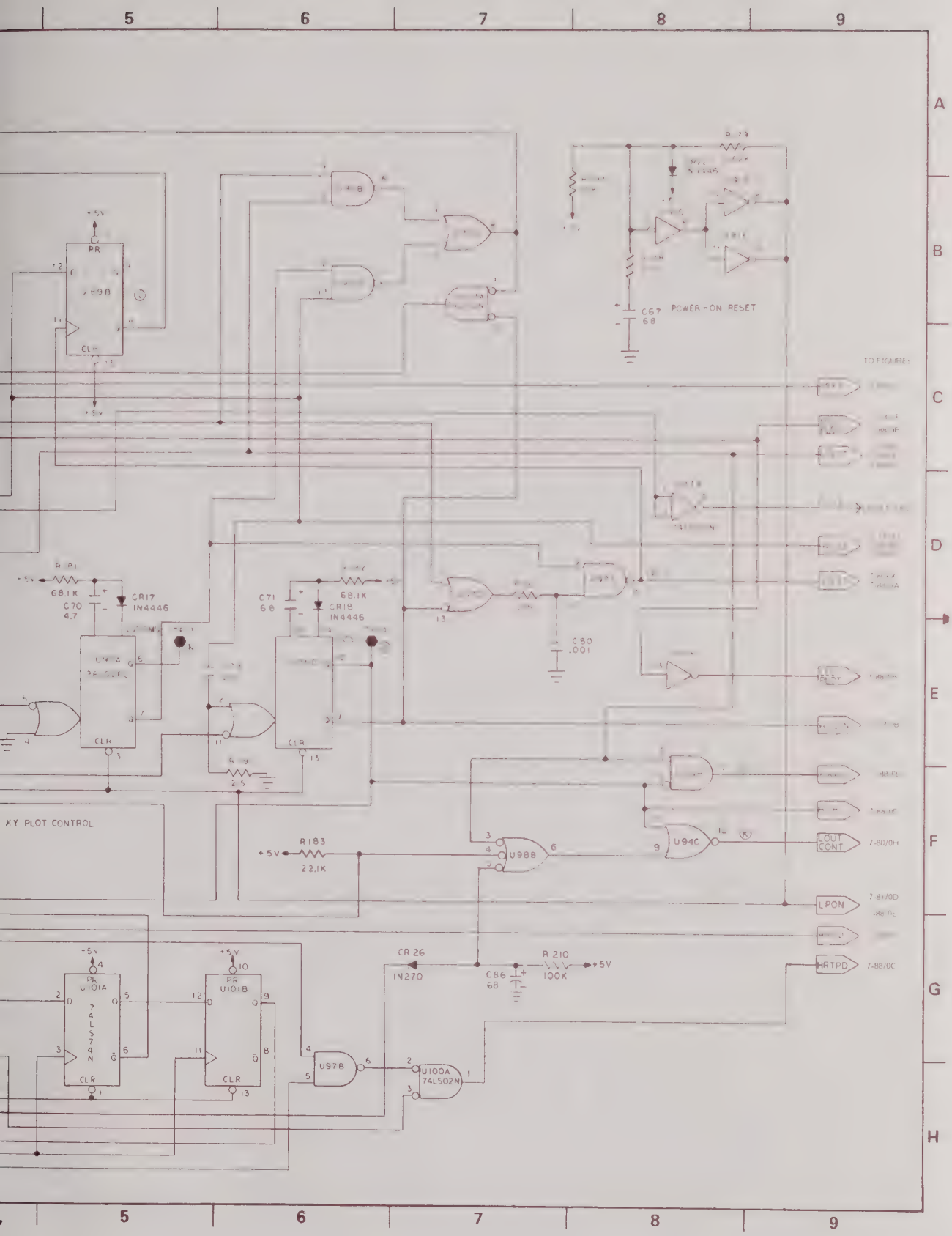


Figure 7-89. Digital (A2) PCB Real Time and Refresh X-Y Plot Control Circuits Schematic Diagram


POWER-ON RESET
C67
68
TO FIGURE
XY PLOT CONTROL
R183
22.1K
+5V
U988
U94C
LOUT CONT
7-80/0H
LPON
7-84/0D
HRTPD
7-88/0C
CR 26
IN270
C86
68
R 210
100K
U101A
U101B
74LS74N
U97B
U100A
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CR17
IN4446
CR18
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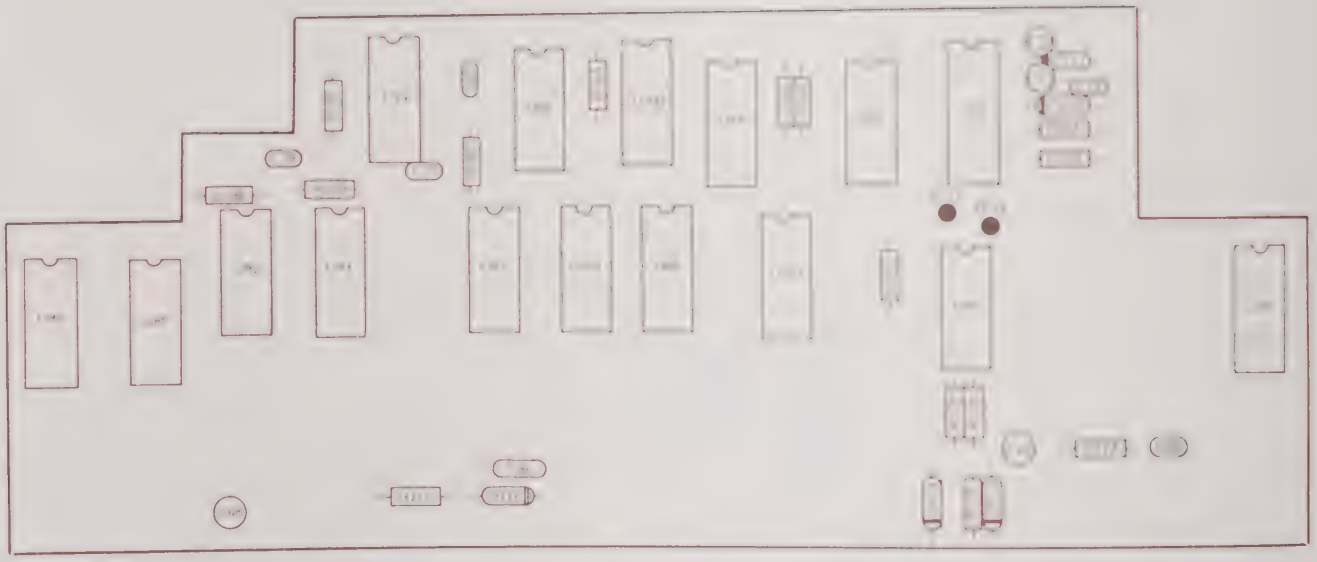
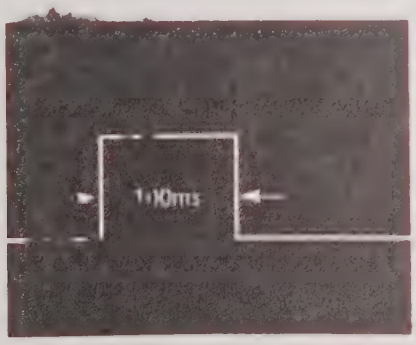
68.1K
C70
4.7
C71
68
C80
.001

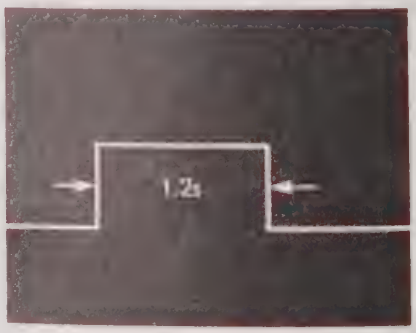


TP 13



TP13 pulse seen at end of refresh plot

TP 14



TP14 pulse seen at beginning of refresh plot

Figure 7-90. Digital (A2) PCB Real Time and Refresh X-Y Plot Control Circuits Parts Locator Diagram

Figure 7-89.

7-7.22 Real Time and Refresh X-Y Plot Control Circuits

These two circuits are described below.

a. Real Time X-Y Plot Control Circuit. This circuit

- controls the pen-lift relay.
- positions the pen at upper-right corner after plot end.
- controls the application of X and Y data to the rear panel HORIZONTAL OUTPUT and VERTICAL OUTPUT connectors if the rear panel OUTPUT MODE switch is in the RCDR position.
- ensures that after the X-Y PLOT pushbutton is depressed, (1) if the 560A is in single-channel operation, the plot begins at the start of the next forward sweep, or (2) if the 560A is in dual-channel operation, the plot begins at the start of the Channel A forward sweep. (Refer to paragraph 7-7.12 for the discussion on single and dual-channel sweep.)

The full schematic for this circuit is shown in Figure 7-89, the parts locator diagram is shown in Figure 7-90, and a simplified schematic is shown in Figure 7-92.

For single-channel operation, the timing diagram of Figure 7-92 shows the various circuit-component output conditions when a plot cycle is initiated. These output conditions are described below.

The HRTR pulse is the retrace blanking pulse from the sweep generator; this pulse is HIGH during sweep generator retrace time and LOW during forward sweep time.

The U99C-8 pulse initiates circuit operation. This pulse occurs when the X-Y PLOT pushbutton is depressed while the REAL TIME pushbutton is engaged; its width is determined by the length of time the X-Y PLOT pushbutton remains depressed.

The U98A-12 pulse is caused by the U98A/U98C latch. This pulse provides the input to flip-flop U95B and turns on the X-Y PLOT indicator.

The U98C-8 pulse (via the LOUT CONT line), causes the X and Y data to be applied to the HORIZ OUTPUT and VERT OUTPUT connectors.

Flip-flop U95B is clocked by the rising edge of the U103D output pulse, which is coincident with the trailing edge of the HRTR pulse. Clocking U95B in this manner ensures that the plot begins with the start of the next forward sweep during single-channel operation or with the start of the Channel A forward sweep during dual-channel operation.

The U97B-5 pulse, LRTR, is the inverted retrace blanking pulse.

The U97B-4 pulse is the delayed HRTR pulse. This pulse, LDRTR, is delayed 500 ms from the falling edge of the HRTR pulse. The delay is provided by one-shot multivibrator U69B (Figure 7-81).

The U97B-6 pulse goes LOW coincident with the rising (trailing) edge of the LDRTR pulse. Only at this time are both inputs to U97B HIGH.

The U100A-1 pulse, the pen-lift relay control signal (HRTPD), goes HIGH 500 ms after the forward sweep begins. This delay allows the recorder's pen time to respond to the vertical position of the plot before pen-drop occurs.

The U101A-6 pulse is the reset pulse; it resets the latch, which in turn resets U95B, U101A, U101B, and U98C.

The R210/C86 network delays pen movement to rest position until after pen lift.

For dual-channel operation, the circuit operation is the same as described above except for the following: instead of U101A resetting the circuit after a single forward sweep, U101B resets the circuit after two forward sweeps. That is, the circuit is reset following the second forward sweep after the Channel A plot starts.

Dual-channel plot operation occurs as follows: (1) Channel A is plotted. (2) The sweep generator's frequency sweep retraces, the recorder pen lifts, and the LDRTR one-shot multivibrator initiates a new 500 ms delay pulse. (3) Channel B is plotted. At the end of the Channel B plot, the circuit is reset and the X-Y PLOT indicator turns off.

b. Refresh X-Y Plot Control Circuit. This circuit

- controls the pen-lift relay.
- positions pen at upper-right corner following plot.
- provides a 1.2-second delay between the time a plot is initiated (X-Y PLOT indicator lights) and the time the pen-lift relay is energized (recorder pen-drop occurs).
- provides for aborting of the plot before full 30-second plot time has elapsed.
- controls application of the X and Y data to the rear panel HORIZONTAL OUTPUT and VERTICAL OUTPUT connectors if the rear panel OUTPUT MODE switch is in the RCDR position.
- initiates a plot on the 1st count from the Refresh Address Control circuit's output counter when the 560A is in a single-channel sweep mode. When the 560A is in a dual-channel sweep mode, the circuit initiates two plots: a Channel A plot that begins on the output counter's 1st count, and, after a delay of 1.2 seconds, a Channel B plot that begins on the output counter's 512th count.
- generates the refresh ramp generator reset pulse, LRST. During single-channel operation, LRST is generated on the 1016th count from the output counter and remains in its low-active state until a count of 1023 is reached. It is generated the first time on a count of 504 and remains LOW thru a count of 511. It is generated again on a count of 1016 and remains LOW thru a count of 1023.

The schematic diagram for this circuit is shown in Figure 7-89. Timing diagrams that show circuit-component output conditions during single and dual sweep operations are presented in Figure 7-93 and 7-94, respectively.

In the single-sweep timing diagram of Figure 7-93, the pulses shown at Ⓐ result from ANDing the HOC 1 thru HOC 6 output count lines from the output counter. These six lines are only high simultaneously during counts of 504-511 and 1016-1023 (see Figure 7-91).

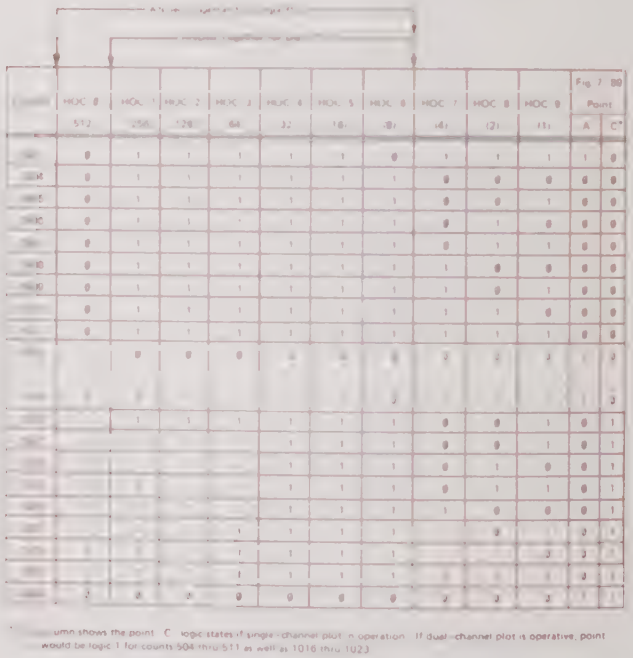


Figure 7-91. Output Counter Logic States

The pulse shown at Ⓑ results from the logic 1 state of the HOC 0 line. The HOC 0 line is HIGH only during counts of 512-1023.

The Ⓓ pulse, HINDC, clocks delay flip-flop U89A. A HINDC pulse occurs for each output counter count pulse. The HINDC pulse is slightly delayed from the count pulses by the refresh address control circuit's timeslot generator.

The pulse shown at Ⓔ is the delay pulse.

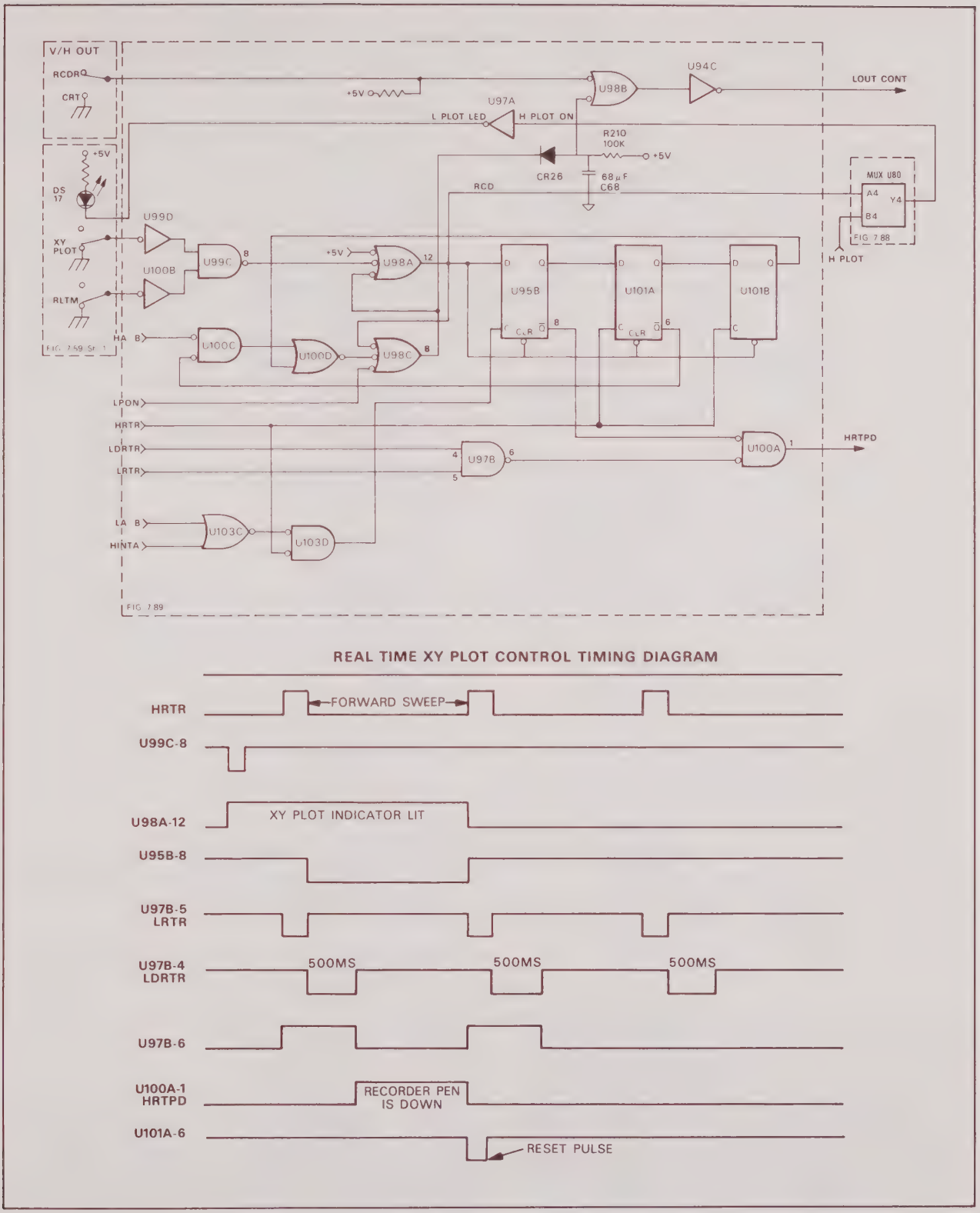


Figure 7-92. Real Time X-Y Plot Control Circuit, Simplified Schematic and Timing Diagram

The low state of this pulse gates LRST LOW; its trailing edge clocks the plot flip-flop, U92B.

The (F) pulse, LRST, is the refresh ramp generator reset pulse. In the refresh mode, this pulse is released to return to its inactive HIGH state when the delay pulse goes away. In the PLOT mode, LRST is released when the 1.2-second pulse from one-shot U96B times-out.

The pulse shown at (G) occurs when the X-Y PLOT pushbutton is depressed while the REFRESH pushbutton is engaged (LRLTM is logic 1). This pulse clocks the plot-start flip-flop, U92A.

The (H) pulse provides the input for U92B. When U92B is clocked by the trailing edge of the delay pulse, the (I) pulse at U92B-Q is created. This is the HPLOT pulse; the U92B-$\overline{Q}$ pulse is the LPLOT pulse. The leading edge of HPLOT triggers the 1.2-second one-shot, U96B.

The LOW state of LPLOT enables U94B-5, and, if the OUTPUT MODE switch is in RCDR, gates the LOUT CONT line LOW. The LOW state of the LOUT CONT line closes FET switches U59A and U59B (Figure 7-80), thereby applying horizontal and vertical data to the rear panel HORIZONTAL OUTPUT and VERTICAL OUTPUT connectors. The LOUT CONT line is gated back to its inactive HIGH state when the 1.2-second pulse times-out and U96B-Q returns to its stable state.

The (L) pulse, RPD, controls pen-lift relay RLY 1. This pulse is gated HIGH for 1.2 seconds when one-shot U96B is triggered by the reset pulse, (M). When HPLOT is HIGH, the reset pulse occurs coincident with a count of 1016. In addition to triggering U96B, the reset pulse resets flip-flop U92A and triggers U96A, a 100 ms one-shot. The trailing edge of the 100 ms U96A-Q pulse clocks U92B to its plot-off state (Q LOW, $\overline{Q}$ HIGH).

The pulse shown at V resets U89A when the X-Y PLOT pushbutton is depressed.

The dual-sweep timing diagram of Figure 7-94 is similar to the single-sweep timing diagram (Figure 7-93) except that two plots and two reset pulses are generated instead of one. The difference for the dual-plot timing diagram is the pulses shown at (O) thru (U). These pulses are used with flip-flop U95A and its associated gates and components to (1) generate a pulse that will initiate a new plot at the end of the Channel A plot, and (2) inhibit the generation of a plot-initiating pulse at the end of the Channel B plot.

In Figure 7-94, the pulse shown at (O), which is the LPLOT pulse, is LOW during plot.

The logic level shown at (P) is LOW when both channels are on.

The pulse shown at (Q) results from ANDing the above two pulses; this pulse is delayed from going LOW coincident with LPLOT by the RC time constant of R190 and C78.

The narrow pulse shown at (R) is created by the changing logic states of LPLOT.

The trailing edge of the pulse shown at (S) clocks flip-flop U95A.

The (T) pulse inhibits U93D and prevents a second plot-initiating pulse from being developed at the end of the Channel B plot.

The pulse shown at (U) initiates the Channel B plot.

7-7.23 Power-On Reset Circuit

This circuit develops a short-duration LOW pulse for resetting circuit components each time the 560A is turned on. The schematic for this circuit is shown in Figure 7-89, and the parts locator diagram is shown in Figure 7-90. The circuit consists of inverters U91C, U91D and U91E, and associated components.

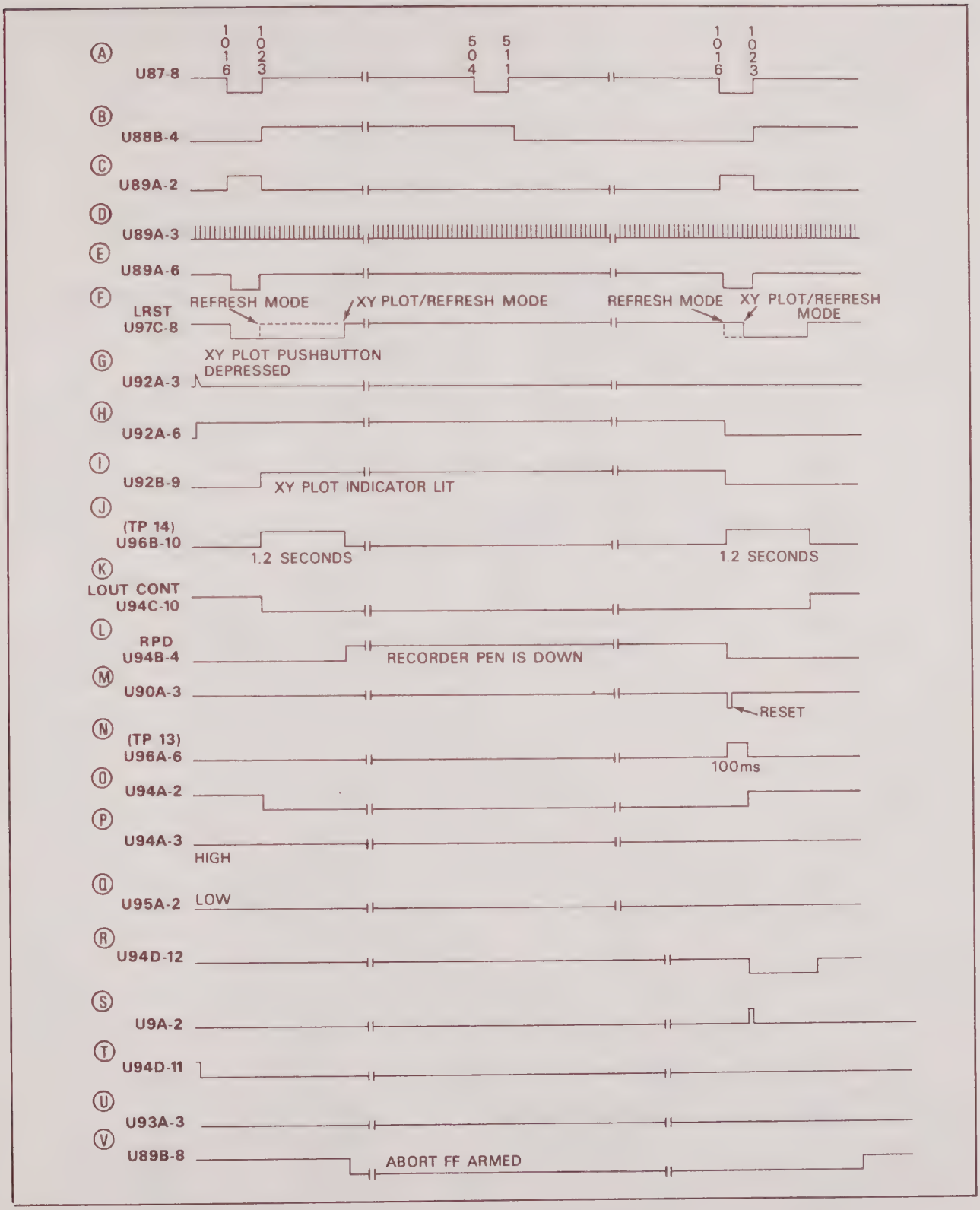


Figure 7-93. Refresh X-Y Plot Single-Channel Sweep Timing Diagram

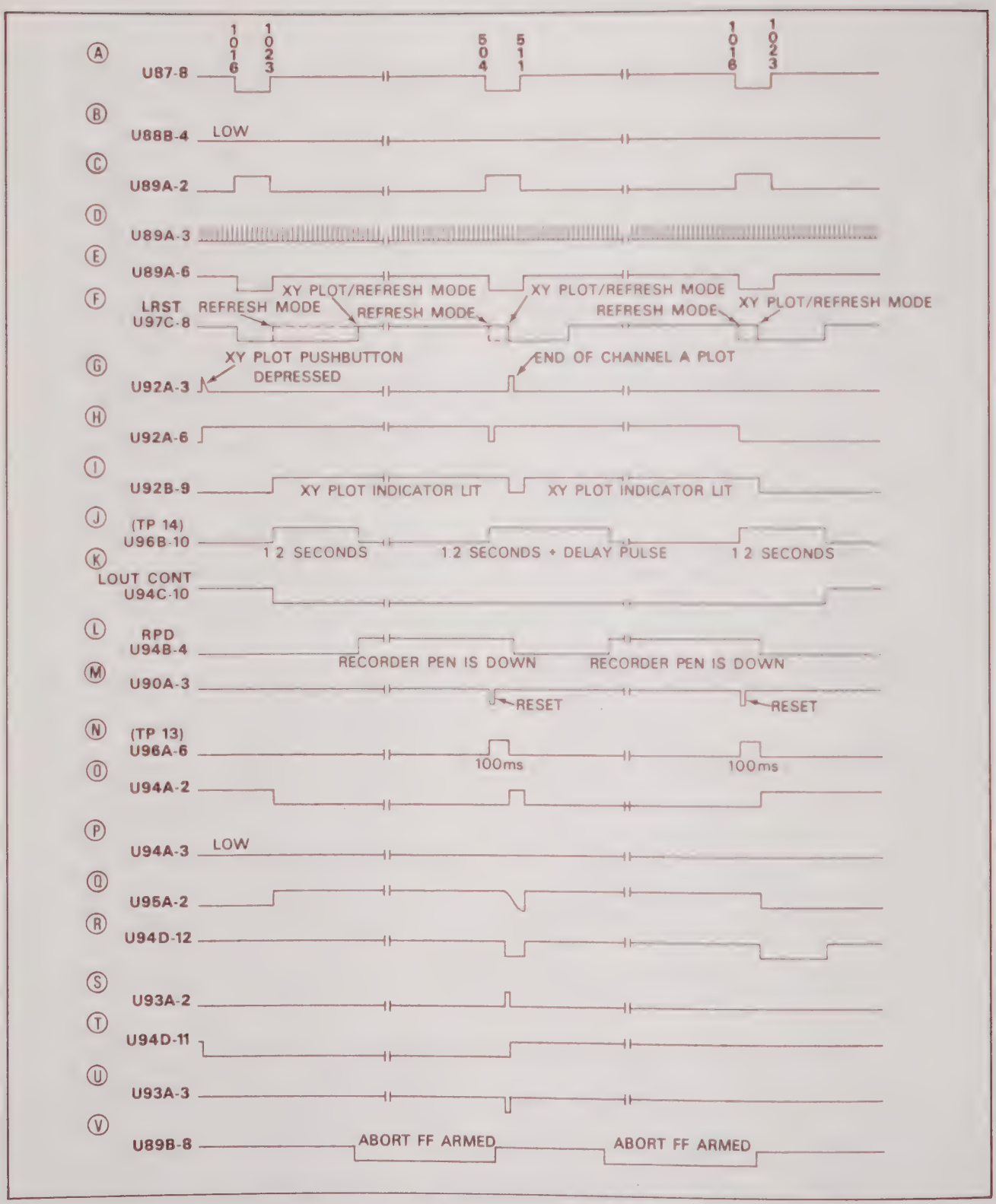


Figure 7-94. Refresh X-Y Plot Dual-Channel Sweep Timing Diagram

LEGEND:

Abbreviations and Symbols:

ADD – Address
I/O – Input/Output
K – Constant
MUX – Multiplexer
R/W – Read/Write
SEL A/B – Select Channel A or Channel B
TSB – Tri-state bus
9 BIT A/D – 9 BIT analog-to-digital converter
9 BIT D/A – 9 BIT digital-to-analog converter
10 BIT A/D – 10 BIT analog-to-digital converter

Summing circuit

Constant current sink

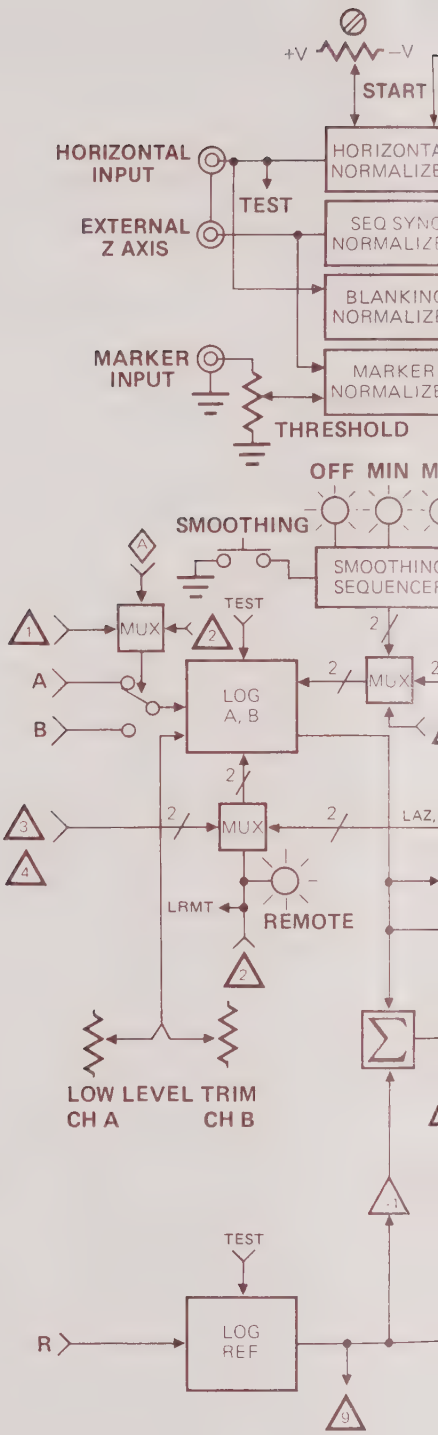
−1 Analog inverter

Mnemonic symbols for control lines from GPIB:

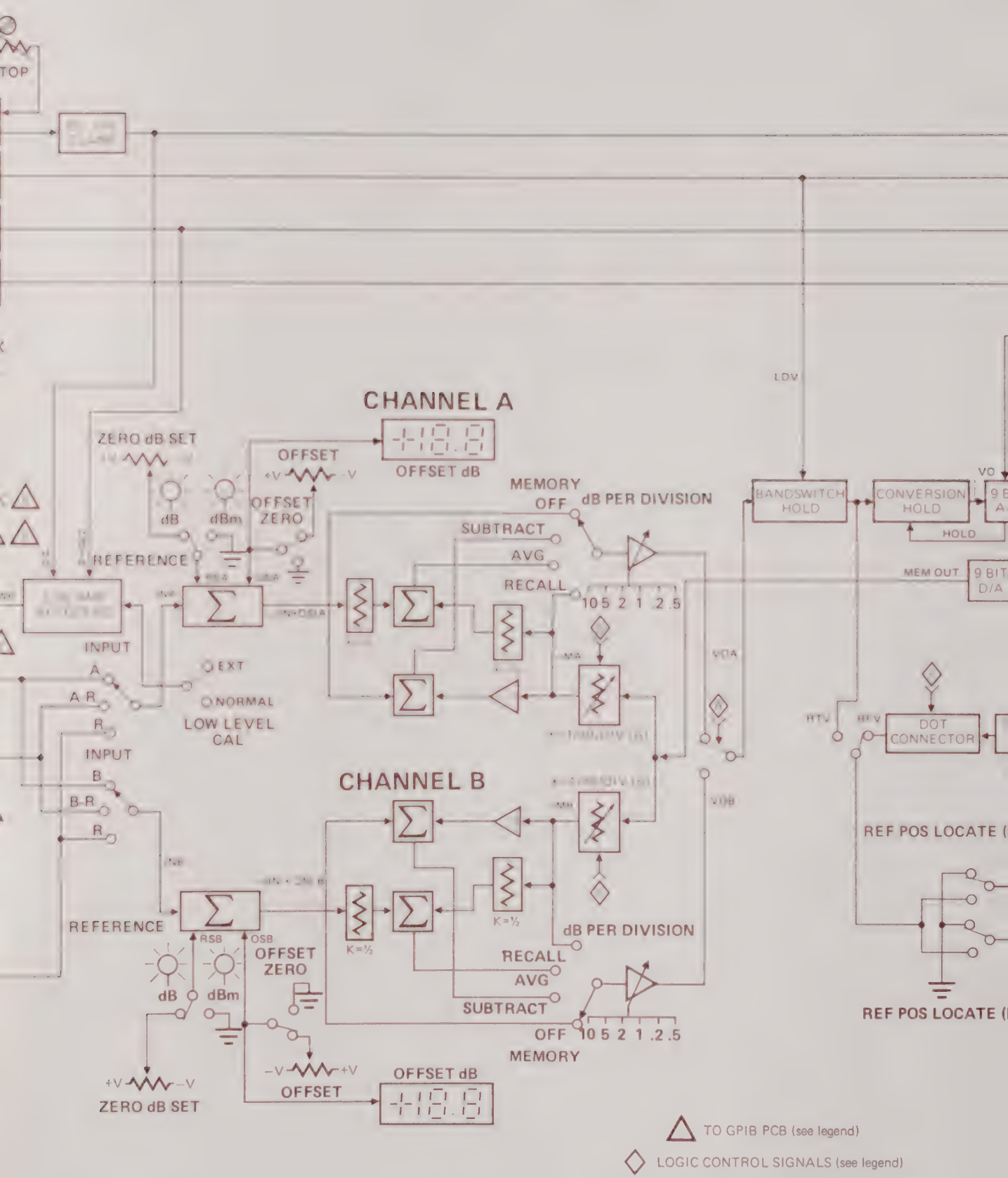
1 LEXT DATA
2 LRMT
3 LEXT AZ
4 LEXT SWR
5 LEXT FILT 1
6 LEXT FILT 2
7 LOG A, B
8 LOG A, B-R
9 LOG R
10 –EXT VERT

Mnemonic symbols for logic control signals:

A HINTA/LINTA
B LDBA
C LDBB
D LRLTM
E LDC
F LMWE
G HLML
H LRWE
I HLRL
J LCA/HCA
K HOCCLK
L HOCEN
M LERWB
N HERWB
O LPLOT
P HRPD/HRTPD
Q LOUT CONT



ΔSee Title Page


CHANNEL A
ZERO dB SET
OFFSET
-10.0
OFFSET dB
dB
dBm
OFFSET ZERO
MEMORY
OFF
dB PER DIVISION
SUBTRACT
AVG
RECALL
10 5 2 1 .2 .5
REFERENCE
INPUT
A
A R
R
EXT
NORMAL
LOW LEVEL CAL
INPUT
B
B-R
R
CHANNEL B
REFERENCE
RSB
OSB
OFFSET ZERO
dB
dBm
K=½
K=½
dB PER DIVISION
RECALL
AVG
SUBTRACT
OFF
10 5 2 1 .2 .5
MEMORY
+V
-V
ZERO dB SET
-V
+V
OFFSET
OFFSET dB
-10.0
LDV
BANDSWITCH HOLD
CONVERSION HOLD
HOLD
MEM OUT
9 BIT D/A
VDA
VDB
RTV
RFV
DOT CONNECTOR
REF POS LOCATE
REF POS LOCATE
TO GPIB PCB (see legend)
LOGIC CONTROL SIGNALS (see legend)

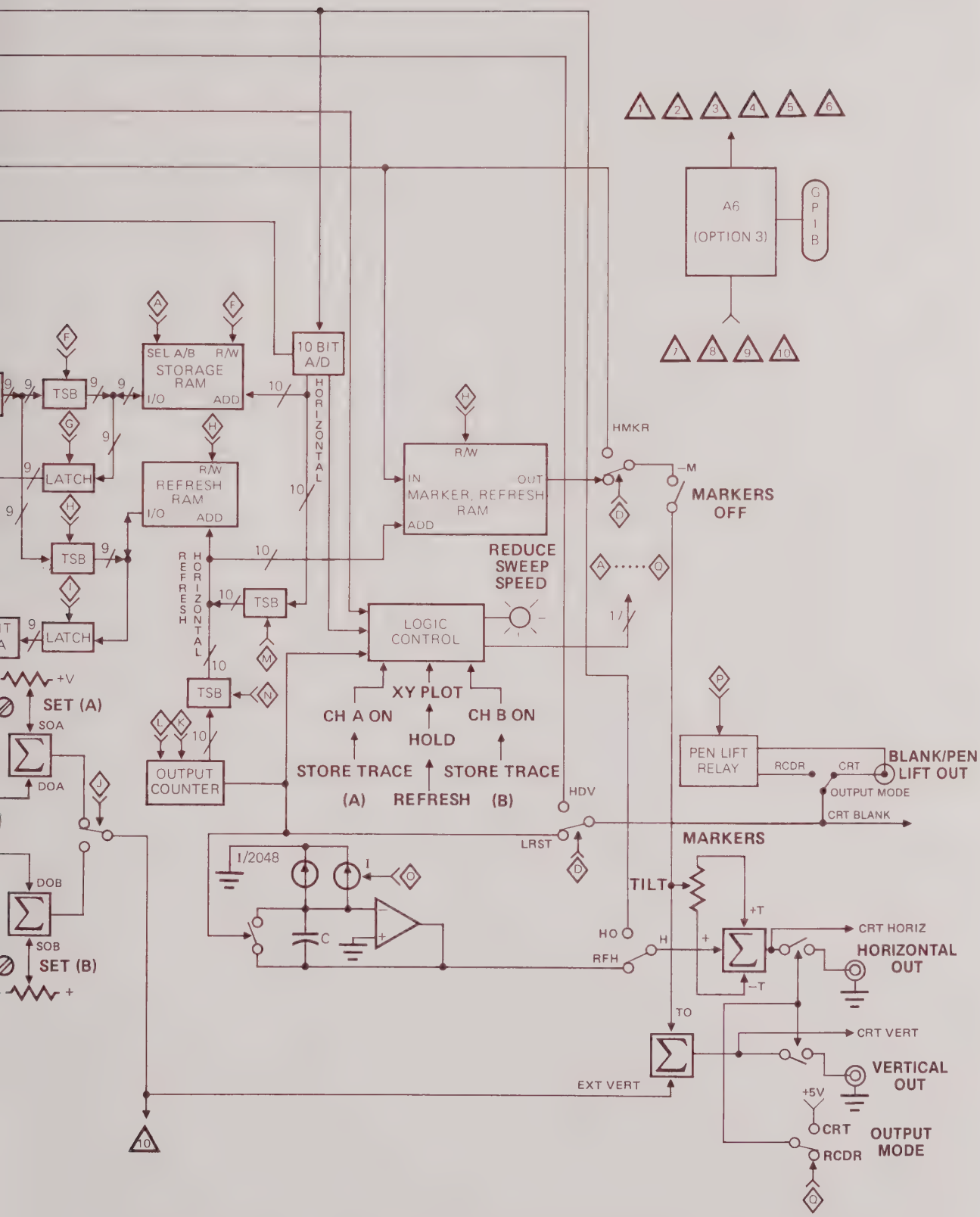


Figure 7-95. Front Panel (A1) and Digital (A2) PCBs Detailed Block Diagram

7-7.24 Detailed Block Diagram of the A1/A2 PCBs

A detailed block diagram of the A1-A2 PCB is presented in Figure 7-95. This diagram shows the overall functional orientation of the circuits described in paragraphs 7-7.1 thru 7-7.23.

7-8 GPIB INTERFACE (A6) PRINTED CIRCUIT BOARD

This printed circuit board (PCB) interfaces the 560A Scalar Network Analyzer to the General Purpose Interface Bus (GPIB). The A6 PCB contains 20 major circuits, diagrammed on 6 sheets of schematics. To provide continuity between schematics, a system of descriptive mnemonic symbols identifies control and signal lines. Table 7-3 provides an alphabetical listing of these mnemonic symbols. The listing also includes "Definition," "To," and "From" columns for each symbol.

To interconnect the A6 PCB with the GPIB and the 560A, two connectors are used. Connector P1, via the rear panel GPIB interface connector, connects A6 circuits with the GPIB. Connector J1, via the Digital (A2) PCB, connects A6 circuits with the 560A. Figure 7-96 provides a pin-out chart for each of these connectors.

To describe the GPIB capability built into the 560A, the chart in Figure 7-97 is presented. This chart lists the IEEE Standard 488 functions by subset number. A description of capability is provided for each function.

To provide integrated maintenance instructions, technical information for the A6 PCB is organized into blocks of data. Each schematic is presented on a foldout page. Along with the schematic is a parts locator diagram showing the physical location of applicable components, and, where appropriate, photographs showing waveforms at schematic test points. The description for each circuit shown on any particular schematic is contained on an adjacent, facing page.

To begin the circuit descriptions, an overall block diagram is presented in Figure 7-98. This diagram shows the A6 PCB major circuits; the diagram also shows the signal and control lines, each identified by a mnemonic symbol, that connect these circuits together. Each of the circuits shown on this block diagram is described in a separate, numbered paragraph under this major heading. For example, the Address Recognition Circuit is described in paragraph 7-8.2, the Listen Function Circuit in 7-8.3, and the Acceptor Handshake Circuit in 7-8.4. Proceed to paragraph 7-8.1, GPIB Bus Transceiver Integrated Circuits, for the first circuit description.

Table 7-3. Listing of Mnemonic Symbols used with A6 PCB Circuits

MNEMONIC	DEFINITION	FROM*	TO*
ADCIN	A/D Converter Input Signal	Fig. 7-111/7A	Fig. 7-116/0B
EXT VERT	External Vertical Input Signal	A2 PCB via A6J2-1	Fig. 7-111/0A
HATNI	High active-state, Attention Input Signal	Fig. 7-102/9D	Fig. 7-110/0C
HAZSEQ	High active-state Autozero (Calibrate) Sequence In Progress Signal	Fig. 7-111/9C	Fig. 7-102/0E & Fig. 7-110/0C
HCONC	High active-state, Conversion Complete-Output Signal	Fig. 7-116/9G	Fig. 7-110/0H
HCONV	High active-state, Start Conversion Signal	Fig. 7-111/9E	Fig. 7-110/0G & Fig. 7-116/0H
HDI01I	High active-state, ASCII Data Bit 1 - Input	Fig. 7-101/9F	Fig. 7-110/0B
HDI01O	High active-state, ASCII Data Bit 1 - Output	Fig. 7-117/9E	Fig. 7-101/0B
HDI02I	High active-state, ASCII Data Bit 2 - Input	Fig. 7-101/9F	Fig. 7-110/0B
HDI02O	High active-state, ASCII Data Bit 2 - Output	Fig. 7-117/9E	Fig. 7-101/0B
HDI03I	High active-state, ASCII Data Bit 3 - Input	Fig. 7-101/9E	Fig. 7-110/0B
HDI03O	High active-state, ASCII Data Bit 3 - Output	Fig. 7-117/9E	Fig. 7-101/0B
HDI04I	High active-state, ASCII Data Bit 4 - Input	Fig. 7-101/9E	Fig. 7-110/0B
HDI04O	High active-state, ASCII Data Bit 4 - Output	Fig. 7-117/9E	Fig. 7-101/0B
HDI05I	High active-state, ASCII Data Bit 5 - Input	Fig. 7-101/9D	Fig. 7-110/0B
HDI05O	High active-state, ASCII Data Bit 5 - Output	Fig. 7-117/9F	Fig. 7-101/0C

*The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

Table 7-3. Listing of Mnemonic Symbols used with A6 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
HDI06I	High active-state, ASCII Data Bit 6 - Input	Fig. 7-101/9D	Fig. 7-110/0B
HDI06O	High active-state, ASCII Data Bit 6 - Output	Fig. 7-117/9F	Fig. 7-101/0C
HDI07I	High active-state, ASCII Data Bit 7 - Input	Fig. 7-101/9C	Fig. 7-110/0A
HDI07O	High active-state, ASCII Data Bit 7 - Output	Fig. 7-117/9F	Fig. 7-101/0C
HDAVI	High active-state, Data Valid - Input Signal	Fig. 7-102/9E	Fig. 7-110/0C
HDAVO	High active-state, Data Valid - Output Signal	U26B-5 (Fig. 7-102/1G)	U4-5
HDBEN	High active-state, Data Bus Enable Signal	Fig. 7-102/9G	Fig. 7-101/0F
HDCAS	High active-state, Device Clear Active State Signal	U30-15 (Fig. 7-110/5G)	U40C-9 & U36A-1
HDCEN	High active-state, Decoder Enable Signal	U28-15 (Fig. 7-110/2B)	U40A-3 & U37E-11
HDDMS	High active-state, Device Dependent Message Strobe Signal	Fig. 7-102/9E	Fig. 7-110/0F & Fig. 7-111/0D
HDETA	High active-state, Detector (Channel) A Signal	Fig. 7-110/9E	Fig. 7-111/0C
HDETB	High active-state, Detector (Channel) B Signal	Fig. 7-110/9E	Fig. 7-111/0C
HDISP	High active-state, Display Signal	Fig. 7-110/9C	Fig. 7-116/0D
HDPON	High active-state, Device Power-On Signal	Fig. 7-110/9A	Fig. 7-111/0D
HEC	High active-state, External Calibrate Signal	Fig. 7-110/9E	Fig. 7-111/0E
HEOIO	High active-state, End or Identify - Output	Fig. 7-117/9G	Fig. 7-102/0C

*The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

Table 7-3. Listing of Mnemonic Symbols used with A6 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
HGTL	High active-state, Go To Local Signal	Fig. 7-110/9G	Fig. 7-104/0C
HHM	High active-state, Hold Mode Signal	Fig. 7-110/9C	Fig. 7-102/0E
HIM	High active-state, Interrupt Mode Signal	U32-7 (Fig. 7-110/6C)	U41A-2, U41B-12 & U39A-5
HIMS	High active-state, Interface Message Strobe Signal	U17C-11 (Fig. 7-102/4D)	U16A-12, U11B-9, U11A-12, U10A-2 & U12D-11
HIFC	High active-state, Interface Clear Signal	GPIB	Fig. 7-102/0D
HIPON	High active-state, Interface Power-On Signal	Fig. 7-110/9A	Fig. 7-102/0C
HLACS	High active-state, Listen Active State Signal	U15B-6 (Fig. 7-102/8D)	U17A-1
HLAD	High active-state, Listen Addressed State Signal	Fig. 7-102/9D	Fig. 7-110/0C
HLAG	High active-state, Listen Address Group Signal	Fig. 7-101/9B	Fig. 7-102/0B
HLC	High active-state, Local Calibrate Signal	Fig. 7-110/9F	Fig. 7-111/0D
HMLA	High active-state, My Listen Address Signal	U15D-11 (Fig. 7-102/7D)	U16A-1
HMLEN	High active-state, Mode Latch Enable Signal	U30-3 (Fig. 7-102/5F)	U35C-9
HMTA	High active-state, My Talk Address Signal	U8C-8 (Fig. 7-102/6B)	U11B-8 & U10B-4
HNL	High active-state, Noise Level Signal	Fig. 7-110/9F	Fig. 7-111/0D
HOTA	High active-state, Other Talk Address Signal	U8D-11 (Fig. 7-102/6B)	U10D-12

*The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

Table 7-3. Listing of Mnemonic Symbols used with A6 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
HREMS	High active-state, Remote State Signal	Fig. 7-102/9E	Fig. 7-111/0E
HRSV	High active-state, Request Service Bit Signal	Fig. 7-110/9E	Fig. 7-102/0C
HSØ	High active-state, Smoothing Off (smoothing level zero) Signal	Fig. 7-110/9F	Fig. 7-111/0E
HS1	High active-state, Smoothing Minimum (smoothing level 1) Signal	Fig. 7-110/9E	Fig. 7-111/0E
HS2	High active-state, Smoothing Maximum (smoothing level 2) Signal	Fig. 7-110/9F	Fig. 7-111/0E
HSETTLE	High active-state, Settle Signal	Fig. 7-111/9D	Fig. 7-102/0E & Fig. 7-110/0G
HSPMS	High active-state, Serial Poll Enable Message Received Signal	U11A-3 (Fig. 7-102/7A)	U13B-4
HSPE	High active-state, Serial Poll Enable Signal	Fig. 7-110/9G	Fig. 7-102/0A
HSPD	High active-state, Serial Poll Disable Signal	Fig. 7-110/9G	Fig. 7-102/0A
HSRQ	High active-state, Service Request Signal	GPIB	Fig. 7-102/0D
HSRQO	High active-state, Service Request - Output Signal	U15A-3 (Fig. 7-102/8C)	U3-4
HSTB1	High active-state, Status Byte Bit 1 Signal	Fig. 7-110/9D	Fig. 7-117/0H
HSTB2	High active-state, Status Byte Bit 2 Signal	Fig. 7-110/9D	Fig. 7-117/0H
HTADS	High active-state, Talker Addressed State Signal	Fig. 7-102/9A	Fig. 7-117/0E
HTAG	High active-state, Talker Address Group Signal	Fig. 7-101/9C	Fig. 7-102/0B
HTRIGEN	High active-state, Trigger Enable Signal	Fig. 7-110/9D	Fig. 7-111/0F

*The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

Table 7-3. Listing of Mnemonic Symbols used with A6 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
HUNL	High active-state, Unlisten Signal	Fig. 7-110/9G	Fig. 7-102/0C
HXY	High active-state, X-Y Plot Signal	Fig. 7-110/9F	Fig. 7-111/0F
LAMPHI/ HAMPLO	Low active-state, Amplitude High (above -30 dBm)/High active-state, Amplitude Low (below -30 dBm) Signal	Fig. 7-116/9A	Fig. 7-111/0F
LATNI	Low active-state, Attention - Input Signal	U9D-8 (Fig. 7-102/8D)	U15B-5, U13B-3, U21D-13 & U13A-2
LAZSEQ	Low active-state, Autozero (Calibrate) Sequence In Progress Signal	Fig. 7-111/9B	Fig. 7-110/0H
LBYAC	Low active-state, Last Byte Accepted Signal	Fig. 7-102/9F	Fig. 7-117/0F
LCHN	Low active-state, Channel Signal	Fig. 7-110/9B	Fig. 7-111/0B
LCONCO	Low active-state, Conversion Complete-Output Signal	Fig. 7-116/9G	Fig. 7-117/0H & Fig. 7-111/0H
LDACI	Low active-state, Data Accepted - Input Signal	U4-14 (Fig. 7-102/1H)	U23C-5 & U24C-11
LDACO	Low active-state, Data Accepted - Output Signal	U21B-6 (Fig. 7-102/1F)	U4-13
LCR/HCR-LF	Low active-state, Carriage Return/ High active-state, Carriage Return - Line Feed Signal	Rear Panel CR-CR/LF Switch via A6P1-16	Fig. 7-117/0D
LDDMS	Low active-state, Device Dependent Message Strobe Signal	Fig. 7-102/9D	Fig. 7-110/0F & Fig. 7-111/0E
LDIF	Low active-state, Difference Signal	Fig. 7-110/9B	Fig. 7-111/0C
LDISP	Low active-state, Display Signal	Fig. 7-110/9C	Fig. 7-116/0B & Fig. 7-111/0C
LDPON	Low active-state, Power-On Reset Signal	Fig. 7-110/9A	Fig. 7-117/0E & Fig. 7-111/0D

*The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

Table 7-3. Listing of Mnemonic Symbols used with A6 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
LEXTAZ	Low active-state, External Autozero Signal	Fig. 7-111/9A	A2 PCB via A6J1-9
LEXT DETA/ HEXT DETB	Low active-state, External Detector A/ High active-state, External Detector B	Fig. 7-111/9A	A2 PCB via A6J1-11
LEXT FILT1	Low active-state, External Filter 1 Signal	Fig. 7-111/9C	A2 PCB via A6J1-13
LEXT FILT2	Low active-state, External Filter 2 Signal	Fig. 7-111/9C	A2 PCB via A6J1-12
LEXT PLT	Low active-state, External Plot Signal	Fig. 7-111/9C	A2 PCB via A6J1-5
LEXT SWR	Low active-state, Switch Reference Signal	Fig. 7-111/9A	A2 PCB via A6J1-10
LFBR	Low active-state, First Byte Received Signal	Fig. 7-117/9G	Fig. 7-110/0F
LFM	Low active-state, Fast Mode Signal	Fig. 7-110/9D	Fig. 7-111/0F
LINTRS	Low active-state, Interrupt (SRQ Generator) Reset Signal	Fig. 7-102/9A	Fig. 7-110/0G
LIPON	Low active-state, Interface Power-On Reset Signal	Fig. 7-110/9B	Fig. 7-102/0H
LLSD1	Low active-state, Least Significant Digit Bit Weight 1 Signal	Fig. 7-116/9F	Fig. 7-117/0A
LLSD2	Low active-state, Least Significant Digit Bit Weight 2 Signal	Fig. 7-116/9F	Fig. 7-117/0A
LLSD4	Low active-state, Least Significant Digit Bit Weight 4 Signal	Fig. 7-116/9E	Fig. 7-117/0A
LLSD8	Low active-state, Least Significant Digit Bit Weight 8 Signal	Fig. 7-116/9E	Fig. 7-117/0A
LMSD1	Low active-state, Most Significant Digit Bit Weight 1 Signal	Fig. 7-116/9D	Fig. 7-117/0B

*The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

Table 7-3. Listing of Mnemonic Symbols used with A6 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
LMSD2	Low active-state, Most Significant Digit Bit Weight 2 Signal	Fig. 7-116/9D	Fig. 7-117/0B
LMSD4	Low active-state, Most Significant Digit Bit Weight 4 Signal	Fig. 7-116/9D	Fig. 7-117/0B
LMSD8	Low active-state, Most Significant Digit Bit Weight 8 Signal	Fig. 7-116/9D	Fig. 7-117/0B
LMYADR	Low active-state, My Address Signal	Fig. 7-101/8B	Fig. 7-102/0B
LNLSD1	Low active-state, Next Least Significant Digit Bit Weight 1 Signal	Fig. 7-116/9E	Fig. 7-117/0A
LNLSD2	Low active-state, Next Least Significant Digit Bit Weight 2 Signal	Fig. 7-116/9E	Fig. 7-117/0A
LNLSD4	Low active-state, Next Least Significant Digit Bit Weight 4 Signal	Fig. 7-116/9E	Fig. 7-117/0B
LNLSD8	Low active-state, Next Least Significant Digit Bit Weight 8 Signal	Fig. 7-116/9E	Fig. 7-117/0B
LNMSD1	Low active-state, Next Most Significant Digit Bit Weight 1 Signal	Fig. 7-116/9D	Fig. 7-117/0B
LNMSD2	Low active-state, Next Most Significant Digit Bit Weight 2 Signal	Fig. 7-116/9D	Fig. 7-117/0B
LNMSD4	Low active-state, Next Most Significant Digit Bit Weight 4 Signal	Fig. 7-116/9D	Fig. 7-117/0B
LNMSD8	Low active-state, Next Most Significant Digit Bit Weight 8 Signal	Fig. 7-116/9D	Fig. 7-117/0B
LNRFDI	Low active-state, Ready For Data Bus - Input Signal	U4-10 (Fig. 7-102/1G)	U24B-3 & U23B-3
LOG A,B	Log Amplifier A or B Input Signal	A2 PCB via A6J1-16	Fig. 7-111/0A
LOG A,B-R	Log Amplifier A or B-R Input Signal	A2 PCB via A6J1-15	Fig. 7-111/0A

*The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

Table 7-3. Listing of Mnemonic Symbols used with A6 PCB Circuits (continued)

MNEMONIC	DEFINITION	FROM*	TO*
LOG R	Log Amplifier R Input Signal	A2 PCB via A6J1-14	Fig. 7-111/0A
LP/HM	Low active-state, Plus/High active-state, Minus Signal	Fig. 7-116/9A	Fig. 7-117/0D
LRDERR	Low active-state, Read Error Signal	Fig. 7-110/9E	Fig. 7-111/0H
LREF	Low active-state, Reference Signal	Fig. 7-110/9C	Fig. 7-111/0A
LRFDO	Low active-state, Ready for Data - Output Signal	U21C-8 (Fig. 7-102/1F)	U4-11
LRFNB	Low active-state, Ready for New Byte Signal	Fig. 7-102/9F	Fig. 7-117/0G
LRLTM	Low active-state, Real Time Signal	A2 PCB via A6J1-17	Fig. 7-111/9A & Fig. 7-116/0D
LRMT	Low active-state, Remote Signal	Fig. 7-111/9D	A2 PCB via A6J1-4
LRSV	Low active-state, Request Service Bit Signal	Fig. 7-110/9D	Fig. 7-117/0E
LSPAS	Low active-state, Serial Poll Active State Signal	Fig. 7-102/8A	Fig. 7-110/0G & Fig. 7-117/0E
LTACS	Low active-state, Talker Active State Signal	Fig. 7-102/9B	Fig. 7-110/0E & Fig. 7-117/0F
LTACS + LSPAS	Low active-state, Talker Active State OR Low active-state, Serial Poll Active State Signal	U41C-8 (Fig. 7-102/8C)	U24A-2, U27A-2, U24B-5 & U24C-10

*The numeric/alpha characters (e.g., 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

P1
To GPIB Interface Connector Board

Pin No.	Mnemonic	Originates (Schematic Fig. No.)
1	S3	Figure 7-101/0A
2	S2	Figure 7-101/0A
3	S1	Figure 7-101/0B
4	Blank	N/A
5	D104	Figure 7-101/0E
6	D101	Figure 7-101/0E
7	D102	Figure 7-101/0E
8	D103	Figure 7-101/0E
9	EOI	Figure 7-102/0D
10	SRQ	Figure 7-102/0D
11	DAV	Figure 7-102/0G
12	ATN	Figure 7-102/0G
13	NRFD	Figure 7-102/0G
14	S4	Figure 7-101/0B
15	S5	Figure 7-101/0A
16	LCR HCR-LF	Figure 7-117/0D
17	Blank	N/A
18	D105	Figure 7-101/0D
19	D108	Figure 7-101/0C
20	D107	Figure 7-101/0C
21	D106	Figure 7-101/0D
22	Blank	N/A
23	Blank	N/A
24	NDAC	Figure 7-102/0G
25	IFC	Figure 7-102/0D
26	REN	Figure 7-102/0D

J1
To Connector A2J1
(Digital PCB)

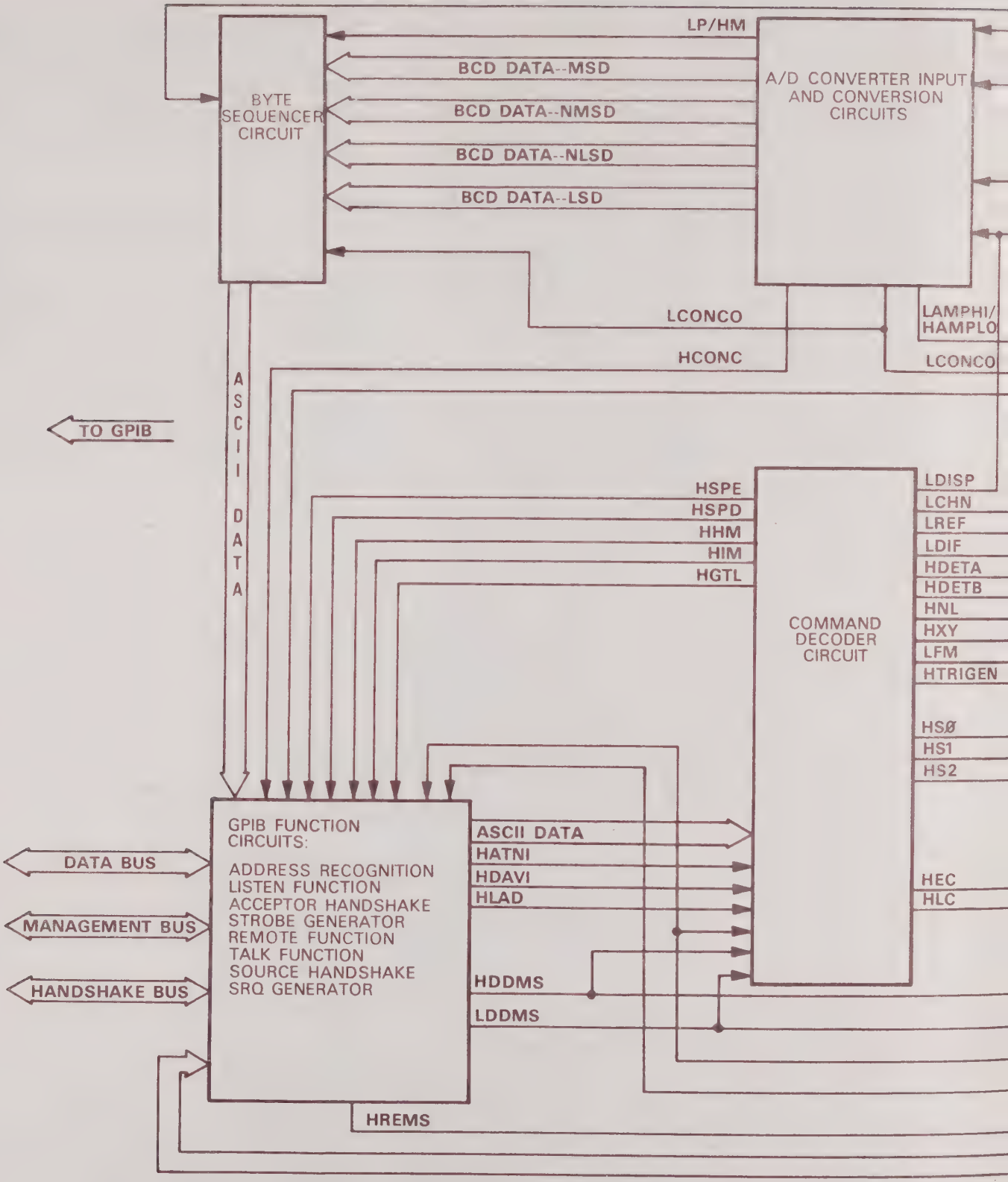
Pin No.	Mnemonic	Originates (Schematic Fig. No.)
1	EXT VERT	Figure 7-111/0A
2	HCG*	Figure 7-111/0G
3	+5V	Figure 7-111/0F
4	LRMT	Figure 7-111/9D
5	EXT PLT	Figure 7-111/9D
6	+18V	Figure 7-116/0G
7	-18V	Figure 7-116/0H
8	LCG**	Figure 7-116/0G
9	LEXTAZ	Figure 7-111/9A
10	LEXT SWR	Figure 7-111/8A
11	LEXT DETA/ HEXT DETB	Figure 7-111/8A
12	LEXT FILT2	Figure 7-111/9C
13	LEXT FILT1	Figure 7-111/9C
14	LOG R	Figure 7-111/0A
15	LOG A, B-R	Figure 7-111/0A
16	LOG A, B	Figure 7-111/0A
17	LRLTM	Figure 7-111/9B
18	HCG*	Figure 7-111/0G

*High Current Ground
**Low Current Ground

Figure 7-96. P1 and J1 Connector Pinout Charts

GPIB Subset	Function	Description
AH1	Acceptor Handshake	Complete Capability
SH1	Source Handshake	Complete Capability
T6	Talker	1. Basic Talker 2. Serial Poll 3. Unaddressed if MLA
TEØ	Talker With Address Extension	No Capability
L4	Listener	1. Basic Listener 2. Unaddressed if MTA
LEØ	Listener With Address Extension	No Capability
SR1	Service Request	Complete Capability
RL2	Remote/Local	No Local Lockout
PPØ	Parallel Poll	No Capability
DC1	Device Clear	Complete Capability
DTØ	Device Trigger	No Capability
CØ	Controller	No Capability

Figure 7-97. IEEE Standard 488 Subset Capability


BYTE SEQUENCER CIRCUIT
LP/HM
BCD DATA--MSD
BCD DATA--NMSD
BCD DATA--NLSD
BCD DATA--LSD
A/D CONVERTER INPUT AND CONVERSION CIRCUITS
LCONCO
HCONC
LAMPHI/ HAMPLO
LCONCO
ASCII DATA
TO GPIB
HSPE
HSPD
HHM
HIM
HGTL
COMMAND DECODER CIRCUIT
LDISP
LCHN
LREF
LDIF
HDETA
HDETB
HNL
HXY
LFM
HTRIGEN
HSØ
HS1
HS2
GPIB FUNCTION CIRCUITS:
ADDRESS RECOGNITION
LISTEN FUNCTION
ACCEPTOR HANDSHAKE
STROBE GENERATOR
REMOTE FUNCTION
TALK FUNCTION
SOURCE HANDSHAKE
SRQ GENERATOR
DATA BUS
MANAGEMENT BUS
HANDSHAKE BUS
ASCII DATA
HATNI
HDAVI
HLAD
HDDMS
LDDMS
HEC
HLC
HREMS

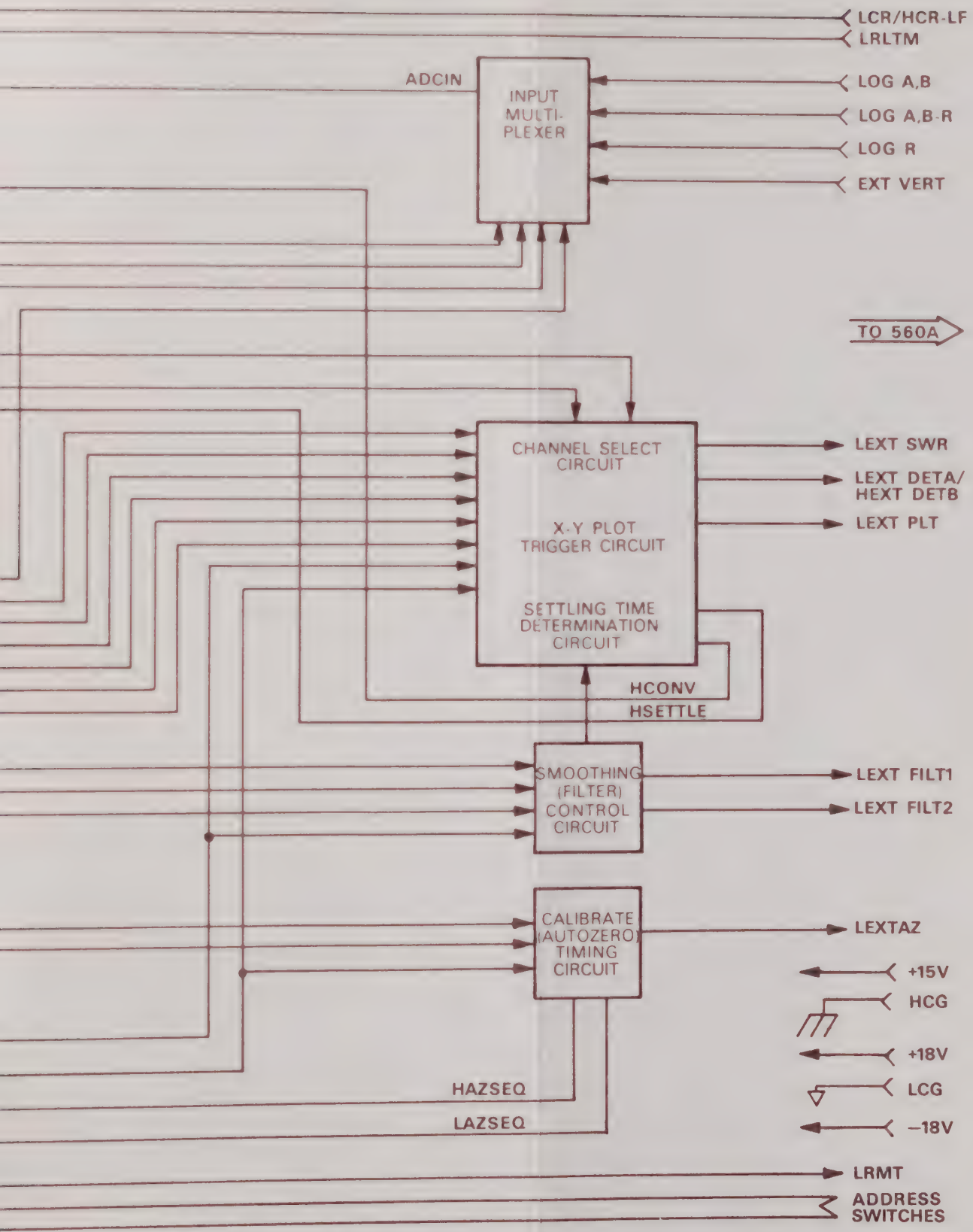


Figure 7-98. GPIB Interface (A6) PCB Overall Block Diagram

7-8.1 GPIB Transceiver Integrated Circuits

GPIB transceivers U1 and U2 (Figure 7-101), and U3 and U4 (Figure 7-102) provide for the bidirectional flow of data and commands between the GPIB and the 560A. Data and commands are input between pins 2-3, 7-6, 9-10, and 15-14. Data and commands are output between pins 4-2, 5-7, 11-9, and 13-14. Figure 7-99 shows the equivalent schematic of these integrated circuits.

7-8.2 Address Recognition Circuit

This circuit

- monitors the GPIB data bus.
- drives the LMYADR control line low when the 560A address is decoded.
- sets either the HLAG control line high when the DIO 6 and DIO 7 data lines are sensed to be in the listen configuration (DIO 6 LOW, DIO 7 HIGH), or sets the HTAG control line high when DIO 6 and DIO 7 are sensed to be in the talk configuration (DIO 6 HIGH, DIO 7 LOW).

The parts locator diagram for this circuit is shown in Figure 7-100, and the schematic diagram is shown in Figure 7-101. The address decoder consists of EX-OR gates U5A-U5D, U6, and NAND gate U7. The listen address group consists of AND gate U8A and inverter U9C. The talk address group consists of AND gate U8B and inverter U9A. Resistors RP2A thru RP2G are used to translate between TTL and CMOS logic levels. The GPIB data bus uses TTL logic and the A6 PCB uses CMOS logic.

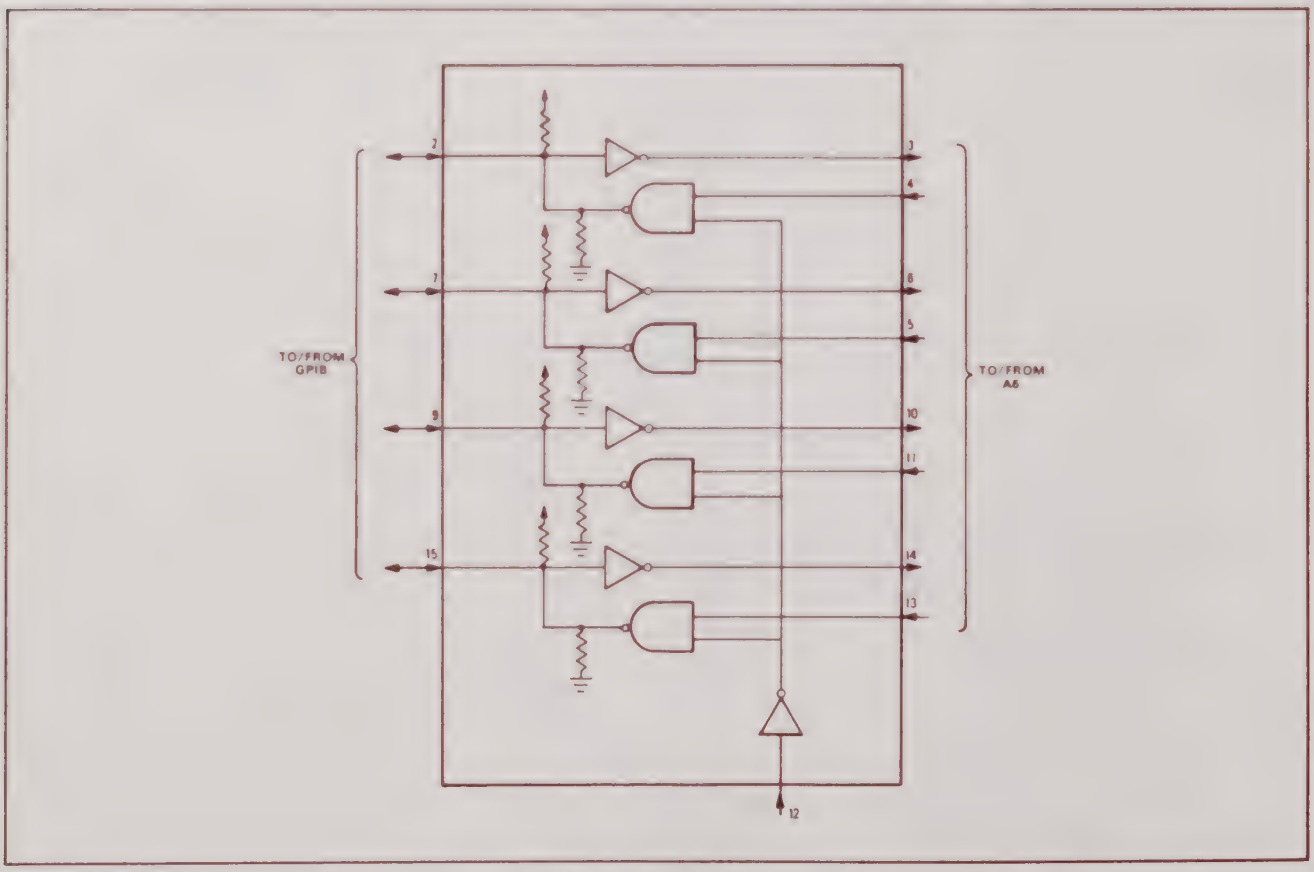
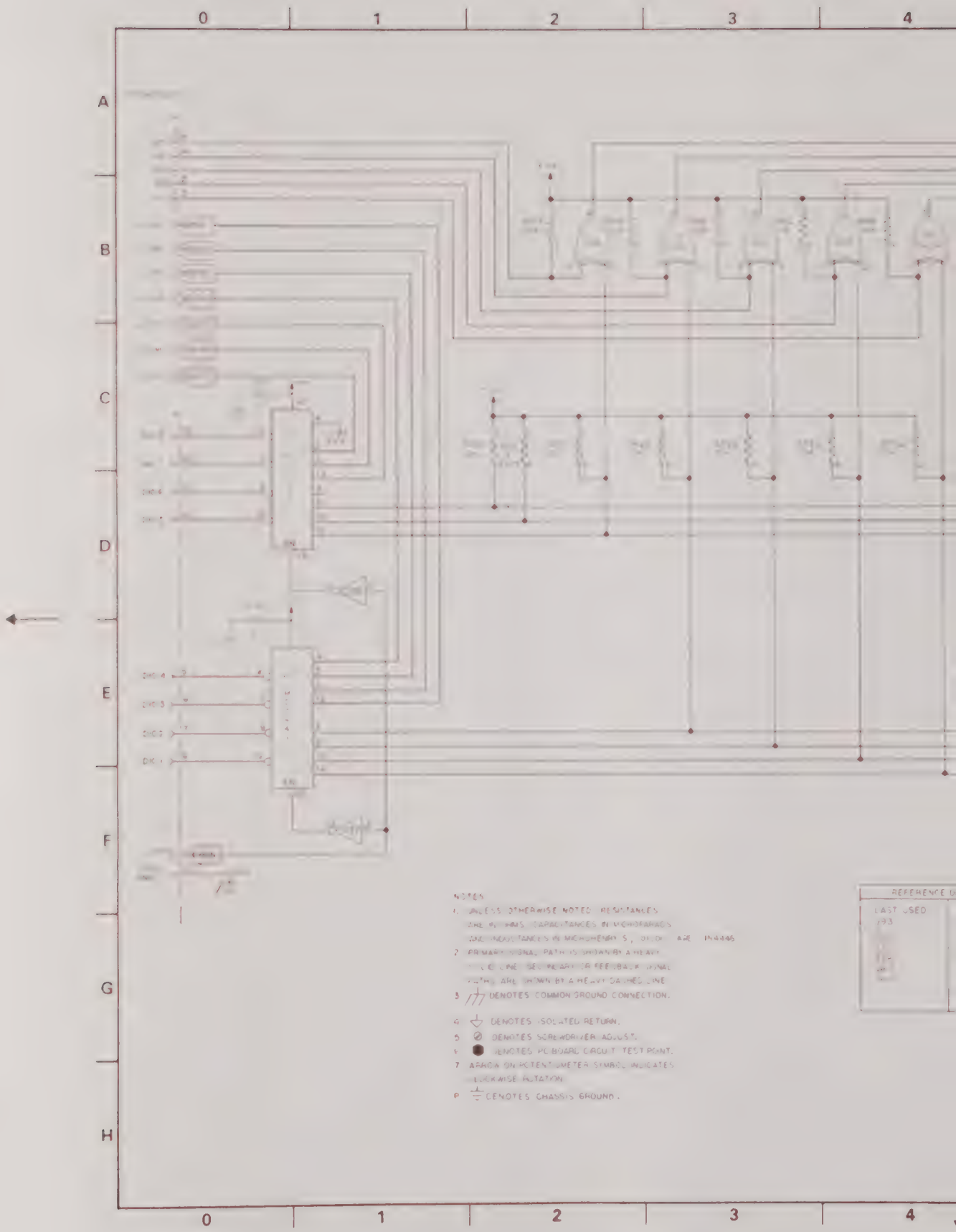


Figure 7-99. Integrated Circuits U1, U2, U3, and U4--Equivalent Circuit Schematic Diagram

Figure 7-100. GPIB Interface (A6) PCB Address Recognition Circuit Parts Locator Diagram



NOTES

1. UNLESS OTHERWISE NOTED: RESISTANCES ARE IN OHMS, CAPACITANCES IN MICROFARADS AND INDUCTANCES IN MICROHENRYS. DIODES ARE IN4446
2. PRIMARY SIGNAL PATH IS SHOWN BY A HEAVY LINE. SECONDARY OR FEEDBACK SIGNAL PATHS ARE SHOWN BY A HEAVY DASHED LINE.
3. DENOTES COMMON GROUND CONNECTION.
4. DENOTES ISOLATED RETURN.
5. DENOTES SCREWDRIVER ADJUST.
6. DENOTES PC BOARD CIRCUIT TEST POINT.
7. ARROW ON POTENTIOMETER SYMBOL INDICATES CLOCKWISE ROTATION.
8. DENOTES CHASSIS GROUND.

REFERENCE D

LAST USED
193

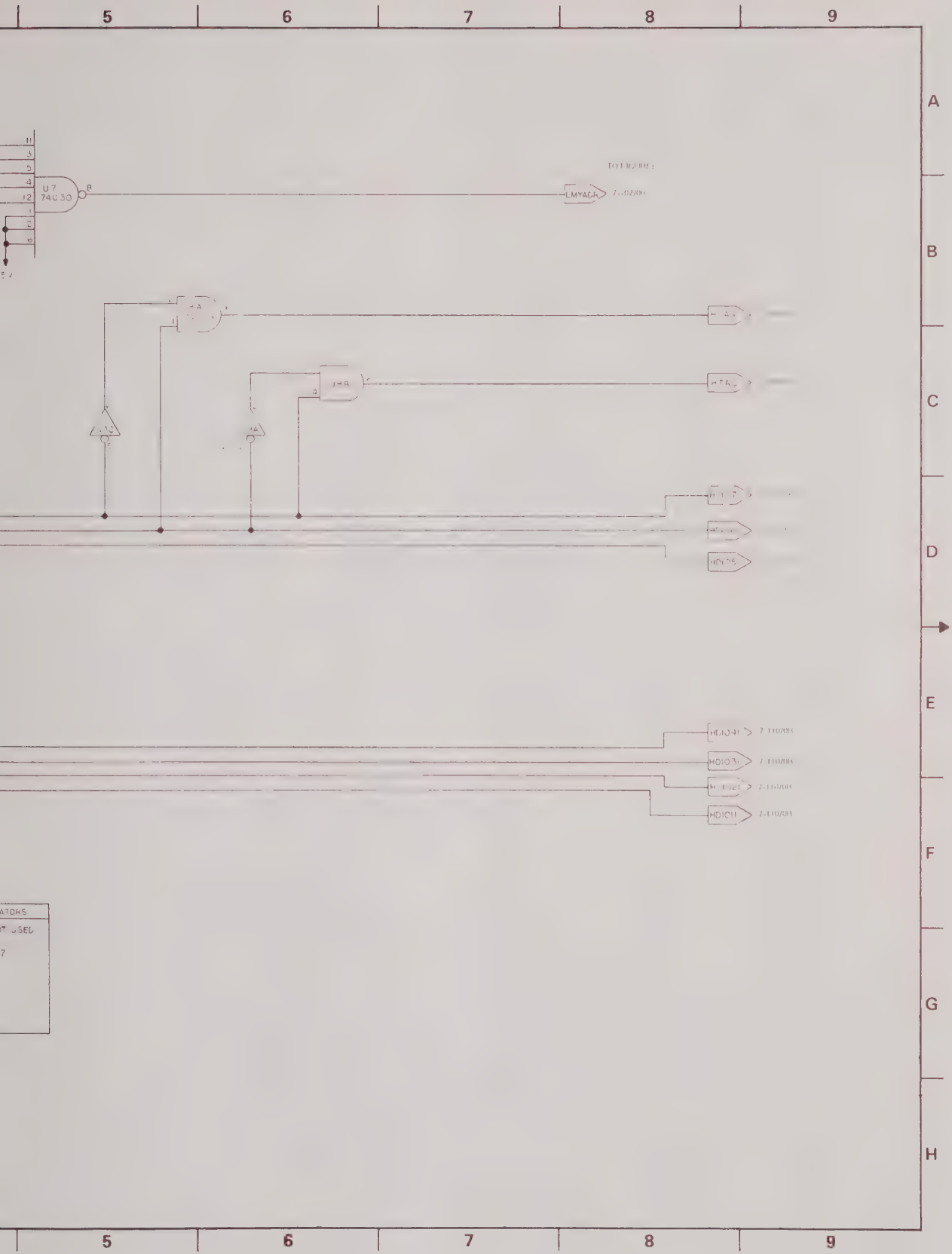


Figure 7-101. GPIB Interface (A6) PCB Address Recognition Circuit Schematic Diagram

Figure 7-100.

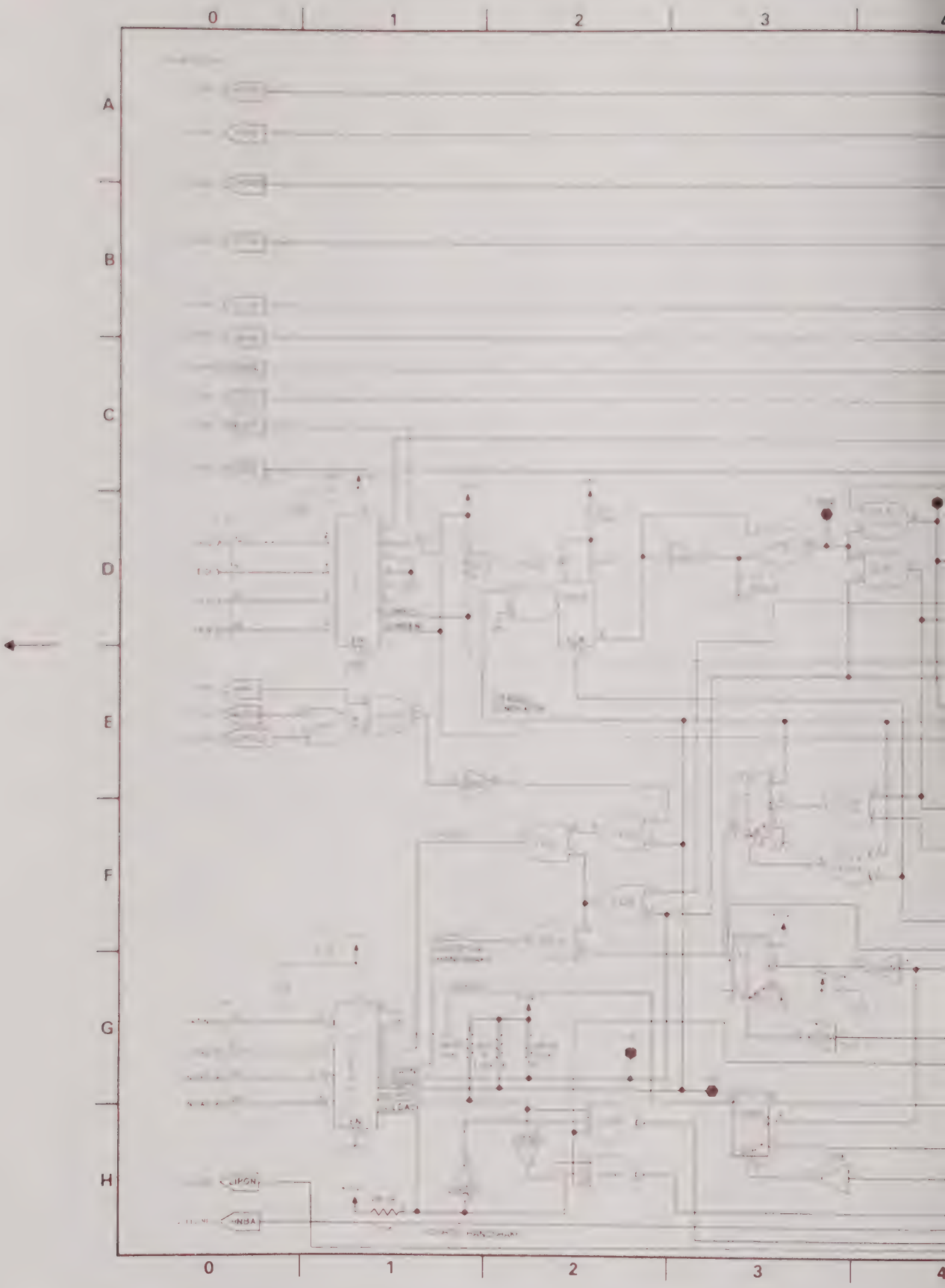
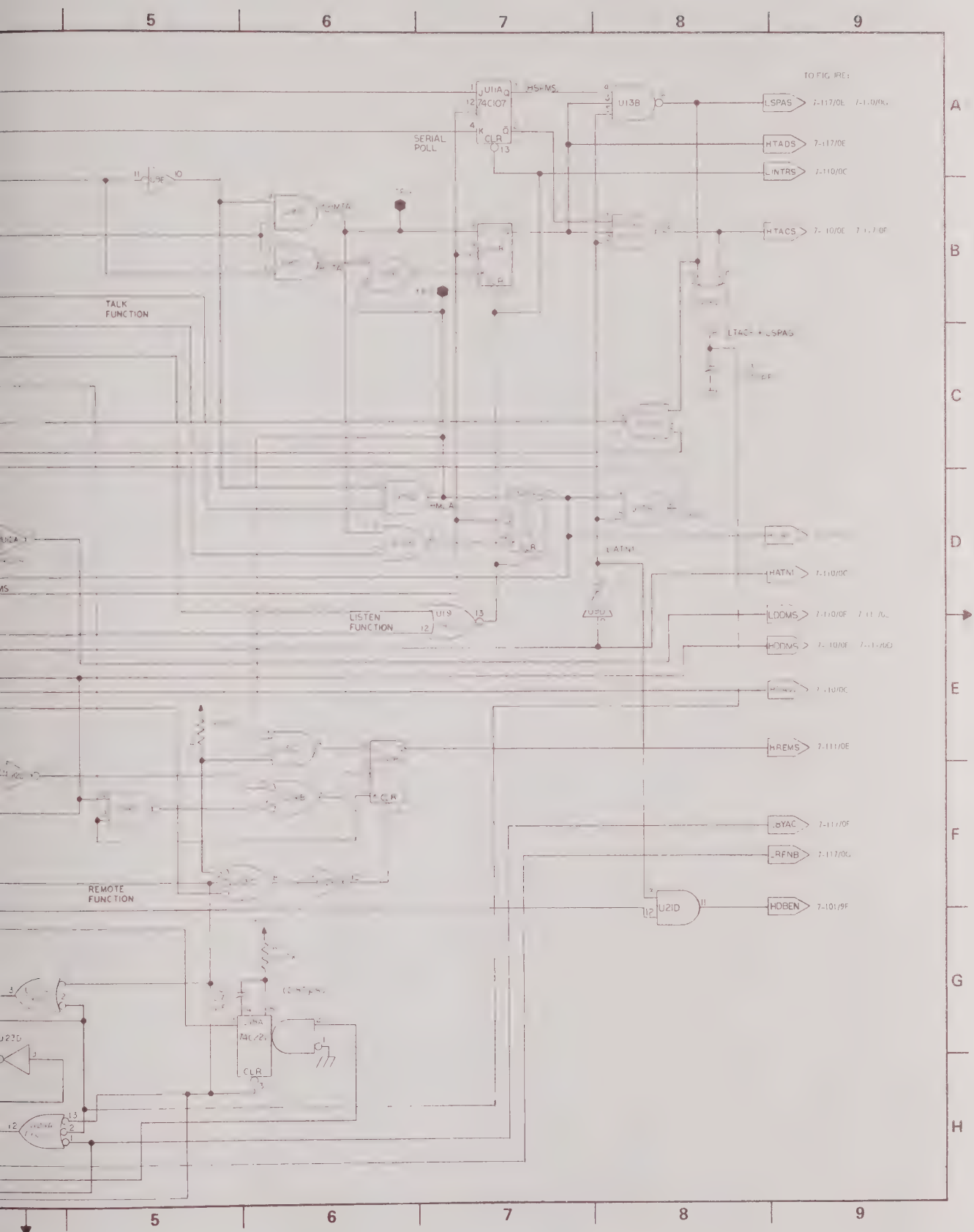


Figure 7-102. GPIB Interface (A6) PCB Listen Function, Acceptor Handshake, Strobe Generator, Remote Function, Talk Function, and Source Handshake Circuits Schematic Diagram


TO FIG. 1RE:
U11A
74C107
HSHMS
SERIAL POLL
U13B
LSPAS
HTADS
INTRS
HTACS
TALK FUNCTION
LATN
HATN
LDDMS
HDDMS
HREMS
SYAC
RFNB
U21D
HDBEN
LISTEN FUNCTION
REMOTE FUNCTION
CLR

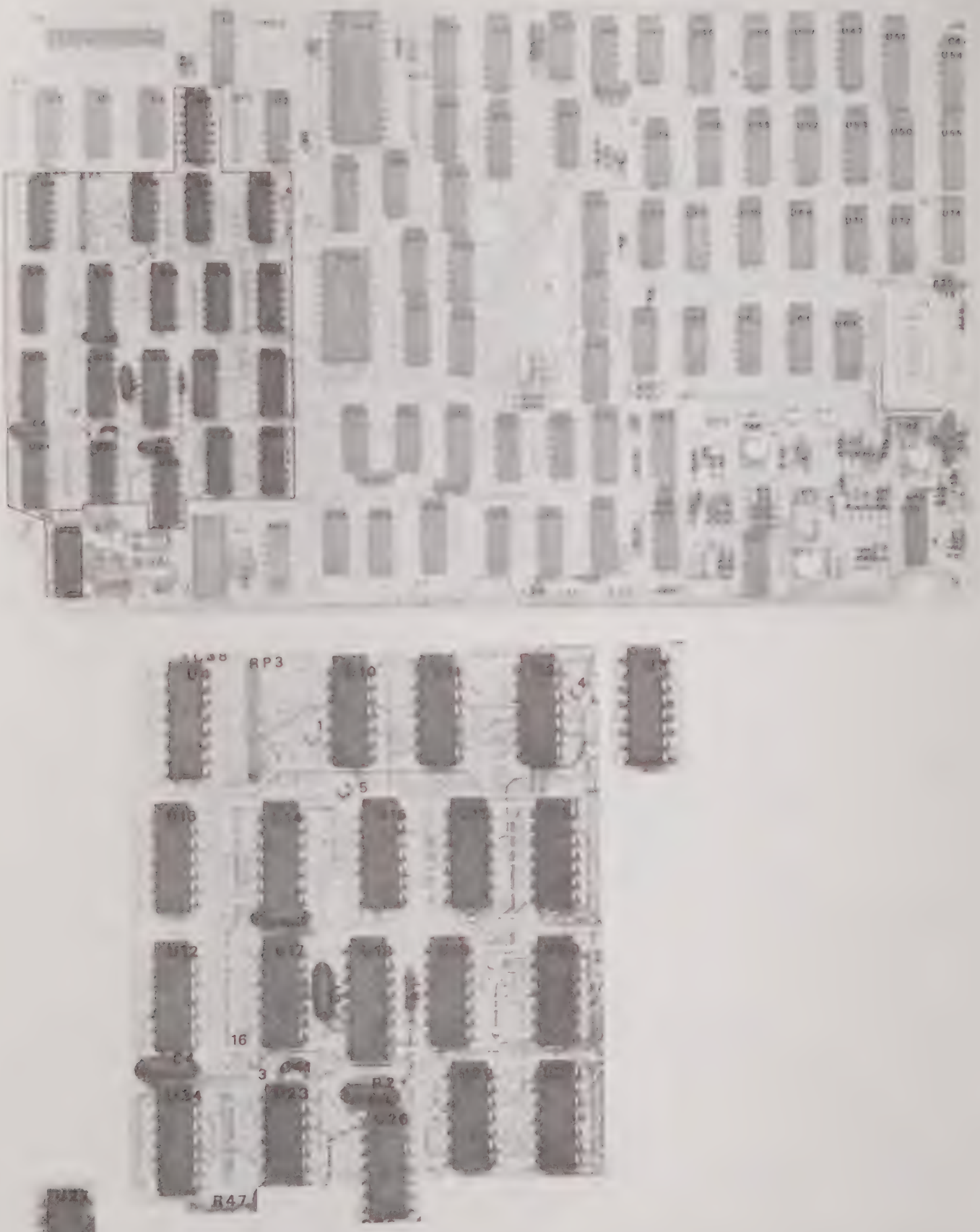


Figure 7-103. GPIB Interface (A6) PCB Listen Function, Acceptor Handshake, Strobe Generator, Remote Function, Talk Function, and Source Handshake Circuits Parts Locator Diagram

Figure 7-102.

7-8.3 Listen Function Circuit

This circuit controls the HLAD (listen addressed state) control line. The circuit latches HLAD

- HIGH when the address recognition circuit decodes the 560A listen address (LMYADR line LOW and HLAG line HIGH).
- LOW when either the address recognition circuit decodes the 560A talk address (LMYADR line LOW and HTAG line HIGH) or when the command decoder circuit decodes the 560A talk address unlisten command (HUNL line HIGH). HLAD is also latched LOW when the interface clear (IFC) message is received or when power is turned on.

The schematic for this circuit is shown in Figure 7-102, and the parts locator diagram is shown in Figure 7-103. The circuit consists of flip-flop U16A and gates U10B, U15D, and U15B.

7-8.4 Acceptor (Listener) Handshake Circuit

This circuit (1) monitors the ATN management, DAV handshake, and HLAD control lines, and (2) handshakes (communicates) with the talker when the logic states of ATN, HLAD and DAV indicate handshaking is required. The handshake cycle and the two conditions under which handshaking occurs are described below. The full schematic for this circuit is shown in Figure 7-102, the parts locator diagram is shown in Figure 7-103, and a simplified schematic is shown in Figure 7-104. Refer to Figure 7-104 for the following discussion.

a. The GPIB Acceptor Handshake Cycle. This cycle (Detail A, Figure 7-104) involves a three-part interchange between the talker (controller) and the listener (560A acceptor handshake circuit). The first part of the interchange occurs when the 560A circuit senses the DAV line is LOW. When DAV is sensed to be LOW, the 560A circuit drives the NRFD line LOW immediately, and, after a delay of 2μs, releases its hold on the NDAC line. Releasing the hold on NDAC allows it to go HIGH.

The second part of the handshake interchange occurs when the talker senses that the NRFD line is LOW and the NDAC line is HIGH. When NRFD is sense to be LOW and NDAC to be HIGH, the talker releases its hold on the DAV line. Releasing the hold on DAV allows it to go HIGH.

The third part of the handshake interchange occurs when the 560A circuit senses the DAV line is HIGH. When DAV is sensed to be HIGH, the 560A circuit drives the NDAC line TRUE immediately, and, unless the HHM control line (paragraph 7-8.10) and either the HAZSEQ (paragraph 7-8.13) or HSETTLE (paragraph 7-8.17) control lines are TRUE, releases its hold on the NRFD line. Releasing the hold on NRFD allows it to return HIGH, thus completing the acceptor handshake.

b. Two Conditions Under Which Handshake Occurs. Handshake occurs when the ATN control line is LOW or when the 560A is addressed to listen (HLAD line from listen function circuit HIGH). The first of these conditions occurs when interface messages such as device clear and serial poll enable are transmitted over the bus, or when bus instruments are being addressed to talk or listen. The second condition occurs when data transmissions are routinely transacted between the 560A and the talker.

The acceptor handshake circuit components that control the NRFD line are gates U21C, U22C and U22D. The components that control the NDAC line are flip-flop U20 and gates U21B and U22D. The 2 μs delay between the NRFD line going TRUE and the NDAC line going FALSE is provided by the DDM strobe generator (paragraph 7-8.5).

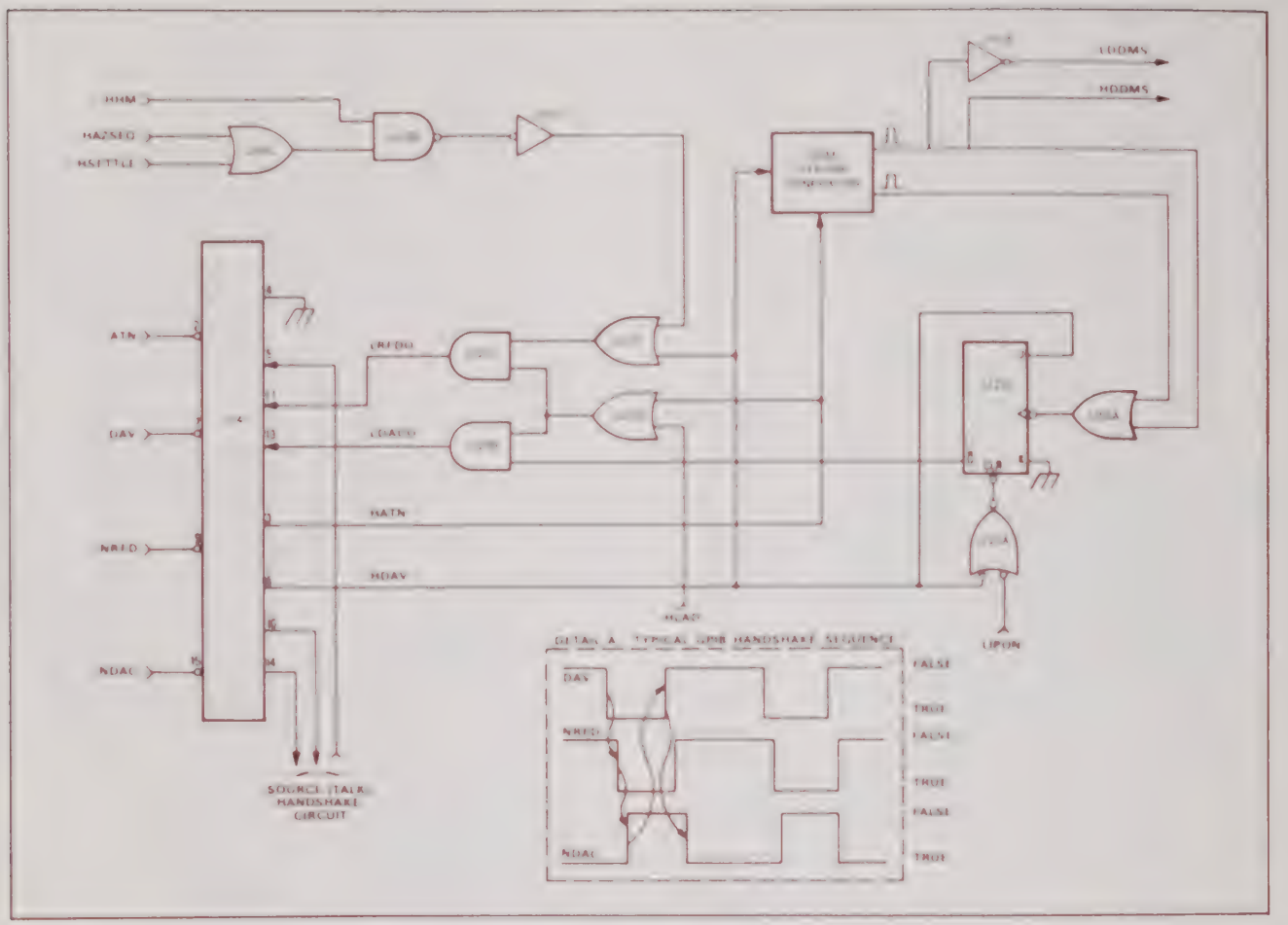


Figure 7-104. Acceptor Handshake Circuit, Simplified Schematic

7-8.5 DDM Strobe Generator Circuit

This circuit generates the device dependent message strobe (DDMS) pulse. A DDMS pulse is generated, following a delay of 2 μs, whenever a handshake cycle is initiated, i.e., when the DAV handshake line changes from HIGH to LOW. The schematic for this circuit is shown in Figure 7-102, and the parts locator diagram is shown in Figure 7-103.

The DDM strobe generator circuit is composed of one-shot multivibrator U18B, inverters U12A, U12B, AND gates U17A, U17B, and U17C. Circuit input is provided by the HDAV line from U4, pin 6. When this line changes from LOW to HIGH, U18B generates a negative-going 2 μs pulse from its $\overline{Q}$ output. At the end of 2 μs, when the U18B-$\overline{Q}$ pulse times out, AND gate U17B, inverter U12B, and capacitor C4 creates a short-duration, positive-going pulse. If the HATNI control line is HIGH, the HIMS pulse is gated out via U17C. If the 560A is addressed listen (HLACS line HIGH), the DDMS pulse is gated out via U17A.

7-8.6 Remote Function Circuit

This circuit controls the logic state of the HREMS control line. The schematic for the circuit is shown in Figure 7-102, and the parts locator diagram is shown in Figure 7-103. The remote function circuit is composed of flip-flop U16B, inverter U12E, gates U13C, U14B, U14D, and U15C.

The HREMS control line is set HIGH when the 560A is addressed to listen. The HREMS control line is driven LOW when any one of the following three conditions occur:

1. The HGTL control line is HIGH and a HIMS pulse is generated. HGTL goes HIGH when the command decoder (paragraph 7-8.10) decodes either the GTL (go to local) interface message or the RL (return to local) 560A command.
2. The REN management bus control line from the GPIB controller returns all bus instruments to local control.
3. The LIPON control line is LOW. This line goes LOW momentarily whenever the 560A power is turned on.

7-8.7 Talk Function Circuit

This circuit controls the logic state of the HTADS and the LTACS control lines. A third line, LINTRS, is also generated by this circuit. The schematic for the circuit is shown in Figure 7-102, and the parts locator diagram is shown in Figure 7-103. The talk function circuit is composed of the following components: flip-flop U11B, inverter U9E, gates U8C, U8D, U10D, and U13A.

The conditions under which the HTADS, LTACS, and LINTRS control lines are driven to their active states are as follows:

- HTADS: The HTADS control line is driven HIGH when the 560A talk address is decoded.
- LTACS: The LTACS control line is driven LOW when (1) the serial poll disable (SPD) command is decoded by the command decoder (HSPD line HIGH), (2) the 560A talk address is decoded by the address recognition circuit, and (3) the ATN management bus line is HIGH.
- LINTRS: The LINTRS control line is driven LOW either during power-on reset (HIPON line HIGH) or when the GPIB controller drives the IFC management bus control line LOW.

7-8.8 Source (Talk) Handshake Circuit

This circuit performs the following functions in the sequence listed. The circuit

- monitors the NRFD and NDAC handshake control lines. When NRFD is sensed to be HIGH and NDAC to be LOW, it
- puts the next data byte onto the bus, and, after an appropriate delay, drives the DAV handshake bus control line LOW. Then, when the listener (controller) communicates that the data byte is accepted (that is, when NRFD goes LOW and NDAC HIGH), the circuit
- takes the data byte off of the bus and drives the DAV line HIGH, thereby completing the source handshake.

The source (talk) handshake circuit has one additional two-part function. When the last data byte has been clocked onto the bus, the circuit's LBYAC control line causes (1) U56, the up-counter I.C. in the byte sequencer circuit, to be reset (i.e., load a count of zero) for the next data transaction, and (2) CR or LF to be taken off the GPIB.

The schematic for the circuit is shown in Figure 7-102, the parts locator diagram is shown in Figure 7-103, and a simplified schematic is shown in Figure 7-105.

The handshake bus condition that initiates a source handshake is shown by (1) in Figure 7-105. When this condition occurs, and if the 560A has been addressed to talk, the LRFNB control line is driven LOW. The LRFNB lines goes to flip-flop U26B, where it sets the J-input HIGH and the K-input LOW, and to 3-input NAND gate U43A. In normal operation the other two inputs of U43A are LOW; therefore, the application of the LRFNB signal causes the U43A output to go HIGH. The U43A output goes to U45C, where it drives the HNBA line HIGH. The HNBA signal clocks U56 and causes the first data byte (+/- sign) to be applied to bus transceivers U1 and U2 (not shown); it also triggers U18A, a 2.85μs one-shot multivibrator.

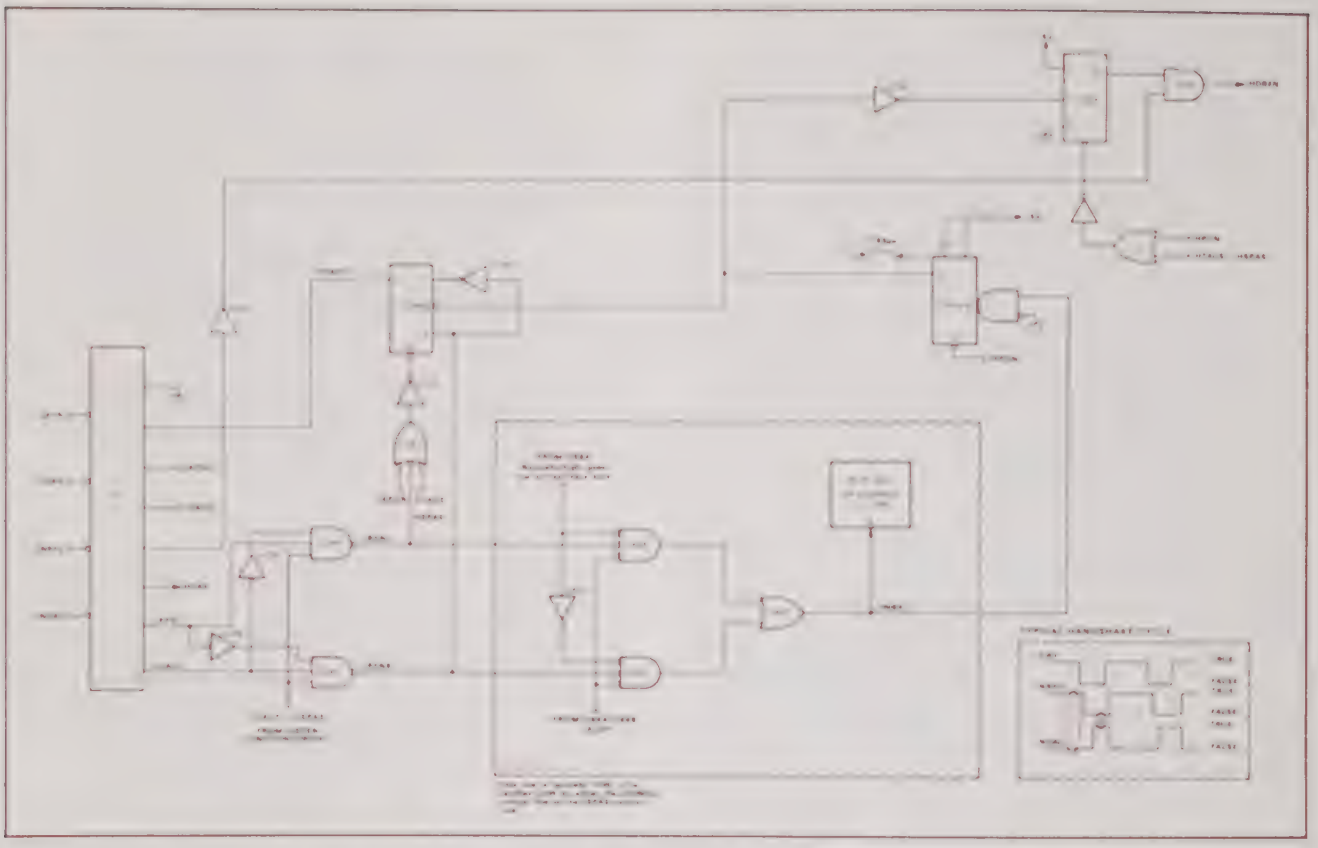


Figure 7-105. Source (Talk) Handshake Circuit, Simplified Schematic

The rising edge of the 2.85 μs pulse from U18A, after getting inverted by U23F, clocks the U26A-Q output HIGH. The U26A-Q output goes to U21D, where it is ANDed with the ATN management bus control line. When ATN is HIGH, the U26A-Q signal drives the HDBEN line HIGH. HDBEN enables U1 and U2 (Figure 7-101), which places the first data byte onto the GPIB. 2.85 μs later, the falling (trailing) edge of the U18A pulse clocks the U26B-Q output HIGH. The U26B-Q output drives the DAV handshake control line LOW. When DAV goes LOW the initial part of the source handshake cycle is complete.

The second part of the source handshake occurs when the listener (controller) communicates it has accepted the data byte. The listener communicates this by driving the NRFD line LOW and the NDAC line HIGH; the condition shown by (2) in Figure 7-105. This condition causes the LBYAC control line to be driven LOW. The LBYAC signal goes to NOR gate U24A and NAND gate U43B. At U43B the LBYAC signal stops. U43B is inhibited by the logic HIGH output of U58A. U43B remains inhibited until the last data byte (CR or LF) is clocked onto the bus by U56. The LBYAC signal is, however, gated through U24A. The signal is inverted by U23E and resets the U26B-Q output LOW. When LOW the U26B-Q output drives the DAV handshake line HIGH, whereby completing the source handshake.

The source handshake repeats either six or seven more times, once for each byte of data placed on the GPIB. The 560A provides either seven or eight bytes of data for each data transaction. These bytes include +/- sign byte, most-significant-digit (MSD) byte, next-most-significant-digit (NMSD) byte, decimal point byte, next-least-significant-digit (NLSD) byte, least-significant-digit (LSD) byte, and either a carriage return (CR) byte or both a carriage return and a line feed (LF) byte.

The secondary function of the source handshake circuit is two-fold. First, it resets up-counter U56, in the byte sequencer circuit, for the next data transaction. Second, it takes the last data byte off of the GPIB. These two actions occur sequentially when the last data byte, either CR or LF, is clocked onto the bus. The clocking of the last data byte onto the bus causes the output of U58A (Figure 7-117) to be driven LOW. (For the discussion on U58A, refer to paragraph 7-8.20). The LOW state of the U58A output enables both U56, pin 9, (load) and U43B, pin 12. With U43B so enabled, when the LBYAC line goes LOW (second part of the source handshake) it passes through U43B and drives the U45C output (HNBA line) HIGH. Again, the HNBA line serves two functions: (1) At this point in time, HNBA clocks U56 and causes zero to be loaded. This zero state prepares U56 for the next data transaction. The zero state also causes the CR or LF data byte to be taken off the internal A6 bus. (2) The HNBA line triggers U18A. Now, only one edge of the U18A pulse is used. The rising (leading) edge of this pulse, as previously described, clocks the U26A-Q output HIGH and causes the last data byte to be taken off the GPIB data bus.

7-8.9 SRQ Generator Circuit

This circuit sequentially performs three functions, which interrelate to provide the interrupt mode capability.

1. It sets the request service bit, creates the status byte, and drives the SRQ management bus control line.
2. It checks the status of the HSPMS (serial poll enable message received signal), HTADS (talker active state), and LATNI (attention-input) control lines.
3. If the three lines checked in 2., above, are HIGH (which indicates the serial poll message has been received, the 560A is currently addressed to talk and the ATN management bus line is HIGH); the circuit then places the request service byte onto the GPIB.

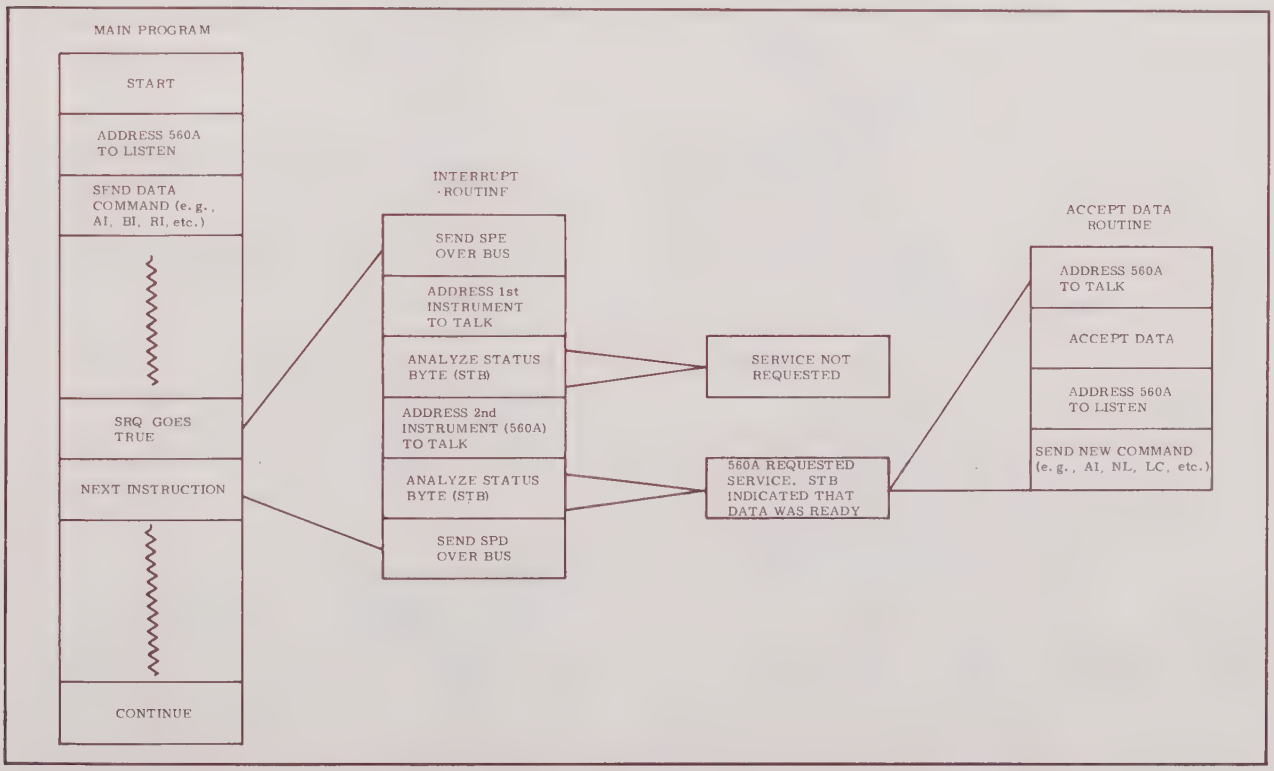

MAIN PROGRAM
START
ADDRESS 560A TO LISTEN
SEND DATA COMMAND (e.g., AI, BI, RI, etc.)
SRQ GOES TRUE
NEXT INSTRUCTION
CONTINUE
INTERRUPT ROUTINE
SEND SPE OVER BUS
ADDRESS 1st INSTRUMENT TO TALK
ANALYZE STATUS BYTE (STB)
ADDRESS 2nd INSTRUMENT (560A) TO TALK
ANALYZE STATUS BYTE (STB)
SEND SPD OVER BUS
SERVICE NOT REQUESTED
560A REQUESTED SERVICE. STB INDICATED THAT DATA WAS READY
ACCEPT DATA ROUTINE
ADDRESS 560A TO TALK
ACCEPT DATA
ADDRESS 560A TO LISTEN
SEND NEW COMMAND (e.g., AI, NL, LC, etc.)

Figure 7-106. Relationship of Interrupt Routine to Main Program

To understand the SRQ generator circuitry, it is necessary to understand the interrupt mode and the relationship between the SRQ, SPE, and SPD messages. Paragraph 3-7.1d2 provides a description of the interrupt mode and tells why the mode is used and how the mode is entered into. Paragraph 3-7.1d2 also provides a description of the request service bit and status byte. Figure 7-106 shows the relationship between the SRQ, SPE, and SPD messages. This figure also shows how the interrupt routine fits into the controller's main program.

A simplified schematic of the SRQ generator circuit is shown in Figure 7-107, a parts locator diagram is shown in Figure 7-109, and the full schematic is shown in Figure 7-110. Refer to the simplified schematic for the following circuit discussion.

The first circuit function is that of setting the request service (RSV) bit, creating the status byte (STB), and driving the SRQ management line. This function uses flip-flops U41A, U41B, U42; gates U39A, U40B, U40D, U38A, U15A; inverters U63E, U72B, U37E; and the SRQ output pins of bus transceiver U3.

The flip-flop and gating/inverter circuit consisting of U41A, U41B, U42, U40B, U40D, U63E, and U72B create the two least significant STB bits. These two bits are either: HSTB=1, HSTB2=0; HSTB1=0, HSTB2=1; or HSTB1=1, HSTB2=1. The first combination of bits (HSTB1=1, HSTB2=0) indicate that the A/D data conversion is complete and the data is ready. The second combination of bits (HSTB1=0, HSTB2=1) indicates the log amplifier autozero calibration sequence is complete. The third combination of bits (HSTB1=1, HSTB2=1) indicates an illegal command sequence has been programmed. (An illegal command sequence is when a data command such as AI, BI, RI, AR, BR, or NL has been programmed so close to an LC or EC calibrate command that the data and calibrate command functions overlap in time.) The creation of the two STB bits is described on the next page.

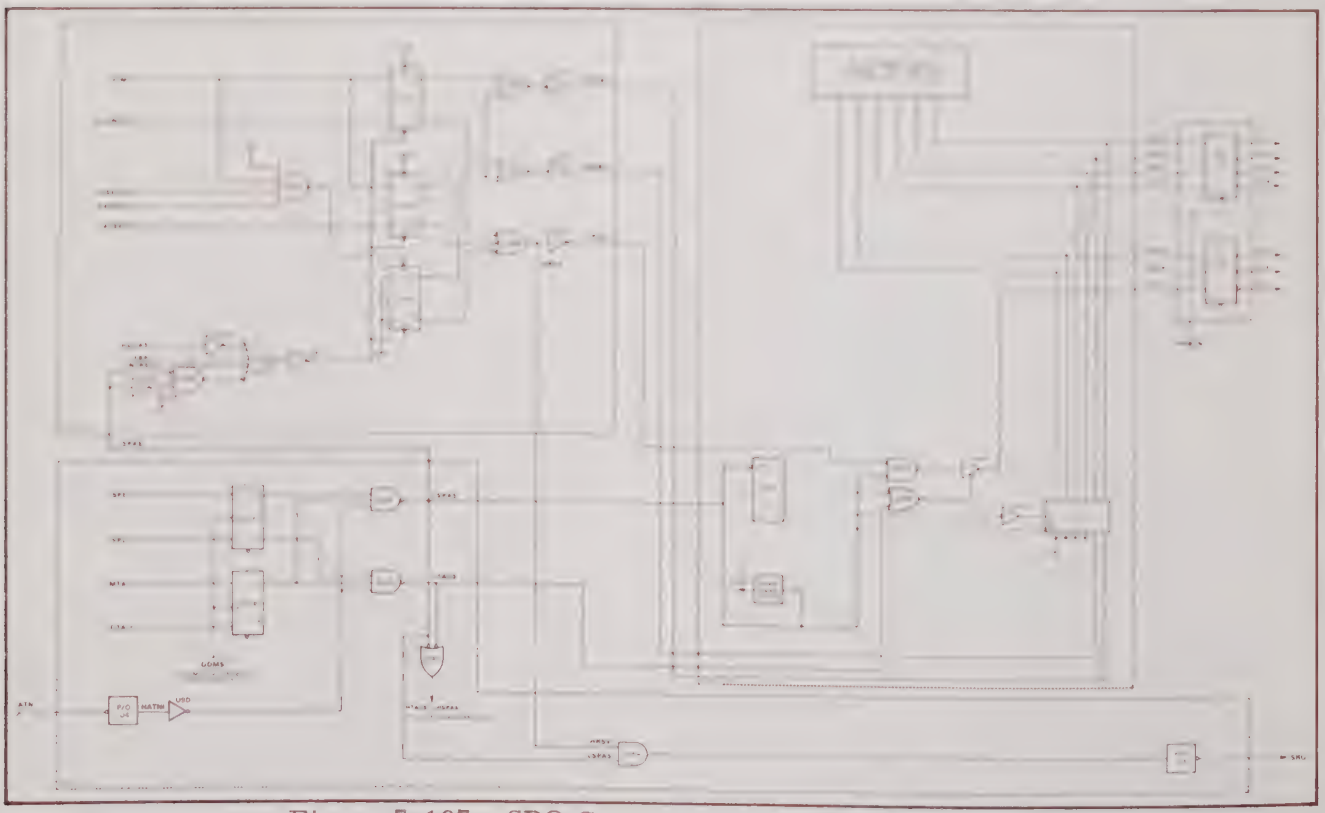


Figure 7-107. SRQ Generator, Simplified Schematic

The D inputs of U41A and U41B are driven HIGH by the HIM signal from the command decoder. When the last data byte has been converted by the A/D converter, the LOW to HIGH transition of the HCONC line clocks the U41A-Q output HIGH. This sets the HSTB1 line HIGH. When the autozero calibration sequence is complete, the LOW to HIGH transition of the LAZSEQ line clocks the U41B-Q output HIGH. This sets the HSTB2 line HIGH. When an illegal command sequence has been programmed, the HIGH states of HSETTLE, and HAZSEQ are ANDed with the HIGH state of HIM. The resulting LOW state of the U39A output presets the U42-Q output HIGH. The HIGH state of the U42-Q output sets both HSTB1 and HSTB2 HIGH.

The RSV bit is set coincident with the creation of the two STB bits. When either or both of these bits are HIGH, the RSV bit is set HIGH by U38A. The RSV bit (HRSV signal line) is then applied to U15A, where it is ANDed with the LSPAS control line. When the LSPAS line is HIGH, which indicates the 560A is not currently engaged in a serial poll, the SRQ management control line is driven LOW.

The second circuit function is that of checking the status of the HSPMS, HTADS, and LATNI control lines. This function uses NAND gate U13B. The HSPE, HTADS, and LATNI lines provide the three inputs for U13B. If the serial poll enable message has been received, the HSPMS line is HIGH; if the 560A is currently addressed to talk, the HTADS line is HIGH; and if the ATN bus line is HIGH, the LATNI line is HIGH. When all three of these line are HIGH concurrently, the U13B output line, LSPAS, goes LOW.

The third function is that of placing the request service bit and status byte on the bus. This function uses gates U45D, U58B, tri-state buffer-inverter U46E, inverter U36F, tri-state octal flip-flop U51, and the data output pins of bus transceivers U1 and U2.

The request service bit is set by the gating action of U58B and U45D. The status byte is gated by U51. U51 is both enabled and clocked by the LSPAS control line. The request service bit and status byte are then applied to U1 and U2. In a parallel circuit action, the LOW state of the LSPAS control line drives the output of the U44A/U44B latch circuit LOW. The LOW state of this latch enables U43A, pin 2. NAND gate U58A, via inverter U46A, enables U43A, pin 8. With U43A thus enabled the LRFNB control line causes bus transceivers U1 and U2 to become enabled (paragraph 7-8.8). When U1 and U2 are enabled, the RSV and STB are placed onto the GPIB data bus.

A collateral function of the SRQ generator circuit is resetting flip-flops U41A, U41B, and U42 when the request service bit and status byte have served their purpose. The circuit that resets the flip-flops consists of gates U35A, U39B, and inverters U36A, U36B, U36C. The flip-flop circuit can be reset in any of the following four ways.

1. The LSPAS line goes HIGH. LSPAS goes HIGH at the end of the serial poll active state. The serial poll active state ends when the controller drives the ATN line LOW and puts the next interface message (serial poll disable) on the bus.

2. The HDCAS line goes HIGH. HDCAS goes HIGH when either the device clear (DCL) of the selected device clear (SDC) interface message is decoded by the command decoder.

3. The LINTRS line goes LOW. LINTRS goes LOW either when the IFC (interface clear) management bus control line goes LOW or when the A6 PCB power-on reset circuit is activated (HDPON line goes HIGH).

4. The LFBR line goes LOW. LFBR goes LOW when the byte sequencer circuit sequences the first data byte (+/- sign) onto the internal A6 bus.

7-8.10 Command Decoder Circuit

This circuit decodes the GPIB data bus. The circuit consists of a programmable logic array (PLA) with associated components. Figure 7-108 is a simplified schematic of this circuit; Table 7-4 is a listing of the PLA program. A parts locator diagram is shown in Figure 7-109, and the full schematic is shown in Figure 7-110.

Figure 7-108 shows the arrangement of circuit components. The primary decoding device in this circuit is the PLA. As used in the 560A, the PLA is similar to a read only memory (ROM) device in that it has the capability to permanently store binary data. Like the ROM, the PLA stores data in 8-bit binary patterns. The PLA is different from the ROM, however, in the way the stored data is accessed. In a ROM, each 8-bit binary pattern has its own unique address. In the PLA, each 8-bit pattern can have any number of addresses. This is because any number of PLA address lines can be declared "don't care" lines. In other words, many addresses are mapped to the location of any given 8-bit binary pattern.

The difference in accessing between a ROM and a PLA is important. This difference means the PLA has a smaller number of different, unique output states for a larger number of different, unique input states (addresses) than a ROM has. For example, the 82S101N PLA used in the 560A is programmed to have 39 output states. Even though only 39 output states (8-bit binary patterns) are available, these 39 output states are accessed by approximately 750 different addresses (input states).

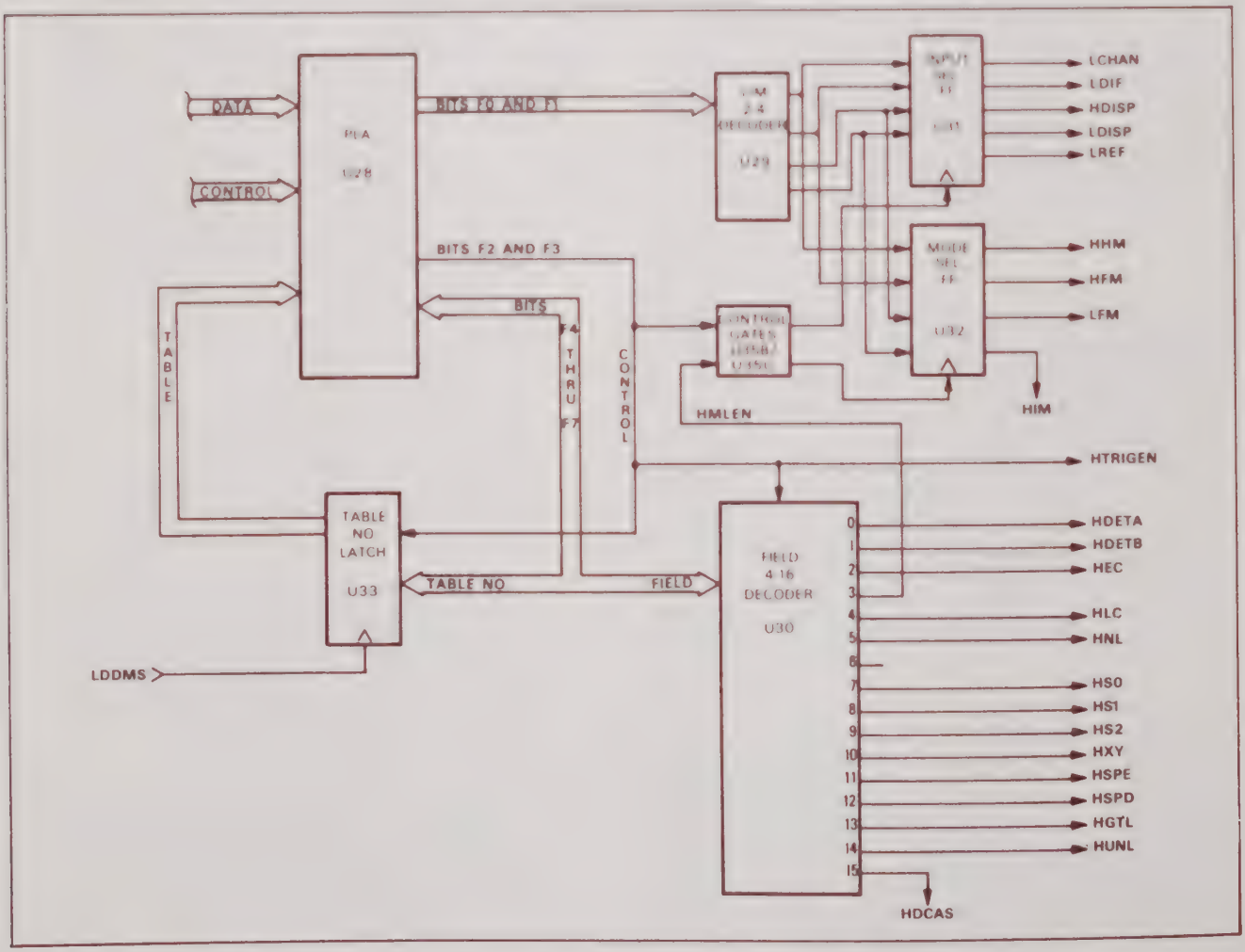


Figure 7-108. Command Decoder Circuit, Simplified Schematic

To decode the GPIB data bus, 33 of the 39 programmed bit-patterns are organized into 13 tables (Table 7-4) and used to decode the 20 two-byte (two-letter) 560A commands. The remaining 6 bit-patterns are used independently to decode the 6 one-byte interface message commands. These interface message commands are SPE (serial poll enable), SPD (serial poll disable), GTL (go to local), UNL (unlisten), DCL (device clear), and SDC (selected device clear).

Table 7-4. PLA Program Listing

INPUT																		OUTPUT											
TABLE NO. LSB					CONTROL				LSB	ASCII DATA							COMMAND LETTER	TN/EC *** LSB				CON-TROL		IS/MC ** LSB		1st LTR.
I 15	I 14	I 13	I 12		I 11	I 10	I 9	I 8	I 7	I 6	I 5	I 4	I 3	I 2	I 1	I 0		F 7	F 6	F 5	F 4	F 3	F 2	F 1	F 0	
0	0	0	0		* -	-	1	1	0	1	0	0	0	0	-	1	A	1	0	0	0	0	0	0	0	A
0	0	0	0		-	-	1	1	0	0	1	0	0	0	-	1	B	0	1	0	0	0	0	0	0	
0	0	0	0		-	-	1	1	0	1	0	1	0	0	-	1	E	1	1	0	0	0	0	0	0	
0	0	0	0		-	-	1	1	0	1	0	0	1	0	-	1	I	0	0	1	0	0	0	0	0	
0	0	0	0		-	-	1	1	0	0	0	1	1	0	-	1	L	1	0	1	0	0	0	0	0	
0	0	0	0		-	-	1	1	0	0	1	1	1	0	-	1	N	0	1	1	0	0	0	0	0	
0	0	0	0		-	-	1	1	0	0	1	0	0	1	-	1	R	1	1	1	0	0	0	0	0	
0	0	0	0		-	-	1	1	0	1	1	0	0	1	-	1	S	0	0	0	1	0	0	0	0	
0	0	0	0		-	-	1	1	0	0	0	0	1	1	-	1	X	1	0	0	1	0	0	0	0	
0	0	0	0		-	-	1	1	0	0	0	0	1	0	-	1	H	0	1	0	1	0	0	0	0	
0	0	0	0		-	-	1	1	0	0	1	1	0	0	-	1	F	1	1	0	1	0	0	0	0	
0	0	0	0		-	-	1	1	0	1	1	0	0	0	-	1	C	0	0	1	1	0	0	0	0	
1	0	0	0		-	-	1	1	0	1	0	0	1	0	-	1	I	0	0	0	0	1	1	0	0	
1	0	0	0		-	-	1	1	0	0	1	0	0	1	-	1	R	0	0	0	0	1	1	1	0	
1	0	0	0		-	-	1	1	0	0	0	1	0	0	-	1	D	0	0	0	0	1	1	0	1	
0	1	0	0		-	-	1	1	0	1	0	0	1	0	-	1	I	1	0	0	0	1	1	0	0	B
0	1	0	0		-	-	1	1	0	0	1	0	0	1	-	1	R	1	0	0	0	1	1	1	0	
0	1	0	0		-	-	1	1	0	0	0	1	0	0	-	1	D	1	0	0	0	1	1	0	1	
1	1	0	0		-	-	1	1	0	1	1	0	0	0	-	1	C	0	1	0	0	1	0	0	0	E
0	0	1	0		-	-	1	1	0	1	0	1	1	0	-	1	M	1	1	0	0	1	0	1	0	I
1	0	1	0		-	-	1	1	0	1	1	0	0	0	-	1	C	0	0	1	0	1	0	0	0	L
0	1	1	0		-	-	1	1	0	0	0	1	1	0	-	1	L	1	0	1	0	1	1	0	0	N
1	1	1	0		-	-	1	1	0	1	0	0	1	0	-	1	I	0	0	0	0	0	1	1	1	R
1	1	1	0		-	-	1	1	0	0	0	1	1	0	-	1	L	1	0	1	1	1	0	0	0	
0	0	0	1		0	-	1	1	0	0	0	0	0	1	1	0	ø	1	1	1	0	1	0	0	0	S
0	0	0	1		0	-	1	1	0	1	1	1	1	0	0	1	O	1	1	1	0	1	0	0	0	
0	0	0	1		0	-	1	1	0	1	0	0	0	1	1	0	1	0	0	0	1	1	0	0	0	
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1	0	0	1		-	-	1	1	0	1	0	0	1	1	-	1	Y	0	1	0	1	1	0	0	0	X
0	1	0	1		-	-	1	1	0	1	0	1	1	0	-	1	M	1	1	0	0	1	0	0	0	H
1	1	0	1		0	-	1	1	0	1	0	1	1	0	-	1	M	1	1	0	0	1	0	0	1	F
0	0	1	1		-	-	1	1	0	1	0	0	0	0	-	1	A	0	0	0	0	1	0	0	0	
0	0	1	1		-	-	1	1	0	0	1	0	0	0	-	1	B	1	0	0	0	1	0	0	0	C
SINGLE-ENTRY COMMANDS																													
-	-	-	-		-	-	-	1	1	0	0	0	1	1	0	0	SPE	1	1	0	1	1	0	0	0	
-	-	-	-		-	-	-	1	1	1	0	0	1	1	0	0	SPD	0	0	1	1	1	0	0	0	
-	-	-	-		-	-	1	1	1	1	0	0	0	0	0	0	GTL	1	0	1	1	1	0	0	0	
-	-	-	-		-	-	1	1	1	1	1	1	1	1	1	0	UNL	0	1	1	1	1	0	0	0	
-	-	-	-		-	-	-	1	1	0	0	1	0	1	0	0	DCL	1	1	1	1	1	0	0	0	
-	-	-	-		-	-	1	1	1	0	0	1	0	0	0	0	SDC	1	1	1	1	1	0	0	0	

*** TN/EC - Table Number or Execute Code

** IS/MC - Input Selector or Mode Control

* Dash (-) indicates "Don't Care" input.

To call up a specific bit-pattern at the output of the PLA, the 16 PLA input lines form an address word. This address word has three data components: an ASCII data component, a control data component, and a table-number data component. If either the control or the table-number data components are incorrect for the command letter being decoded, the address word will be invalid; a bit pattern of all 0's will be produced at the PLA output.

For example, assume the letter A is present on the ASCII data-input lines. In order for this A to be considered a valid command character,

1. the HDAV input line (I_8) must be HIGH,
2. the HLAD input line (I_9) must be HIGH,
3. the HATNI input line (I_7) must be LOW, and
4. the table-number data-input lines must indicate either table number 0 (0000) if the A is the first letter in the command, or table number 12 (1100) if A is the second letter in the command.

The PLA output lines are also organized with three data components: table number/execution code (TN/EC), control, and input selector or mode control (IS/MC). The TN/EC data component indicates either the table number or execution code number. If the command character just decoded was the first letter in the 560A command, then the TN/EC data component indicates the number of the table of which the second letter should be a member. If the character just decoded, however, is either (1) the second letter in the 560A command or (2) any one of the interface messages, then the TN/EC data component indicates the execution code of the command. This execution code is decoded by 4-line to 16-line decoder U30; depending on the number decoded, one of the U30 output lines is set HIGH.

The control data component consists of two control lines: HDCEN and HTRIGEN. The HDCEN control line either inhibits decoder U30 and enables AND gates U34A thru U34D (Figure 7-110), or enables U30 and inhibits U34A thru U34D. When LOW, the HDCEN line inhibits U30 and enables U34A thru U34D. Gates U34A thru U34D supply table-number data to the PLA. Conversely, when HIGH, the HDCEN line enables U30 and inhibits U34A thru U34D. When inhibited, U34A thru U34D supply 0000 to quad-D flip-flop U33. The HTRIGEN control line enables NAND gate U35B and allows the HDDMS pulse to clock the four input selector flip-flops of U31. In addition, the HTRIGEN control line initiates the data-taking sequence by triggering the Settling Time Determination circuit (paragraph 7-8.17).

The input selector or mode control (IS/MC) data component is a binary number that indicates what input-selector input has been selected (paragraph 7-8.16) or what mode has been selected. The IS/MC data component sets up the D_A, D_B, D_C, or D_D inputs to both the input selector and the mode control flip-flops. If an input command such as AI, BI, RI, AR, BR, AD, BD, or NL is decoded, NAND gate U35B is enable by the HTRIGEN control line. If a mode command such as HM, IM, or FM is decoded, NAND gate U35C is enable by the "3" output from U30, pin 8.

To illustrate the complete decoding process, assume the command AI is sent over the bus. Upon decoding the letter A, the following occur:

1. The TN/EC data component is configured such that the binary code for table number 1 (0001) is applied to AND gates U34A thru U34D.
2. The control data component is configured such that the HDCEN control line enables AND gates U34A thru U34D; this places the table-number data on the D_A thru D_D inputs of flip-flop U33. U33 is clocked by the LDDMS pulse, and the table-number data is applied to the I_{12} thru I_{15} inputs of the PLA.

Upon decoding the letter I, the following actions occur:

1. The TN/EC data component is configured such that binary execution code 0 (0000) is applied to the A thru D inputs of U30.

2. The IS/MC data component is configured such that the binary code for the number 1 is applied to the A and B inputs of U29. U29 decodes this number and sets its 0 output line HIGH. The U29-0 line provides the D_A input for U31.

3. The control data component is configured such that the HDCEN control line enables decoder U30, and the NTRIGEN control line enables NAND gate U35B. (Note that U34A-U34D are inhibited. This causes 0000 to be latched into U33 and the 0 (first character) table to be accessed by the next byte received.) When U30 is enabled, execution code 0000 is decoded; this sets the HDETA line HIGH. When U35B is enabled, the HDDMS pulse clocks quad-D flip-flop U31. In this case when U31 is clocked it drives the LCHN line LOW.

7-8.11 Power-On Reset Circuit

This circuit

- generates two signals, HIPON and LIPON, that reset A6 PCB circuits each time the 560A power is turned on.
- ORs the HDPON signal with a signal from the command decoder, HDCAS, and creates the HDPON and LDPON signals. The HDPON and LDPON signals reset A6 PCB circuits when either the 560A power is turned on or the 560A decodes the DCL (device clear) or SDC (selected device clear) interface messages.

A parts locator diagram for this circuit is shown in Figure 7-109, and the schematic is shown in Figure 7-110. The circuit consists of NOR gate U35D and associated components, NOR gate U40C, inverter U37C, and inverter U37D.

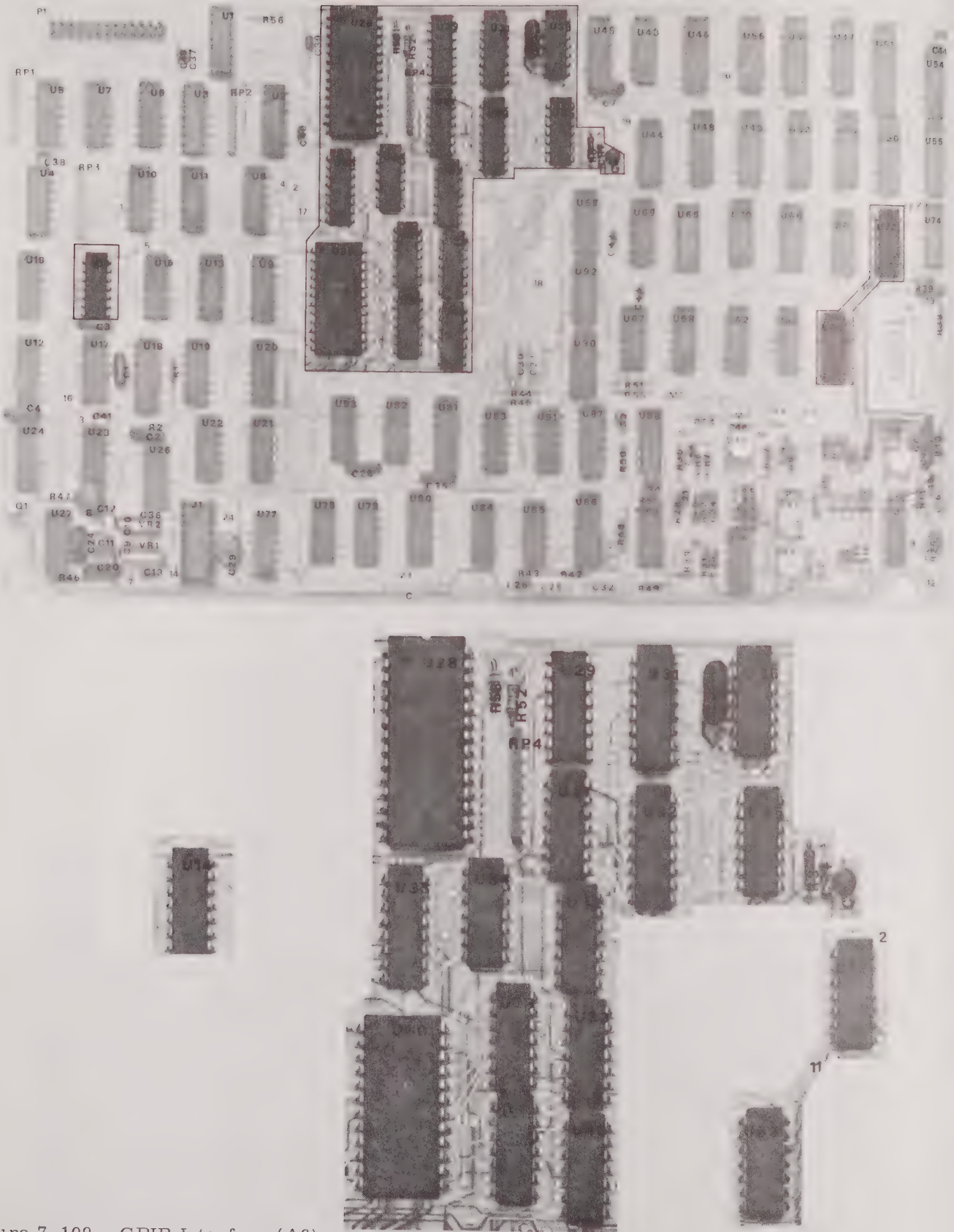
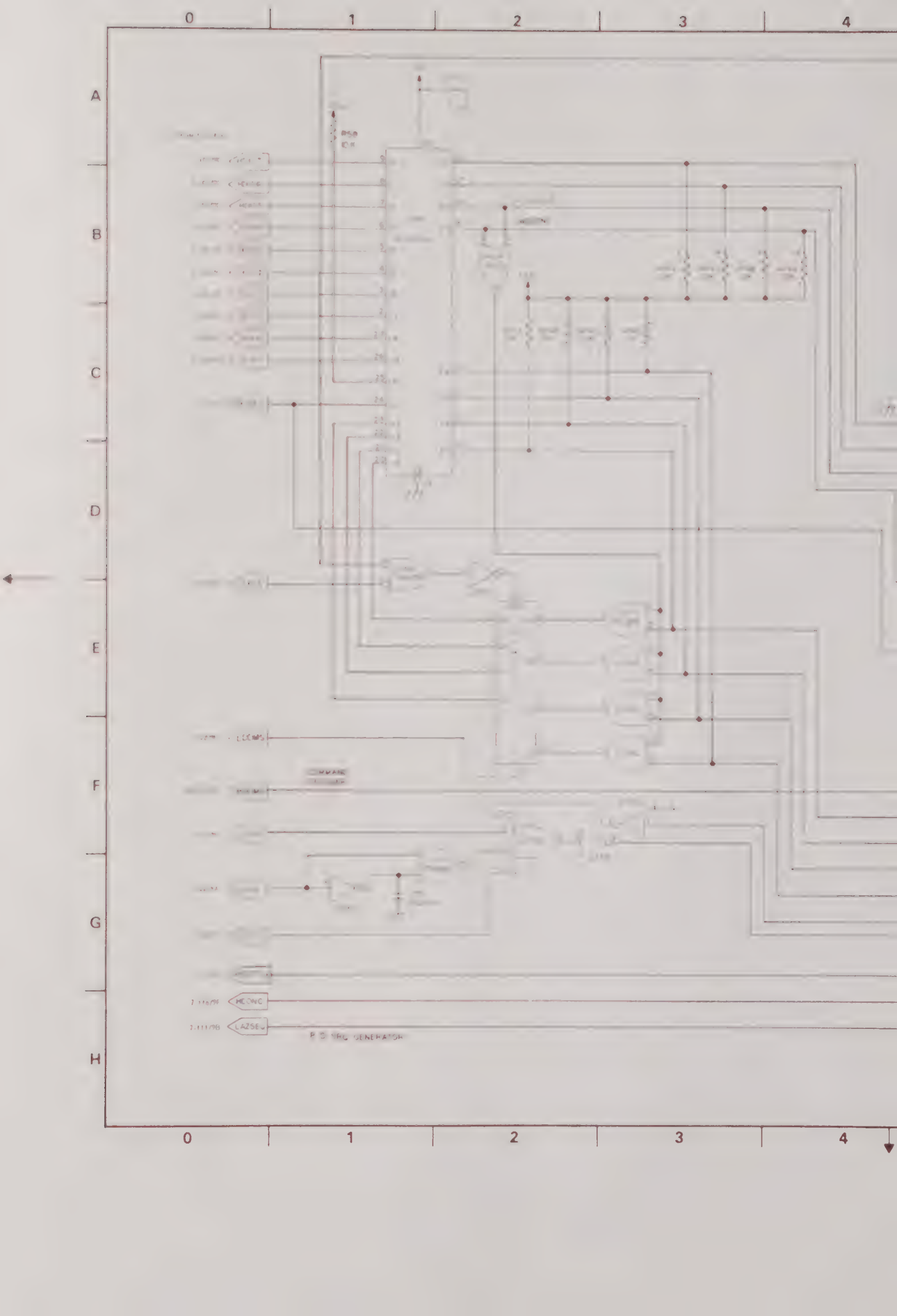


Figure 7-109. GPIB Interface (A6)
PCB SRQ Generator, Command Decoder,
and Power-On Reset Circuits Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
MECONC
LAZSEL
P.S. SRC GENERATOR

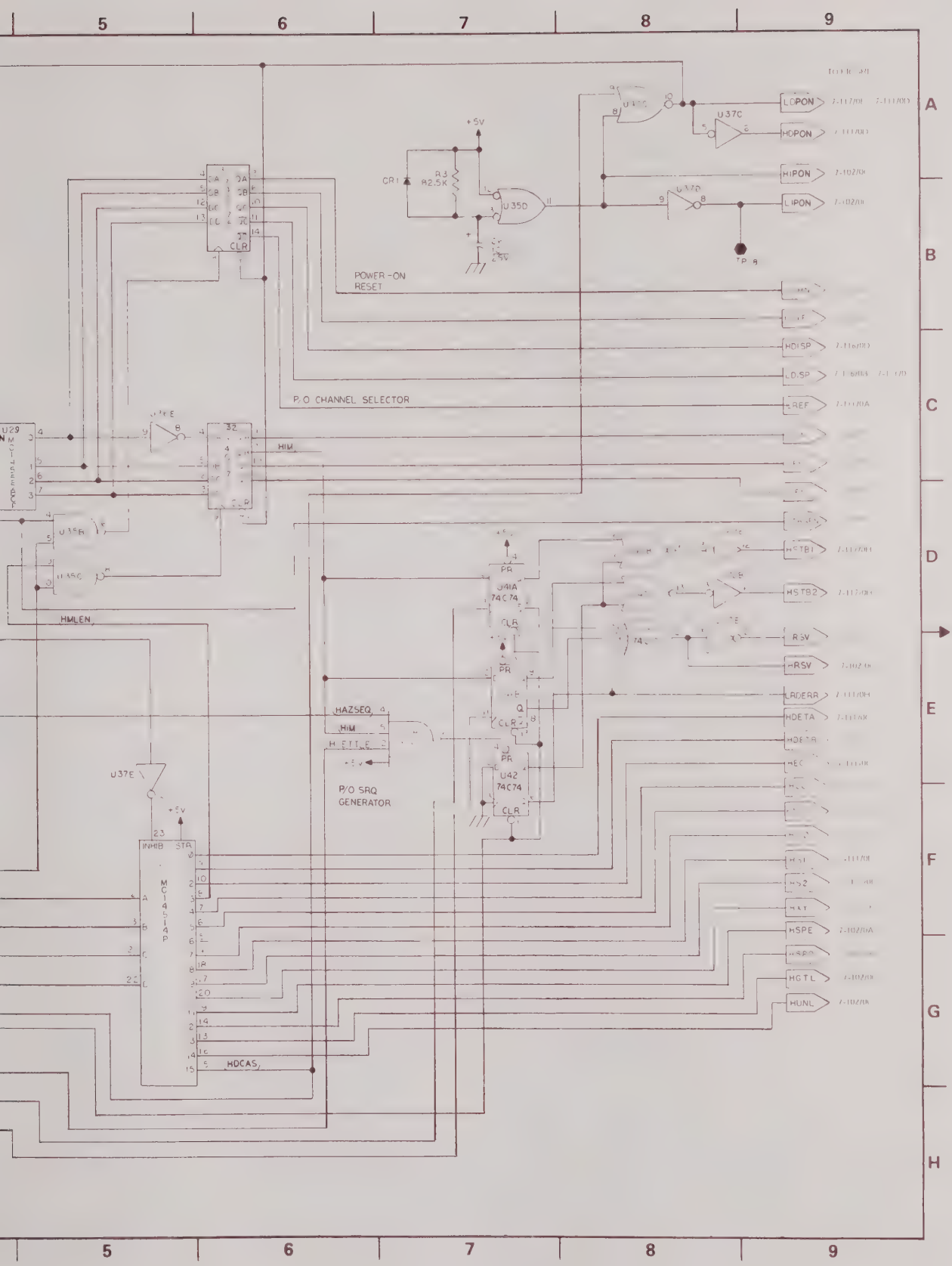


Figure 7-110. GPIB Interface (A6) PCB SRQ Generator, Command Decoder, and Power-On Reset Circuits Schematic Diagram

Figure 7-109.

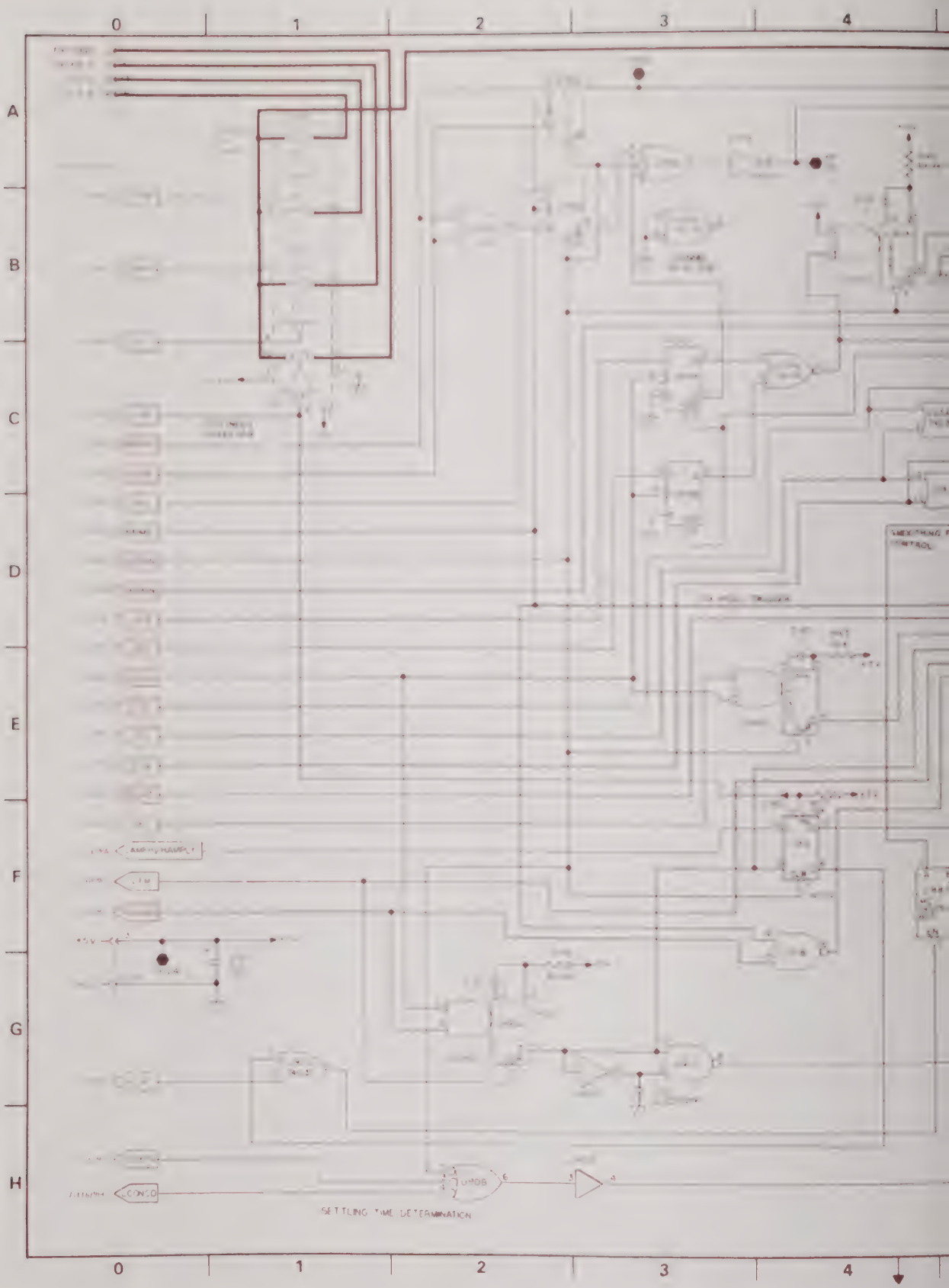
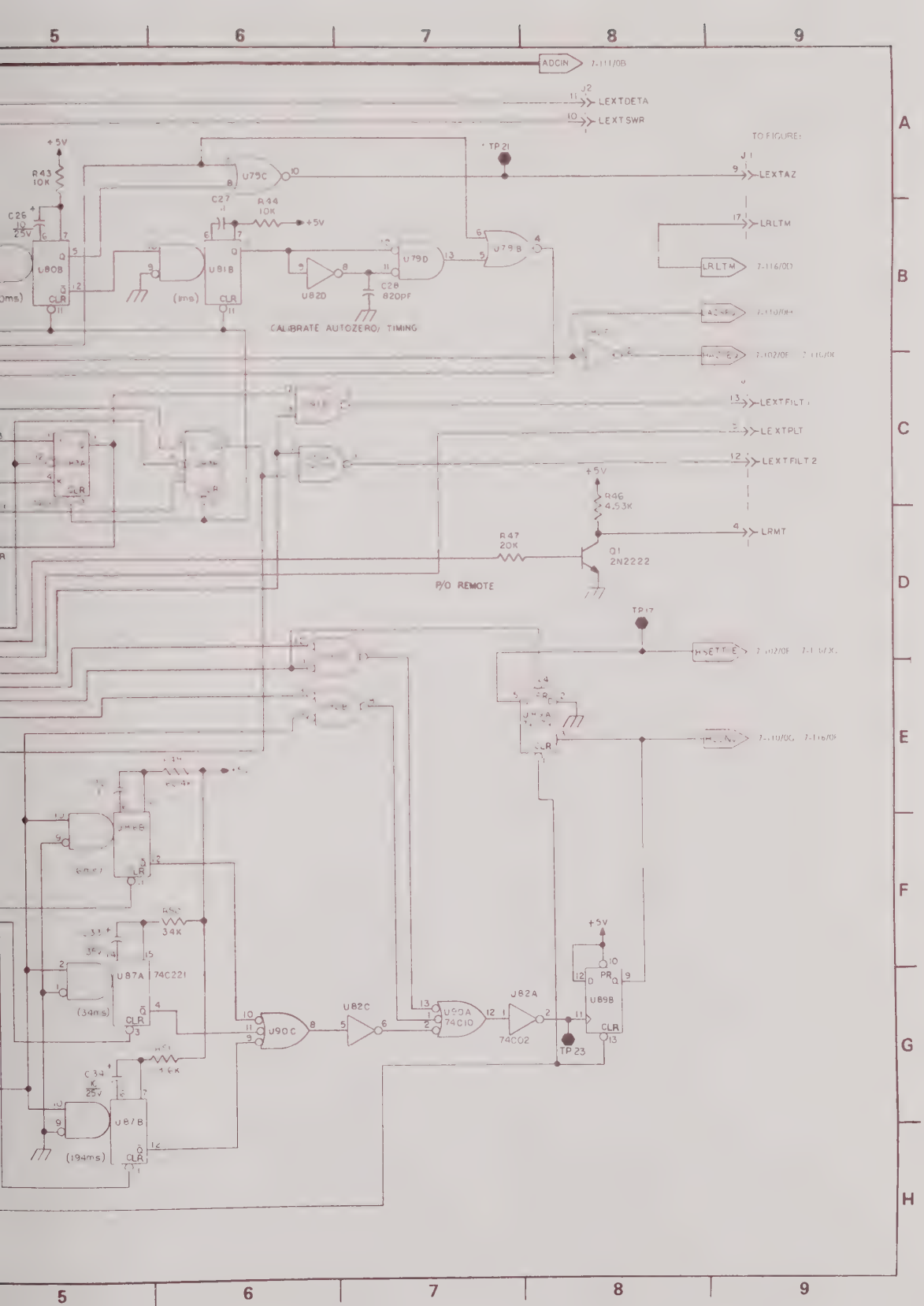


Figure 7-111. GPIB Interface (A6) PCB Channel Selector, Calibrate (Autozero) Timing, X-Y Plot Trigger, Input Selector, and Settling Time Determination Circuits Schematic Diagram


ADCIN
LEXTDETA
LEXTSWR
TO FIGURE:
LEXTAZ
LRLTM
LEXTFILT1
LEXTPLT
LEXTFILT2
LRMT
+5V
R43 10K
R44 10K
C26 10 25V
C27
C28 820pF
U79C
U79B
U79D
U80B
U81B
U82D
TP21
CALIBRATE AUTOZERO/ TIMING
R46 4.53K
R47 20K
Q1 2N2222
P/O REMOTE
TP17
U87A 74C221
(34ms)
R50 34K
U87B
(194ms)
C34 .1 25V
R51 1.6K
U90C
U82C
U90A 74C10
U82A 74C02
U89B
TP23
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B
C
D
E
F
G
H
5
6
7
8
9

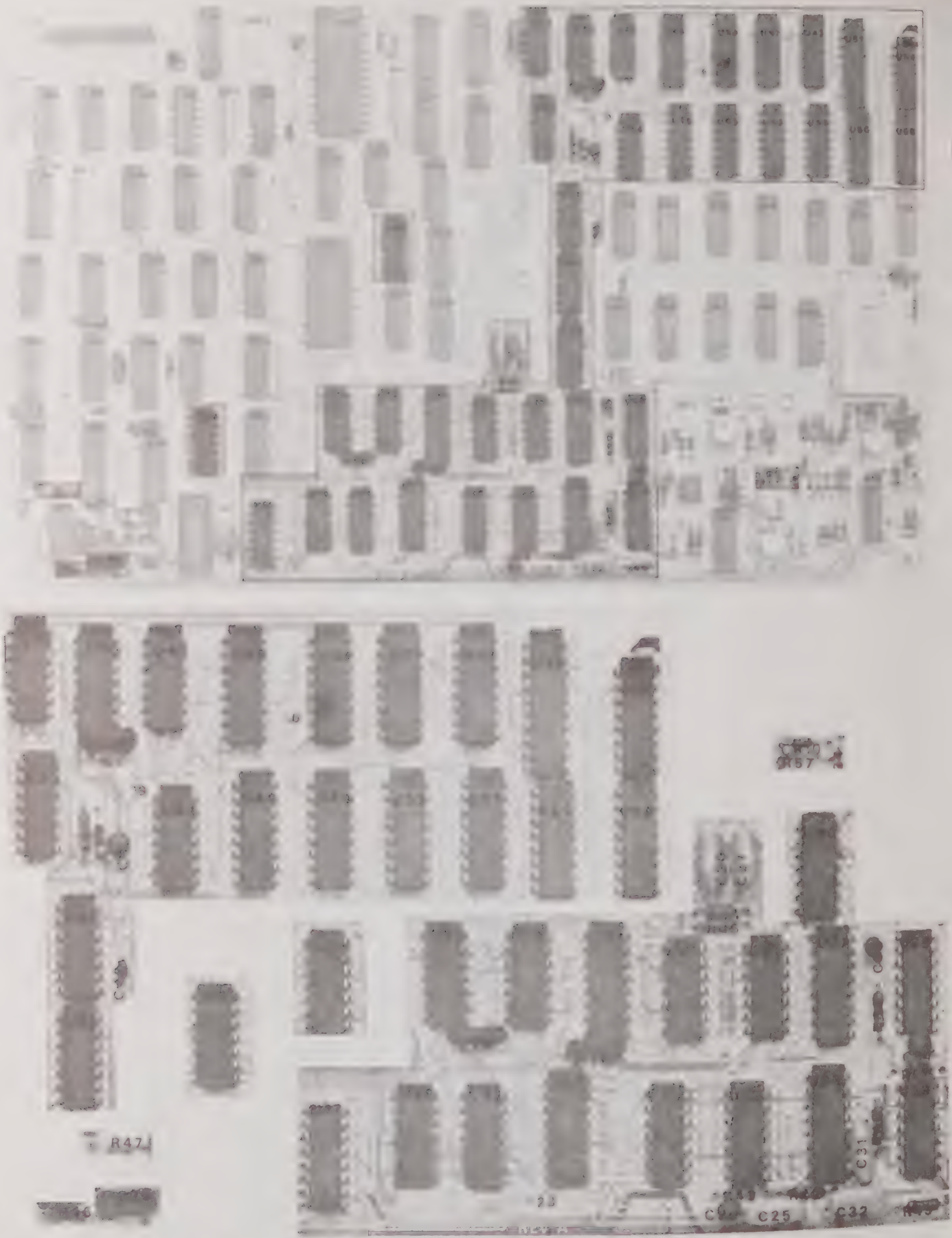


Figure 7-112. GPIB Interface (A6) PCB Channel Selector, Calibrate (Autozero) Timing, X-Y Plot Trigger, Input Selector, and Settling Time Determination Circuits Parts Locator Diagram

Figure 7-111.

7-8.12 Channel Select Circuit

This circuit

- latches the LEXT DETA/HEXT DETB output line LOW when a Channel A command (AI, AR, AD, CA) is decoded.
- latches the LEXT DETA/HEXT DETB output line HIGH when a Channel B command (BI, BR, BD, CB) is decoded.
- drives the LEXT SWR output line LOW when the noise level (NL) command is decoded.

The schematic for this circuit is shown in Figure 7-111, and the parts locator diagram is shown in Figure 7-112. The circuit consists of flip-flops U78A, U78B, gates U22B, U38B, and inverter U37A.

7-8.13 Calibrate (Autozero) Timing Circuit

This circuit generates log amplifier (A3 PCB) calibration (autozero) pulses as follows:

- LEXT AZ when the external calibrate (EC) command is decoded.
- LEXT AZ and LSWR when the local calibrated (LC) command is decoded.

The schematic for this circuit is shown in Figure 7-111, the parts locator diagram is shown in Figure 7-112, and a timing diagram is shown in Figure 7-113. The circuit consists of flip-flops U84A and U84B; one-shots U80A, U80B, and U81B, gates U79A, U79C, U79D, and U79B; and inverter U82D. Refer to the schematic and the timing diagram for the following discussion.

The HAZSEQ pulse is the first signal generated by the Calibrate (Autozero) Timing circuit. The HAZSEQ pulse occurs when either the LC or the EC command is decoded. (The LAZSEQ pulse is also generated at the same time; it is the same as the HAZSEQ signal, only inverted.) The HAZSEQ pulse is generated by Q output of U84A when LC is decoded or by the Q output of U84B when EC is decoded.

The LSWR pulse occurs coincident with the HAZSEQ pulse. LSWR is generated by the

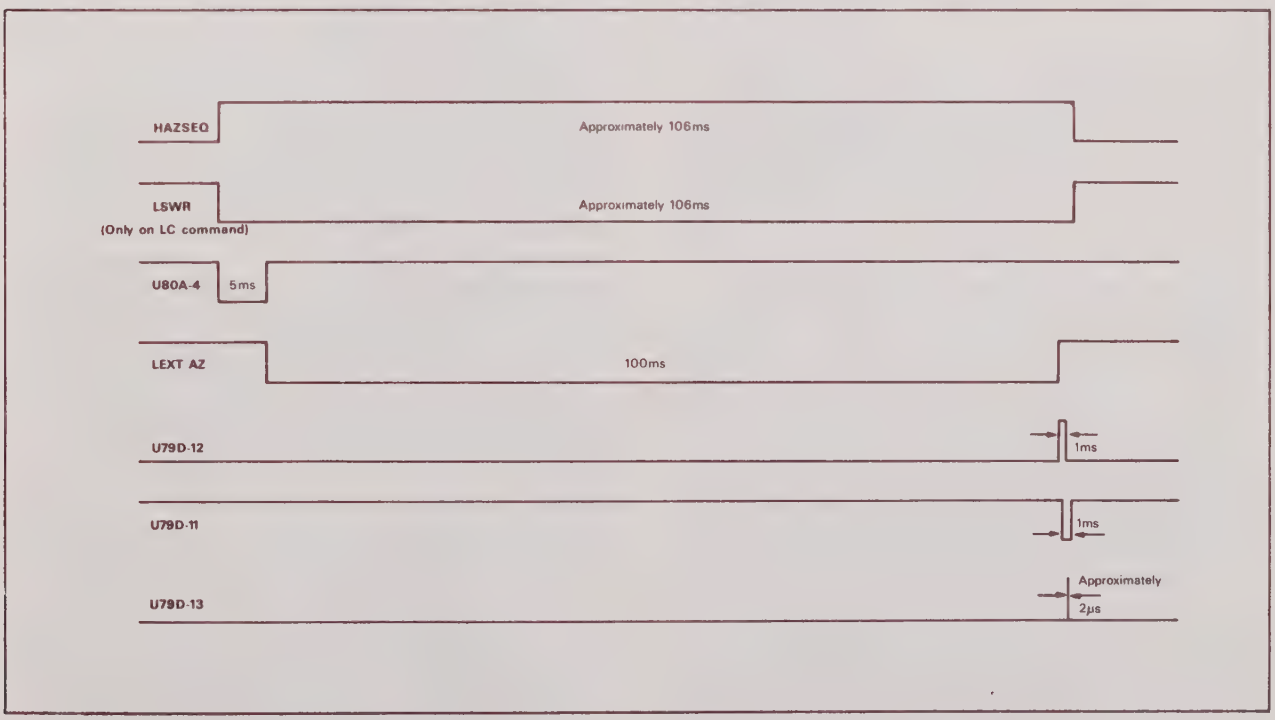


Figure 7-113. Calibrate (Autozero) Circuit Timing Diagram

$\overline{Q}$ output of U84A only when the LC command is decoded.

The third pulse generated by this circuit is the U80A-4 output pulse. This pulse creates a 5 ms delay before triggering U80B.

The LEXT AZ pulse is created by the Q output of 100ms one-shot multivibrator U80A. The trailing edge (LOW to HIGH transition) of the U80A-$\overline{Q}$ pulse triggers the start of 1ms one-shot U81B. The U81B-Q output pulse is applied to inverter U82D and NAND gate U79D. On the LOW to HIGH transition (trailing edge) this pulse, the U82D/U79D circuit produces a short-duration pulse.

The last pulse shown on the timing diagram is the U79D-13 pulse. As shown, this pulse is approximately 2 μs wide, its width is determined by the delay provided by C28. The U79D-13 pulse is inverted by NOR gate U79B and applied to the clear (CLR) inputs of U84A and U84B. When the U84A clear input is LOW, its $\overline{Q}$ output goes HIGH, and its Q output goes LOW. The LOW state of the U84A-Q output causes the HAZSEQ pulse to go LOW; the HIGH state of the U84A-$\overline{Q}$ pulse causes the LSWR pulse to go HIGH.

7-8.14 Smoothing (Filter) Control Circuit

This circuit generates log amplifier (A3 PCB) smoothing commands as follows:

- LEXT FILT 1--LOW,
  LEXT FILT 2--HIGH
  (smoothing command S1 decoded);
- LEXT FILT 1--LOW,
  LEXT FILT 2--LOW
  (smoothing command S2 decoded);
- LEXT FILT 1--HIGH,
  LEXT FILT 2--HIGH
  (smoothing command SØ (or SO) decoded, HDPON line HIGH, or the U86A-$\overline{Q}$ output LOW).

The schematic for this circuit is shown in Figure 7-111, and the parts locator diagram is shown in Figure 7-112. The circuit consists of the following components: flip-flops U83A, U83B, and gates U93A, U93B, U91A, and U91D.

The smoothing (filter) control circuit (Figure 7-111) has four inputs: the $\overline{Q}$ output from 6 ms one-shot multivibrator U86A (Settling Time Determination circuit), the HSØ input line, the HS1 input line, and the HS2 input line.

The U86A-$\overline{Q}$ output pulse is caused by two signals. The HTRIGEN signal, which enables the one-shot, and the DDMS pulse, which triggers the start of the output pulse. The LOW state of this 6 ms pulse inhibits NAND gates U91A and U91D, which sets smoothing to the off (SØ) state for 6 milliseconds following the decoding of AI, AR, AD, BI, BR, BD, NL, and RI.

The HSØ input sets the K input of both U83A and U83B HIGH. When clocked by the HDDMS pulse, the LOW state of the U83A-Q and U83B-Q output lines inhibits U91D and U91A. When U91A and U91D are inhibited, the LEXT FILT 1 and LEXT FILT 2 output lines go HIGH.

The HS1 input sets the J-input of U83A and the K-input of U83B HIGH. When clocked by the HDDMS pulse, as previously described, the HIGH state of the U83A-Q output line enables U91D, pin 12; the LOW state of the U83B-Q output line inhibits U91A. When U91D is enabled and U91A is inhibited, the LEXT FILT 1 output line goes LOW and the LEXT FILT 2 output line goes HIGH.

The HS2 input sets the J-input of both U83A and U83B HIGH. Again, when clocked by the HDDMS pulse, the HIGH states of the U83A- and U83B-Q output lines enable U91D, pin 12, and U91A, pin 2. When U91D and U91A are both enabled, the LEXT FILT 1 and LEXT FILT 2 output lines are both TRUE.

7-8.15 X-Y Plot Trigger Circuit

This circuit drives the LEXT PLT control line LOW when the X-Y plot command (XY) is decoded. The schematic for this circuit is shown in Figure 7-111, and the parts locator diagram is shown in Figure 7-112.

The circuit consists of one-shot U81A and associated components.

7-8.16 Input Selector Circuit

This circuit selects which input signal--LOG A,B; LOG A,B-R; LOG R; or EXT VERT--will be applied to the A/D Converter Input circuits (paragraph 7-8.18). The Input Selector circuit consists of multiplexer U77 (Figure 7-111) and input selector flip-flop U31 (Figure 7-110). A parts locator diagram for this circuit is shown in Figure 7-112.

7-8.17 Settling Time Determination Circuit

This circuit determines how much time (0 to 200 ms) the input data will be allowed to settle before A/D conversion is accomplished by A6 PCB circuitry. Settling time, what it is and why it is needed, is discussed in paragraph 3-6.1c.

The schematic for this circuit is shown in Figure 7-111, and the parts locator diagram is shown in Figure 7-112.

The settling time determination circuit

- sets smoothing temporarily to SØ when any of the following eight commands are decoded: AI, AR, AD, BI, BR, BD, RI, or NL. (See paragraph 7-8.13.)
- sets the HSETTLE (NRFD inhibit signal, paragraph 7-8.4) control line HIGH approximately 2 μs following the decoding of any one of the applicable eight commands.
- sets the HCONV (start A/D conversion) control line HIGH after 6 ms when the power level of the input signal is above -30 dBm.
- sets the HCONV control line HIGH after either 12, 40, or 200 ms, depending on smoothing level, when the power level of the input signal is below -30 dBm.
- inhibits 6 ms one-shot multivibrator U86A, and enables NAND gate U92C, when the fast mode (FM) command is decoded. This inhibiting and enabling action allows any one of the applicable eight commands to set the HCONV control line HIGH immediately.
- resets the HSETTLE control line either (1) immediately, if the 560A is in the fast mode or (2) after the applicable delay time (i.e., 6, 12, 40, or 200 ms), if the 560A is in either the HOLD or INTERRUPT mode.
- resets the HCONV control line LOW when either: (1) the LCONCO (A/D conversion complete) control line from the A/D converter circuit (paragraph 7-8.16) goes LOW, (2) the LRDERR (read error) control line from the SRQ generator circuit goes LOW, or (3) the LDPON (power-on reset) control line from the power-on reset circuit goes LOW.

The smoothing is temporarily set to SØ by one-shot multivibrator U86A in the settling time determination circuit, and gates U91D and U91A in the smoothing (filter) control circuit. The HTRIGEN control line enables U86A, pin 2, which allows the LDDMS pulse to trigger U86A. The U86A-Q output inhibits U91D and U91A, which sets smoothing to SØ.

The HSETTLE control line is set HIGH by gate U91B and flip-flop U89A. The HTRIGEN control line enables U91B and allows the HDDMS pulse to preset the U89A-Q output HIGH. The HIGH state of U89A-Q sets the HSETTLE control line HIGH.

The HCONV control line is set HIGH after 6ms by one-shot U86A, gate U91C, flip-flop U85, gates U92B and U90A, inverter U82A, and flip-flop U89B. The LAMPHI/HAMPLO control line is applied to the D input of U85. When the power level of the input signal is above -30 dBm, this line is LOW. The U85-Q output is clocked LOW by the trailing edge (LOW to HIGH transition) of the U86A-$\overline{Q}$ pulse. The LOW state of the U85-Q output enables U92B, pin 9. The trailing edge of the U86A-$\overline{Q}$ pulse, in addition to clocking U85, also causes a short-duration, negative-going pulse to be created at U91C-8. This pulse,

via gates U92B, U90A, and inverter U82A, clocks the U89B-Q output HIGH. The LOW to HIGH transition of the U89B-Q output sets the HCONV control line HIGH, and clocks the U89A-Q output LOW. When the U89A-Q output goes LOW, the HSETTLE line goes HIGH. The HIGH state of this line releases the hold on the NRFD handshake line and allows the acceptor handshake to be completed.

The HCONV control line is set HIGH after 12, 40, or 200 ms by the following components: the same components used in the "after 6 ms" circuit, above, plus 2-line to 4-line decoder U88, one-shot multivibrators U86B, U87A, U87B, gate U90C, and inverter U82C. The creation of the U91C-8 output pulse, and the operation of the U85 flip-flop are the same as described for the "after 6 ms" circuit operation, except: the LAMPHI/HAMPLO control line is HIGH when the input signal is below -30 DBM. With the LAMPHI/HAMPLO line HIGH, the U85-Q output is clocked HIGH; this inhibits U92B and prevents the U91C-8 pulse from clocking U89B. The U91-8 pulse, although prevented from clocking U89B, is allowed to trigger one of the three one-shot multivibrators, U86B, U87A, or U87B. Which multivibrator will be triggered depends on decoder U88; U88 controls the U86B, U87A, and U87B clear (CLR) inputs. If the clear input is LOW, the multivibrator will not respond to a trigger input. The input to U88 is from the smoothing (filter) control circuit. This input is a binary code that indicates the level of smoothing (SØ, S1, S2) that has been programmed. When decoded by U88, this binary code determines which one-shot will be enabled. If SØ is decoded, U86B is enabled; if S1 is decoded, U87A is enabled, and if S2 is decoded, U87B is enabled. The pulse width of whichever one-shot is enabled is added to the 6 ms pulse width of the U86A one-shot; the sum of these two pulse widths provides the overall circuit delay. This delay is 12 ms for SØ operation, 40 ms for S1 operation, and 200 ms for S2 operation.

The one-shot multivibrator U86A is inhibited by the LFM signal being applied to its clear (CLR) input. NAND gate U92A is enabled by the LFM signal being applied to pin 12. The HFM signal, which also occurs when the FM command is decoded, is ORed with the U85-$\overline{Q}$ signal and used to inhibit decoder U88. With U88 so inhibited, one-shot multivibrators U86B, U87A, and U87B are positively prevented from producing an output when either the FM command is decoded or the power level of the input signal is above -30 dBm.

The HSETTLE control line is reset LOW when the FM command is decoded by gate U90A, inverter U82A, and flip-flop U89B. The circuit operation for resetting the HSETTLE line following either 6, 12, 40, or 200 ms was described during the discussion on setting the HCONV line HIGH after 6 ms.

The HCONV control line is reset LOW by gate U90B, inverter U82B, and flip-flop U89B. When either (1) the A/D conversion cycle is complete, (2) a read error (paragraph 7-8.9) is detected, or (3) the 560A power is turned on or the DCL or SDC interface message command is received, the U89B-Q and U89A-Q outputs are cleared LOW. This clearing action resets the HCONV line LOW and insures that the HSETTLE line is also reset LOW.

7-8.18 A/D Converter Input Circuits

These circuits consist of an input display/normal circuit, a sign detector circuit, a -30 dBm comparator circuit, an absolute value circuit, and a track and hold circuit. A parts locator diagram for these circuits is shown in Figure 7-115, and the schematic is shown in Figure 7-116.

a. Input Display/Normal Circuit. This circuit consists of FET switch U59A and operational amplifier U73A and associated components. The circuit provides voltage gain for the EXT VERT input signal. The EXT VERT signal provides the A/D converter input when a display command, either AD or BD, is decoded. This signal requires amplification because its input amplitude

is referenced differently than the input amplitude of the LOG A, B; LOG, A, B-R; or LOG R signals. Whereas, the LOG A,B; LOG A,B-R; and LOG R signals are referenced to 125mV per dB of input signal, the EXT VERT signal is referenced to the vertical displacement of the CRT Y-axis signal, as determined by the front panel dB PER DIVISION switch-bank. The magnitude of this signal is 1 volt per CRT large division.

A voltage gain of 1.25 is provided by operational amplifier U73A when the LDISP command line is LOW. The LDISP line goes LOW when either the AD or BD command is decoded. When the LDISP line is HIGH, feedback resistors R23 and R24 are not switched into the circuit and U73A provides a gain of 1 for the normal (LOG A,B; LOG A,B-R; or LOG R) input signal.

b. Sign Detector Circuit. This circuit consists of flip-flop U67, inverter U72C, EXOR gate U76, and comparator U75A, with its associated components. The circuit detects the sign (+, -) of the input signal and latches the sign onto the LP/HM (LOW plus/HIGH minus) signal line. The input signal voltage, after being processed by the input display/normal circuit, is applied to sign detector U75A. At U75A, the input signal voltage is compared to zero volts (ground). If the input signal is above zero volts, the sign is plus (+); conversely, if the input signal is below zero volts, the sign is minus (-). The output of U75A is applied to EXOR gate U76.

Exclusive OR gate U76 is used to reverse the polarity of the sign when the display command input (EXT VERT) signal is processed. The polarity of the display command input signal is opposite to that of the normal input signal (LOG A,B; LOG A,B-R; LOG R); consequently, the polarity is reversed after the sign has been detected. Polarity reversal occurs before the sign data is latched onto the output signal line.

The output of U76 is applied to flip-flop U67. When the A/D converter has completed a conversion cycle, the HCONC line goes HIGH. The HIGH to LOW transition of this signal line clocks the sign data onto the LP/HM signal line.

c. -30 dBm Comparator Circuit. This circuit consists of comparator U75B and associated components. The circuit detects whether the input signal power level is above or below -30 dBm. (For the significance of this -30 dBm figure, refer to paragraph 3-6.1c and read the discussion on "Smoothing Commands.") The input signal, which is unaltered by the input display/normal circuit, is applied to the -30 dBm comparator U75B. At U75B, the input signal is compared with a voltage that represents -30 dBm. If the input signal power level is above the reference voltage level, the U75B output goes LOW; conversely, if the input signal power level is below the reference voltage level, the U75B output goes HIGH. The U75B output (LAMPHI/HAMPLO) is applied to the settling time determination circuit.

NOTE

When the input signal is below -30 dBm (U75B, pin 6, HIGH), U75B is prevented by R33 and R34 from changing logic states until the power level of the input signal rises above -29 dBm. This feedback circuit (R33-R34) prevents the LAMPHI/HAMPLO control line from alternately changing logic states when the input signal power level fluctuates around -30 dBm.

d. Absolute Value Circuit. This circuit consists of operational amplifiers U73C, U73B, and associated components. The circuit takes the absolute value of the input-signal voltage, i.e., the voltage

value of the input signal without regard to its sign (+, -), and produces a positive-value voltage signal. If the input signal is a negative-voltage value, the signal is inverted. Conversely, if the input signal is a positive-voltage value, the signal is routed through the circuit without inversion.

e. Track and Hold Circuit. This circuit consists of FET switch U59B and operational amplifier U73D and associated components. The circuit prevents (holds) the A/D converter's input signal from changing while a conversion cycle is in progress. The HCONV (start conversion) control line is applied to U59B. When the HCONV line is HIGH, U59B pins 8 and 9 open and prevent the input signal from updating the voltage that is applied to the A/D converter input (U61, pin 17).

7-8.19 A/D Converter Conversion Circuits

These circuits consist of an A/D converter, a BCD logic gating circuit, and a display input/refresh mode inhibit circuit. A parts locator diagram for these circuits is shown in Figure 7-115, and the schematic is shown in Figure 7-116.

a. A/D Converter Circuit. This circuit is a BCD successive-approximation A/D converter circuit. The input to this circuit is an analog voltage that falls between 0 and +10 volts. The output of this circuit is a 4-digit (0000 to 9999) representation of the input voltage.

The successive approximation (S/A) circuit consists of D/A converter U61; comparator U60; S/A registers U65 and U66; HCONV line-latch and gating circuit, which consists of U74, U27C, U72F, and C20; and 20 kHz clock oscillator circuit, which consists of U72D, U71E, U71D, and their associated components.

The S/A conversion cycle begins when the HCONV control line goes HIGH. The HIGH state of HCONV causes a logic HIGH to be applied to U66, pin 10, and U65, pin 9. The HIGH state of U66-10 inhibits the U66 successive approximation register (SAR). The HIGH state of U65-9 enables the U65 SAR. When U65 is enabled, the rising edge of the clock pulse applied to pin 7 starts the conversion cycle. When the U65 conversion cycle is complete, the EOC line (pin 11) goes HIGH. The U65-EOC line causes two circuit actions. The LOW to HIGH logic transition of the line causes the U74-Q output to be cleared LOW, which enables U66-10 and inhibits U65. The HIGH logic state of the EOC line enables U66, pin 9; this allows the A/D conversion cycle to continue. When the U66 conversion cycle is complete, the U66 EOC pulse clocks U67, sets the HCONC control line HIGH, and creates a pulse output (LCONCO) from NAND gate U27B.

b. BCD Logic Gating Circuit. This circuit prevents "illegal" bits from being retained by the SAR during the course of a conversion cycle. In BCD logic, illegal codes are 1010 (ten), 1011 (eleven), 1100 (twelve), 1101 (thirteen), 1110 (fourteen), and 1111 (fifteen). When any of the illegal codes are generated by the SAR (Figure 7-114), the BCD logic gating circuit drives the SAR decision (D) input (pin 6) LOW. A LOW on the SAR decision input resets to 0 the bit that created the illegal code. The next SAR bit is then tried. If this bit also creates an illegal code, it too is reset to a logic 0. The S/A process continues in this manner until a close approximation of the input voltage is attained by a legal BCD code.

c. Display Input/Refresh Mode Inhibit Circuit.

This circuit inhibts the generation of logic 1 bits by the SAR when (1) a display command (AD, BD) is decoded, and (2) the 560A is in the REFRESH DISPLAY mode. The LDISP control line that goes to U38C, pin 11, is HIGH

when either the AD or the BD command is decoded. The LRLTM control line that goes to U38C, pin 10, is HIGH when the 560A is in the REFRESH DISPLAY mode. When both of these lines are HIGH at the same time, U38C is driven LOW. The LOW from U38C is applied, via NOR gate U68 and inverter U72A, to the decision (D) input of SARs U65 and U66. A continuous LOW on the decision input causes the SAR output lines to be driven LOW.

Order of Approximations	SAR BIT Code* MSD MSB	MSD NMSB	MSD NLSB	MSD LSB		NMSD MSB	NMSD NMSB	NMSD NLSB	NMSD LSB	Remarks
1st	1	0	0	0		0	0	0	0	This BIT code is "tried" (compared against the input analog voltage) and produces a voltage, V_O, at the output (pin 21) of U61. This voltage, V_O, is applied to U60, where it is compared against a reference (zero) voltage, V_R. If V_O is greater than V_R, then the U60 output (pin 1) is HIGH. The output of U60 is applied to 8-input NOR gate U68. If none of the U68 input pins is LOW, the U68 output (pin 8) is LOW. The LOW state of the U68 output causes the U65 and U66 decision (D) inputs to go HIGH. The next BIT is then tried.
2nd	1	1	0	0		0	0	0	0	This is an illegal BCD code. This code; via U62A, U63B, and U64B; causes the U68 output to go HIGH. The HIGH state of the U68 output causes the U65 and U66 "D" input to go LOW. The next BIT is then tried.
3rd	1	0	1	0		0	0	0	0	NMSB* is reset to 0; NLSB* is tried. This produces an illegal BCD code.
4th	1	0	0	1		0	0	0	0	NLSB* is reset to 0; LSB* is tried. This produces a legal BCD code. The U65 "D" input either stays a 1 or is reset to a 0; this depends on whether V_O is greater or lesser, respectively, than V_R.
5th thru 8th	1	0	0	1	thru	1	0	0	0	The sequence of conversion operations with the NMSD* is the same as described above for the MSD*. When the U65 conversion cycle is complete and all of the BITs of the MSD* and NMSD* have been tried, the U66 SAR conversion cycle begins. In the same manner as described for the MSD*, the U66 SAR tries the NLSD* and LSD* BITs.
	1	0	0	1		1	0	0	1	

* Legend

MSD:	Most Significant Digit	MSB:	Most Significant BIT
NMSD:	Next Most Significant Digit	NMSB:	Next Most Significant BIT
NLSD:	Next Least Significant Digit	NLSB:	Next Least Significant BIT
LSD:	Least Significant Digit	LSB:	Least Significant BIT

Figure 7-114. BCD Successive Approximation Conversion Cycle

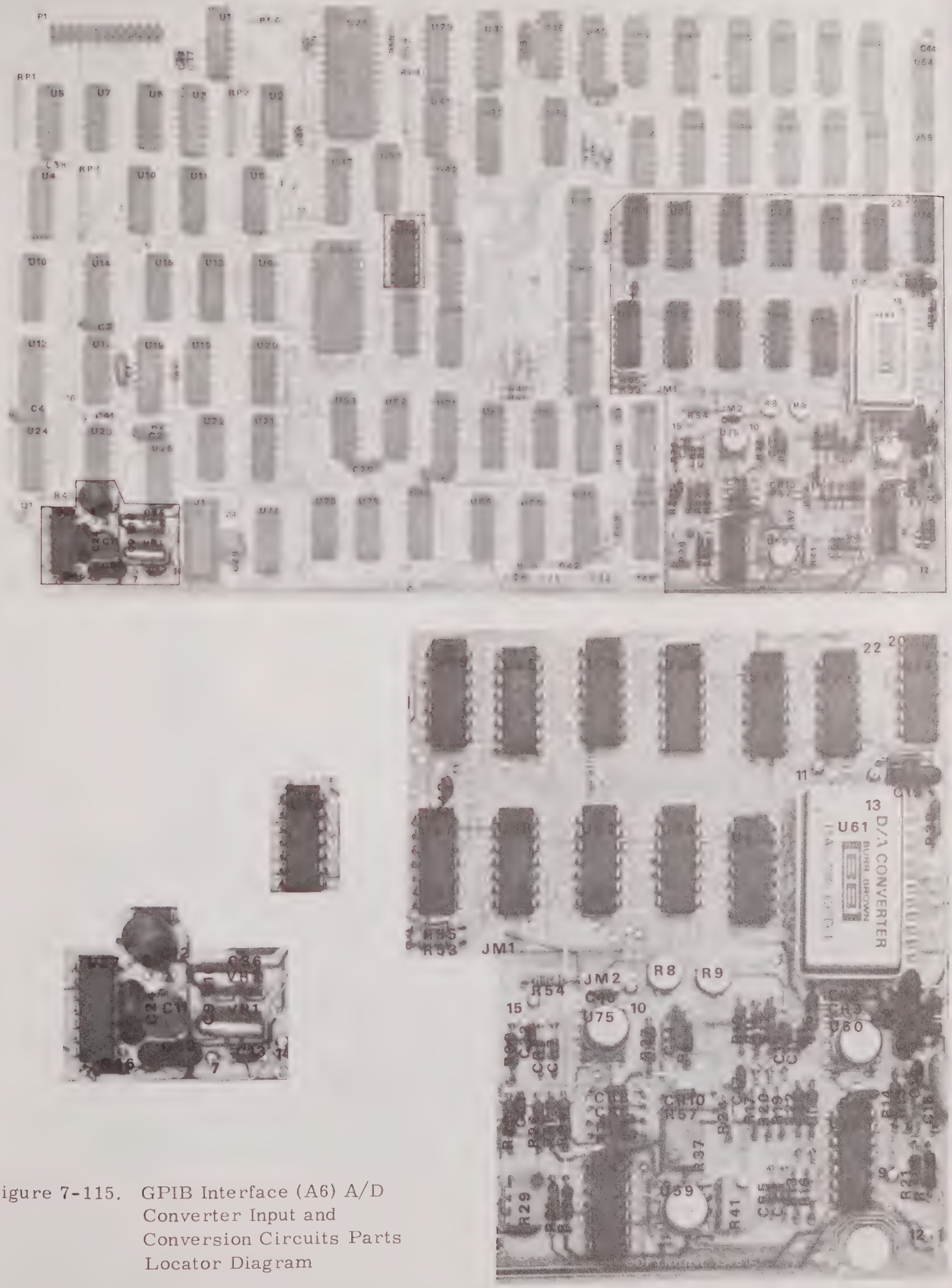
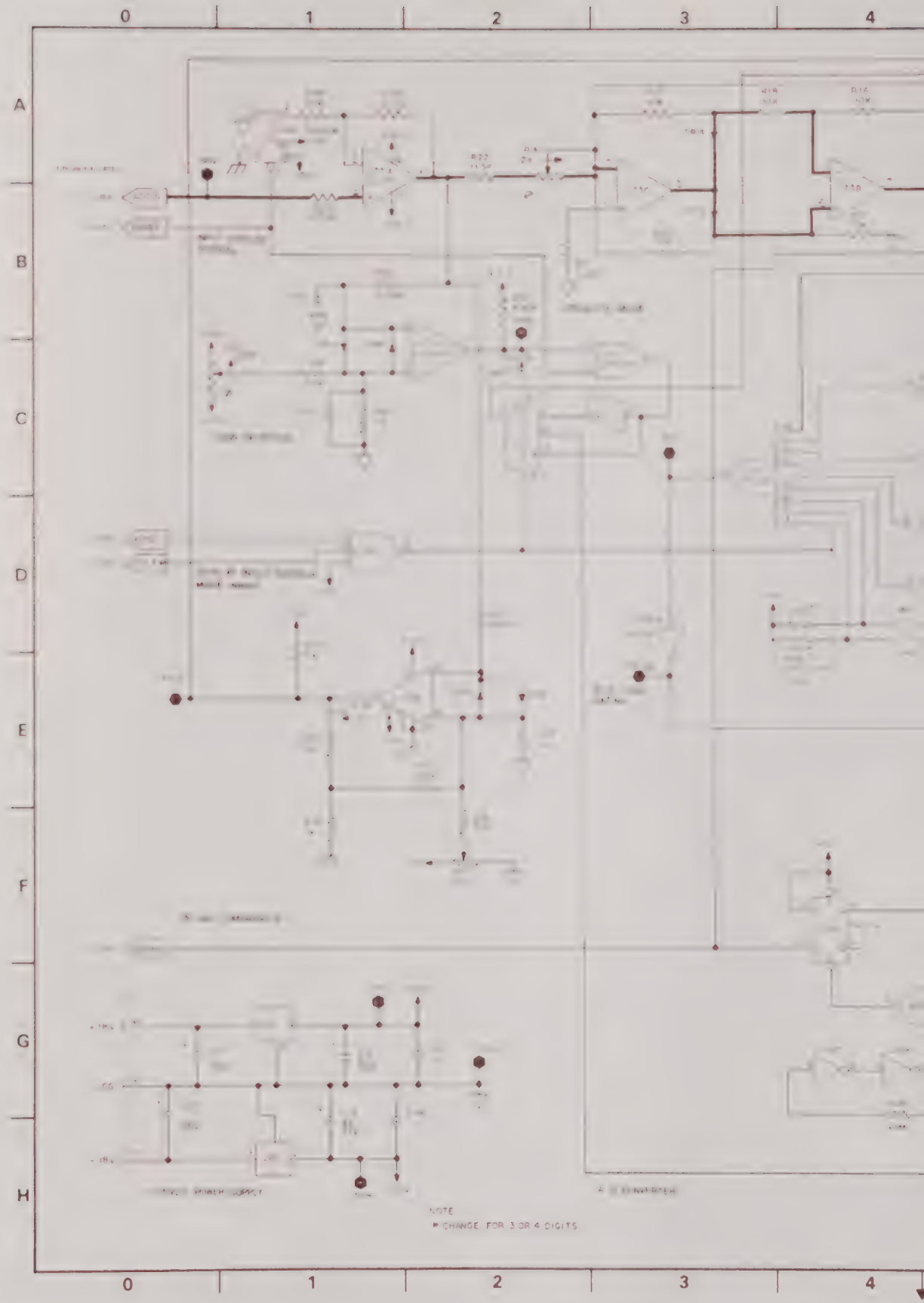


Figure 7-115. GPIB Interface (A6) A/D Converter Input and Conversion Circuits Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H
NOTE
* CHANGE FOR 3 OR 4 DIGITS

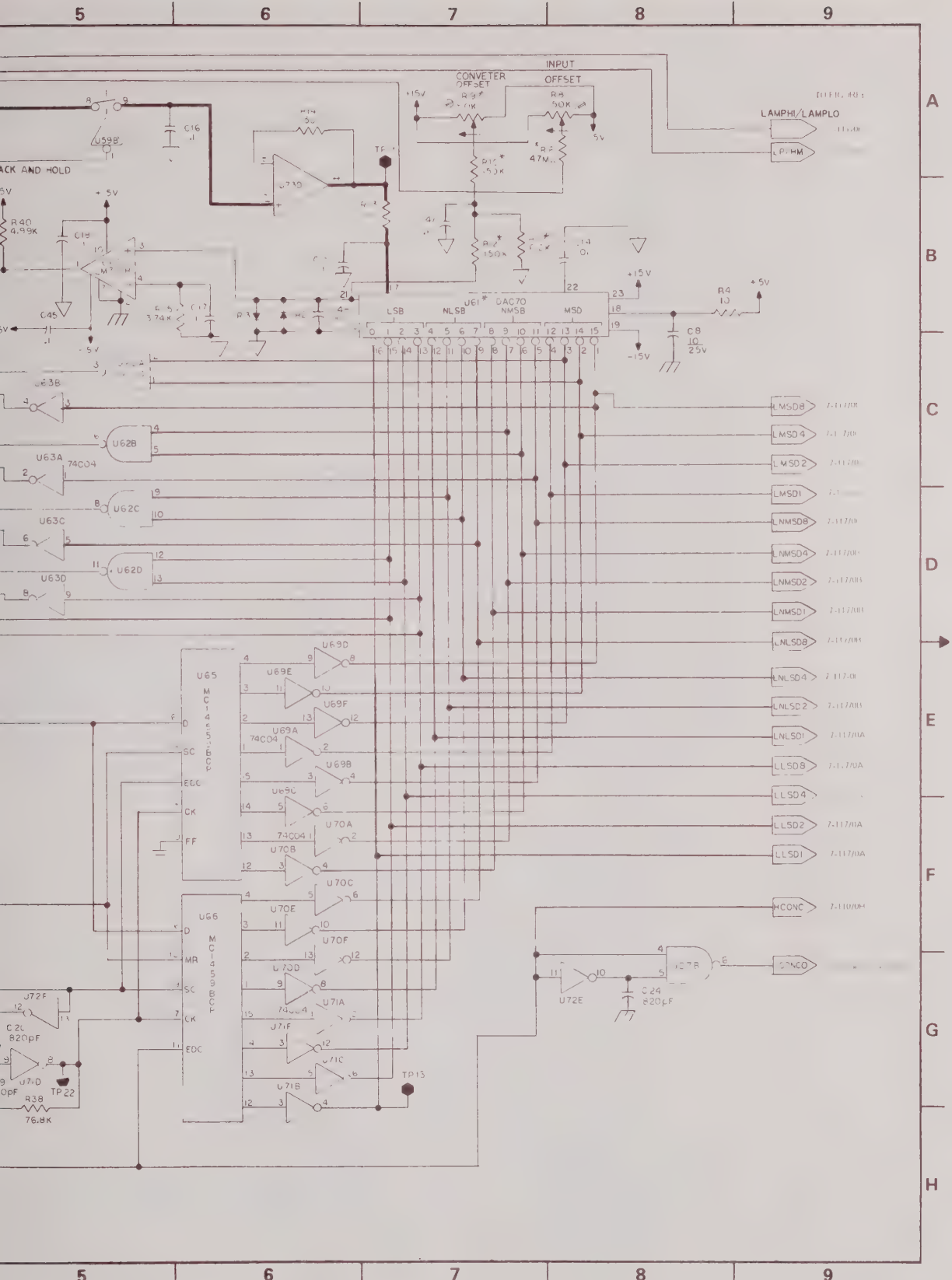


Figure 7-116. GPIB Interface (A6) A/D Converter Input and Conversion Circuits Schematic Diagram

Figure7-115.

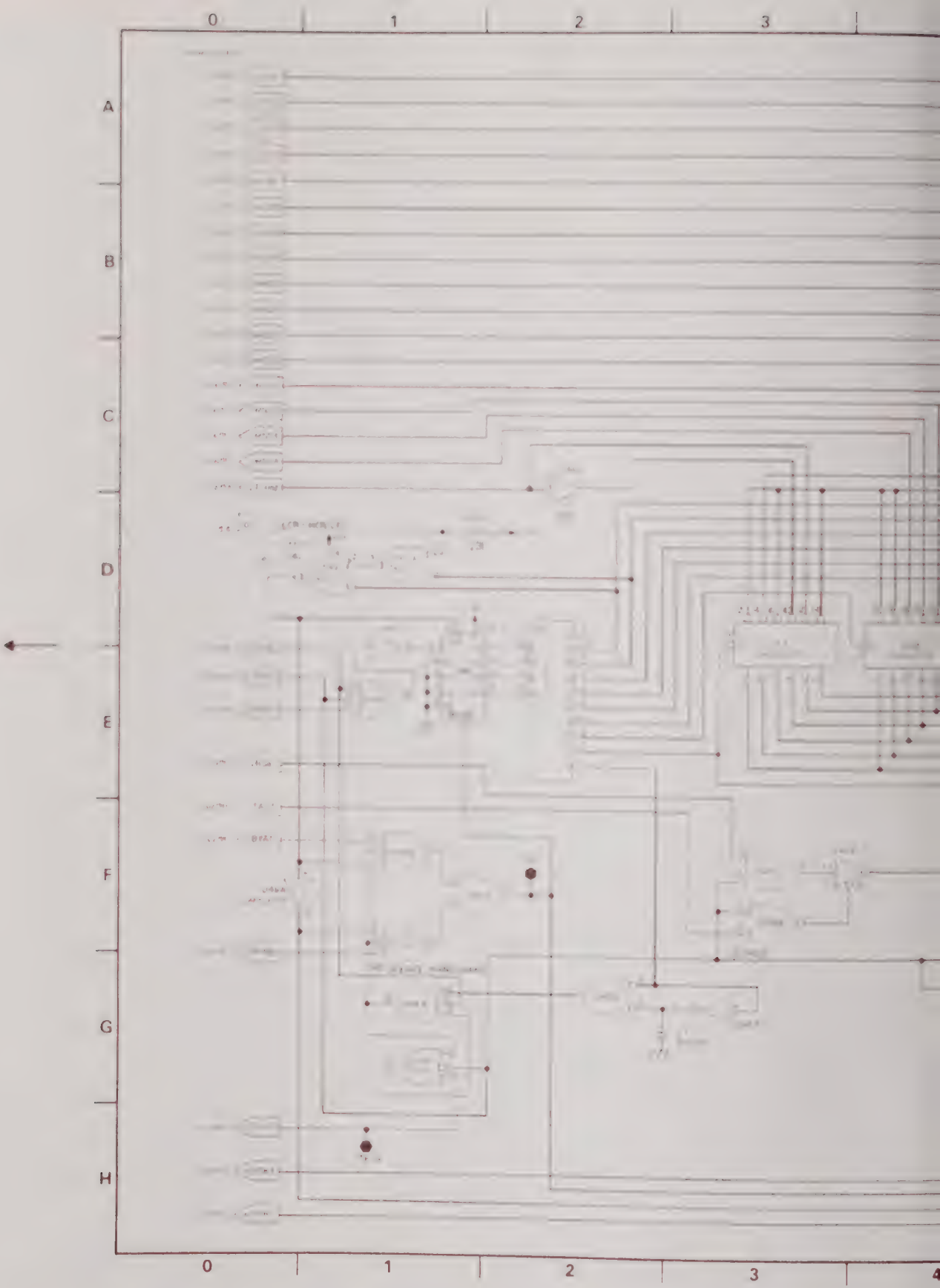
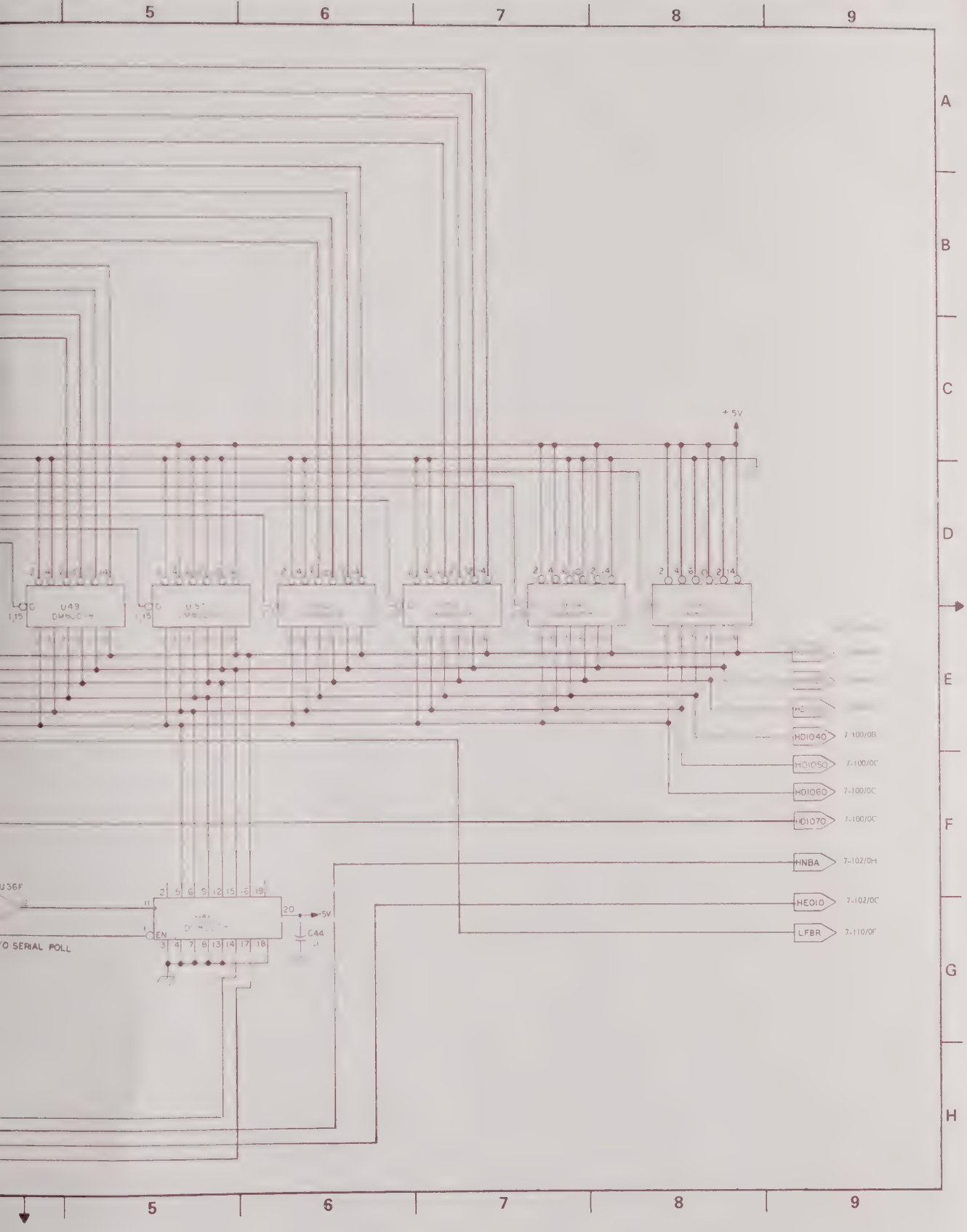


Figure 7-117. GPIB Interface (A6) PCB Byte Sequencer Circuit Schematic Diagram


5
6
7
8
9
A
B
C
D
E
F
G
H
+5V
HDI040
7-100/0B
HDI050
7-100/0C
HDI060
7-100/0C
HDI070
7-100/0C
HNBA
7-102/0H
HEOI0
7-102/0C
LFBR
7-110/0F
+5V
C44
EN
SERIAL POLL

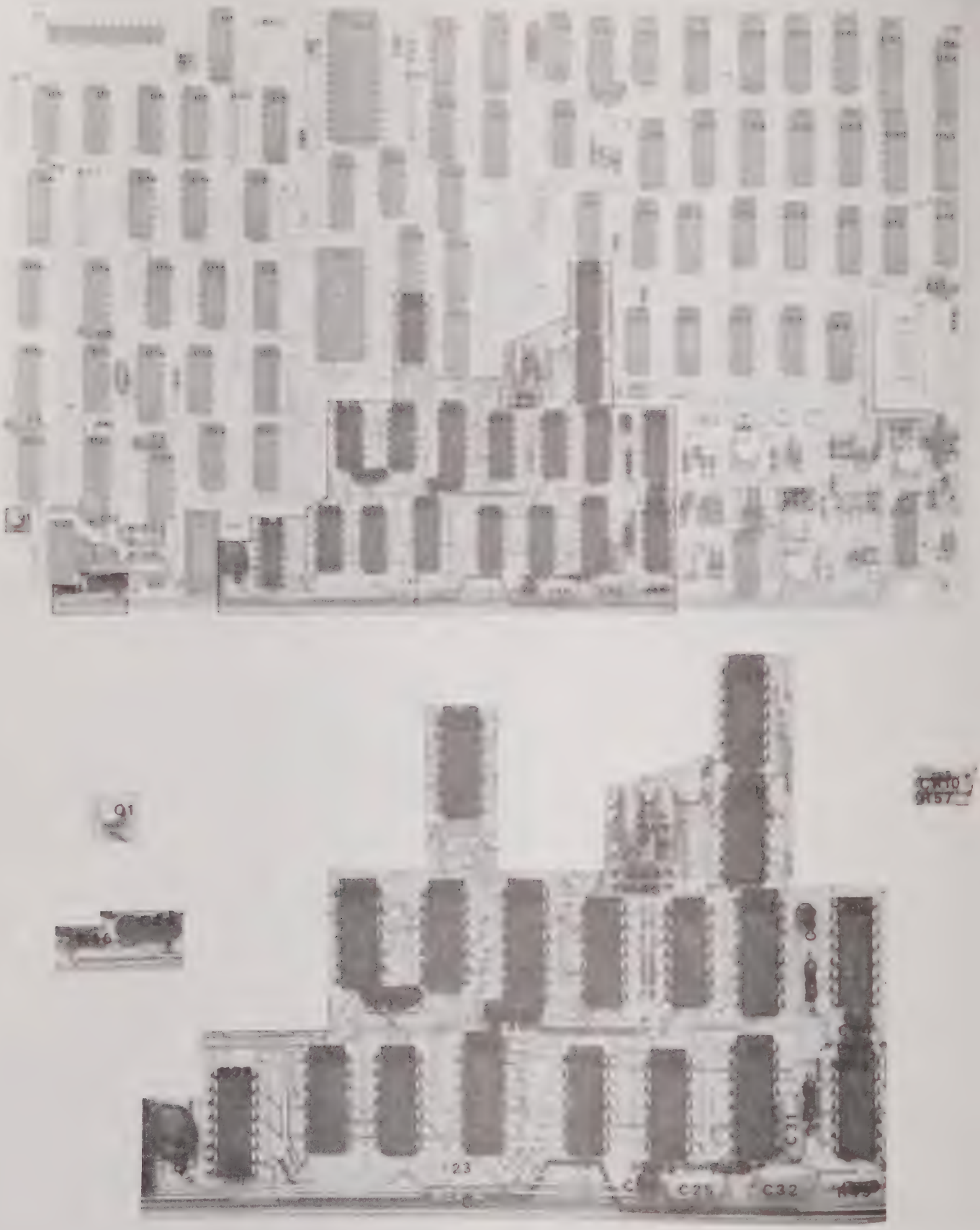


Figure 7-118. GPIB Interface (A6) PCB Byte Sequencer Circuit Parts Locator Diagram

Figure 7-117.

7-8.20 Byte Sequencer Circuit

This circuit, via tri-state buffers, converts the BCD data from the A/D converter into ASCII data, and gates the ASCII data onto the data output pins of bus transceivers U1 and U2 (Figure 7-101). This data is gated onto the data output pins of U1 and U2 in the following byte-order sequence:

- Sign (+, -) byte
- Most-significant-digit (MSD) byte
- Next-most-significant-digit (NMSD) byte
- Decimal point byte
- Next-least-significant-digit (NLSD) byte
- Least-significant-digit (LSD) byte
- Carriage return (CR) byte (rear panel CR-CR/LF switch in CR position)
- Line feed (LF) byte (CR-CR/LF switch in CR/LF position)

The schematic diagram for this circuit is shown in Figure 7-117, and the parts locator diagram is shown in Figure 7-118. The circuit consists of tri-state buffers U47 thru U50 and U52 thru U55; 4-line to 10-line decoder U57; synchronous up-counter U56; gates U45A, U58A, U44C, U45B, U44A, U44B; and inverters U46A thru U46D.

Sign data from the sign detector circuit and BCD data from the A/D converter circuit provide the input to the byte sequencer circuit (Figure 7-117). The sign data is applied to tri-state buffer (TSB) U47, and the BCD data is applied to TSBs U48, U49, U52, and U53. The input lines to TSBs U50, U54, and U55 are configured such that when gated the TSB output lines contain a preset ASCII character: U50 has the decimal point character, U54 has the CR character, and U55 has the LF character.

Tri-state buffers U47 thru U50 and U52 thru U55 are gated sequentially in accordance with the output logic state of decoder U57. U57 is driven by the output of U56. U56 is a 4-bit binary synchronous up-counter. U56 is clocked by either the LRFNB signal (via U43A and U45C) or the LBYAC signal (via U43B and U45C) from the source (talk) handshake circuit.

Counter U56 is reset to zero in one of the following three ways.

1. When either the LDPON or LSPAS control line goes LOW or the HTADS control line goes LOW, U56 is cleared to zero by the LOW applied to its CLR input.

2. When the U57 "7" output line goes TRUE, it enables U45A, pin 2. If the rear panel CR/CR-LF switch is in the CR position, it enables U45A pin 1. When both of the U45A input pins are enabled, its logic 0 ouput, via U58A, enables the load (LD) pin of U56. The enabling of its LD pins causes U56 to load, on the next clock pulse, the logic state of its D_A thru D_D input lines, which are a logic 0 (ground).

3. When the U57 "8" output line goes TRUE, it, via U58A, enables the LD pin of U56. U56 is then reset to zero as described above.

NOTE

The "8" line of U57 will be activated only if the CR/CR-LF switch is in the CR-LF position; otherwise, U56 is reset to zero before the count of eight is reached.

One other signal is generated by this circuit; it is the U44A/U44B latch circuit reset pulse. When decoder U57 decodes a zero count from U56, the U57, pin 1, "0" line goes LOW. The HIGH to LOW transition of this line causes U45B to generate a short-duration, negative-going pulse. This pulse goes to U44B, pin 4, where it sets the output state of U44B HIGH. The HIGH state of the U44B output inhibits U43A and U43B. The U44A/U44B latch circuit is reset LOW again by either the LCONCO (end of conversion output) control line or the LSPAS (serial poll active state) control line.

7-9 GPIB CONNECTOR PANEL (A7) PRINTED CIRCUIT BOARD

This printed circuit board (PCB) provides a connecting plane for the OPTION 3 IEEE 488, IEC 625-1, Interface (GPIB) Panel connector and ADDRESS switches. The Option 3 Interface Panel and A7 PCB is shown in Figure 7-119; the A7 PCB schematic is shown in Figure 7-120.

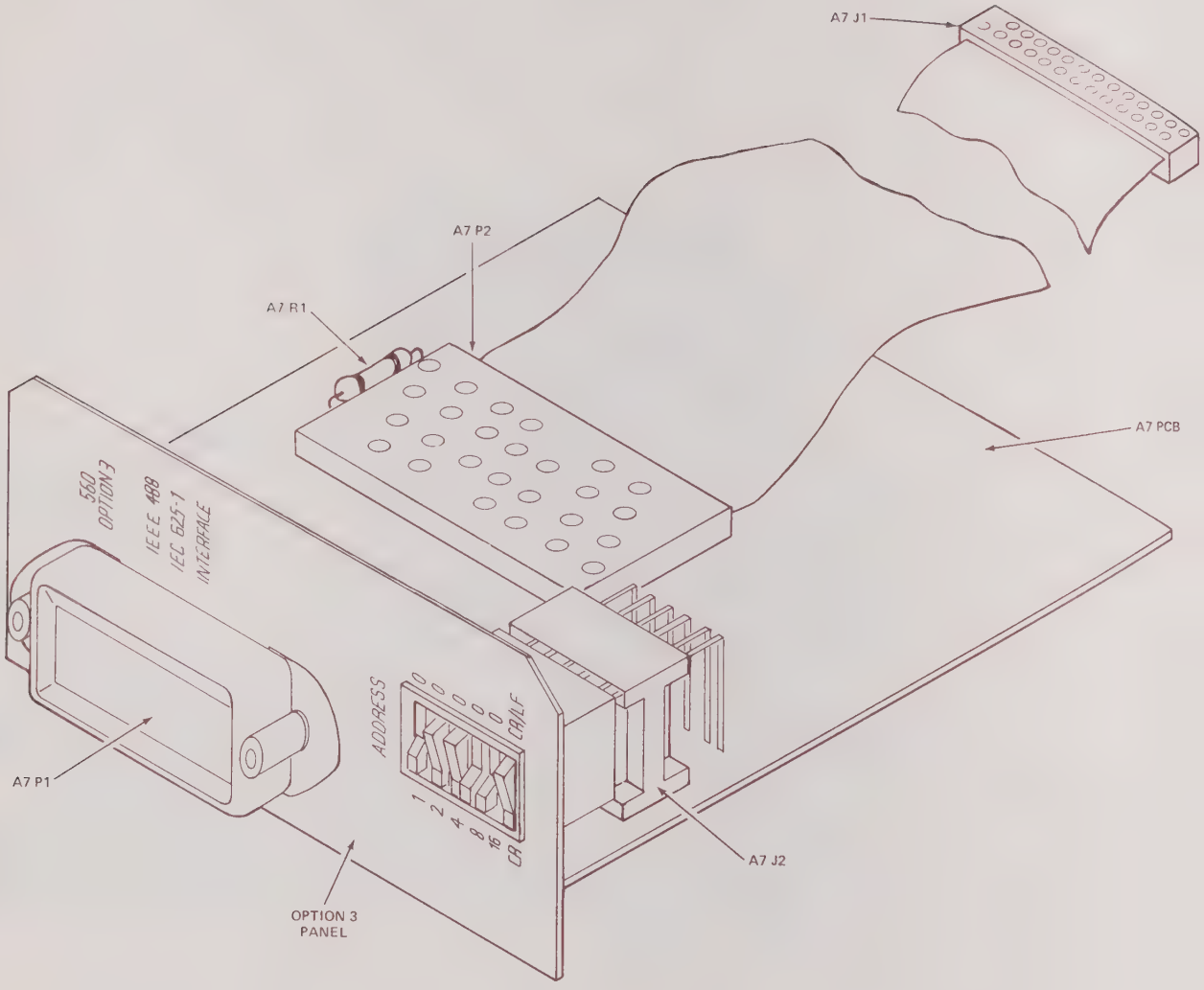
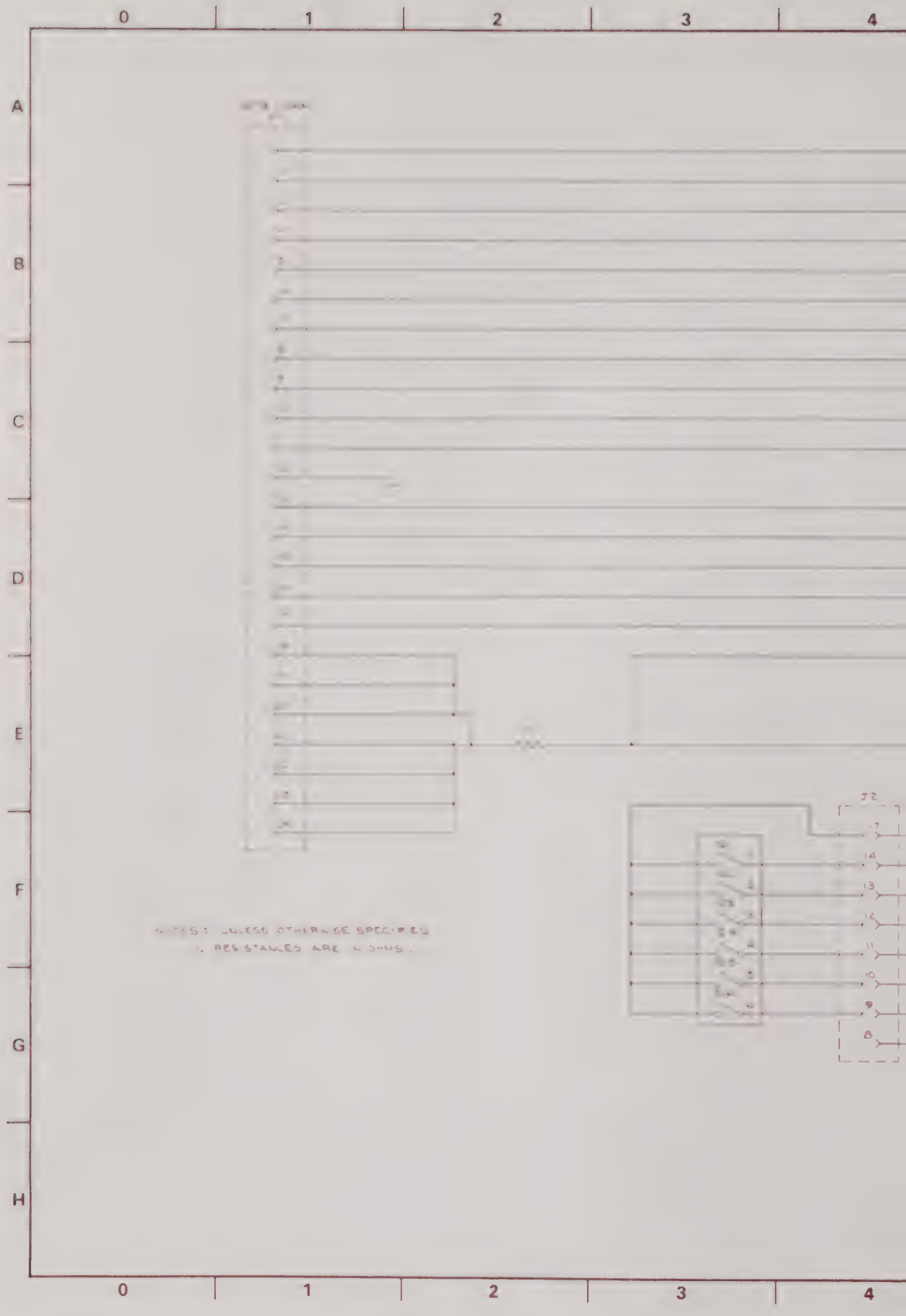


Figure 7-119. Option 3 Interface Panel and A7 PCB Assembly


0
1
2
3
4
A
B
C
D
E
F
G
H
J2
7
14
13
12
11
10
9
8

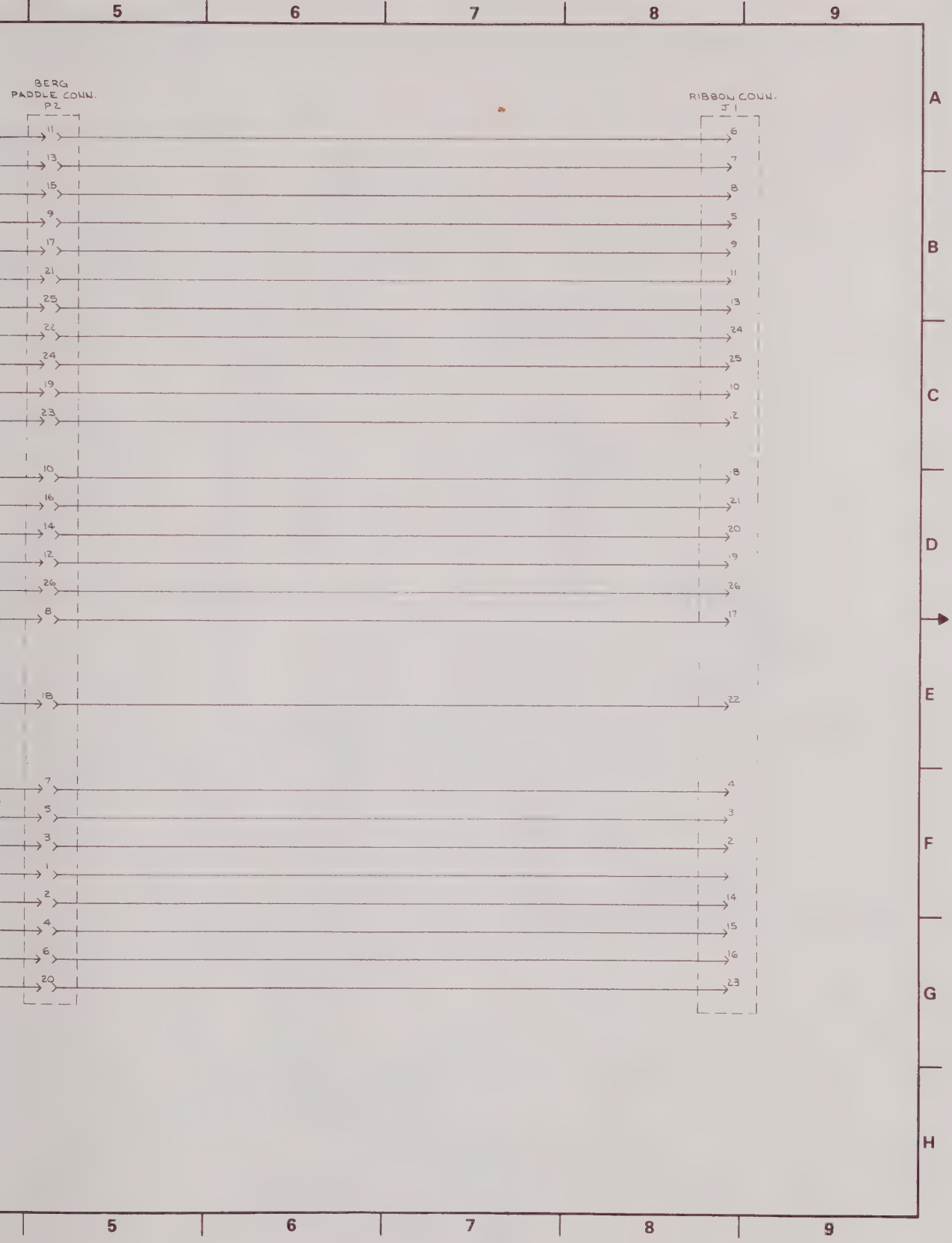
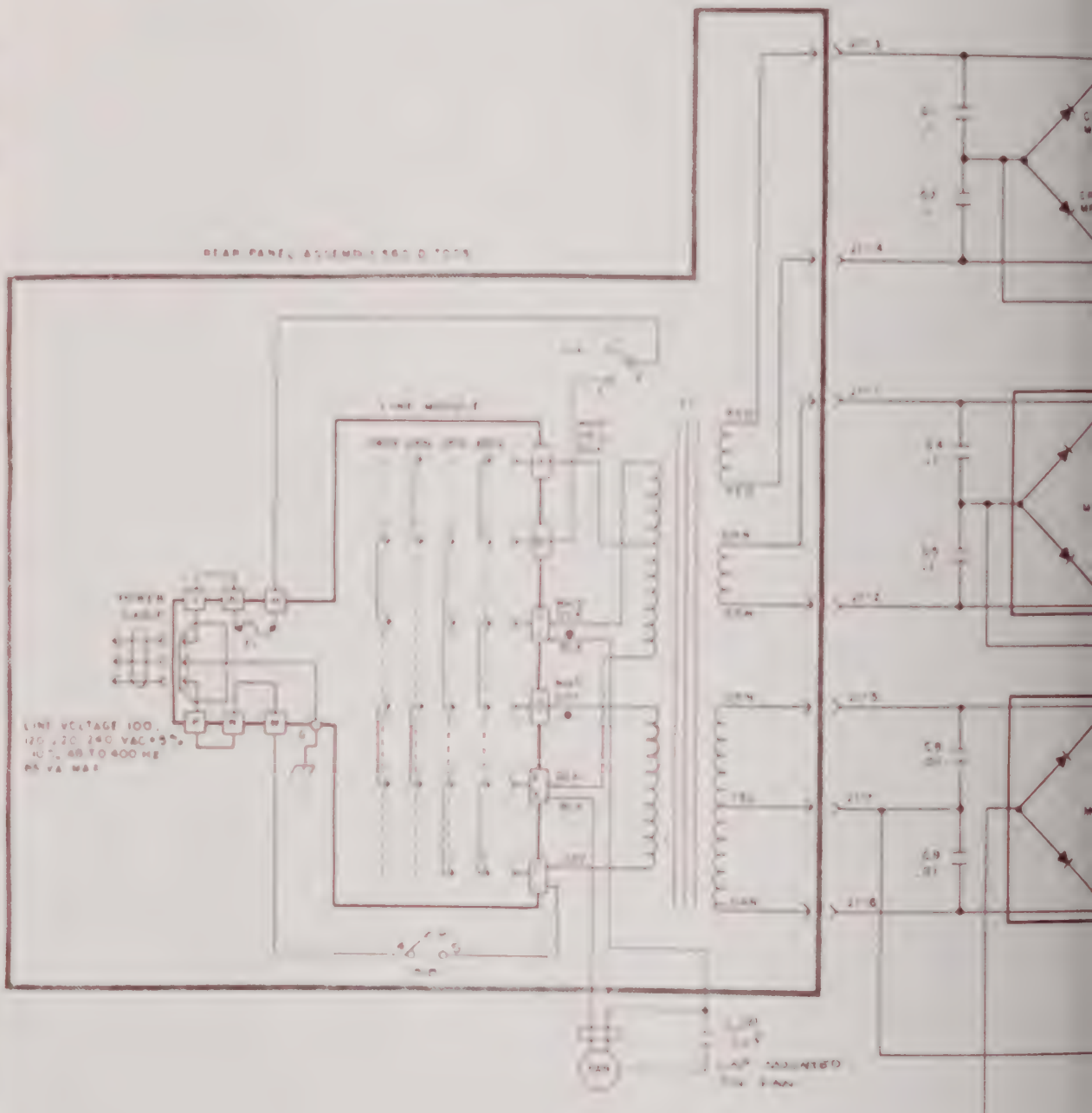


Figure 7-120. GPIB Connector (A7) PCB Schematic Diagram

Figure 7-119.



NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCE VALUES ARE IN OHMS. CAPACITANCE VALUES ARE IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W 1% METAL FILM.
3. ⏚ DENOTES CHASSIS GROUND.
4. B1 OMITTED ON MODEL 661.

REFERENCE DESIGNATORS	
LAST USED	NOT USED
R 8	
C 11	
CR 15	
Q 4	
VR 2	
S 1	
T 1	
F 1	

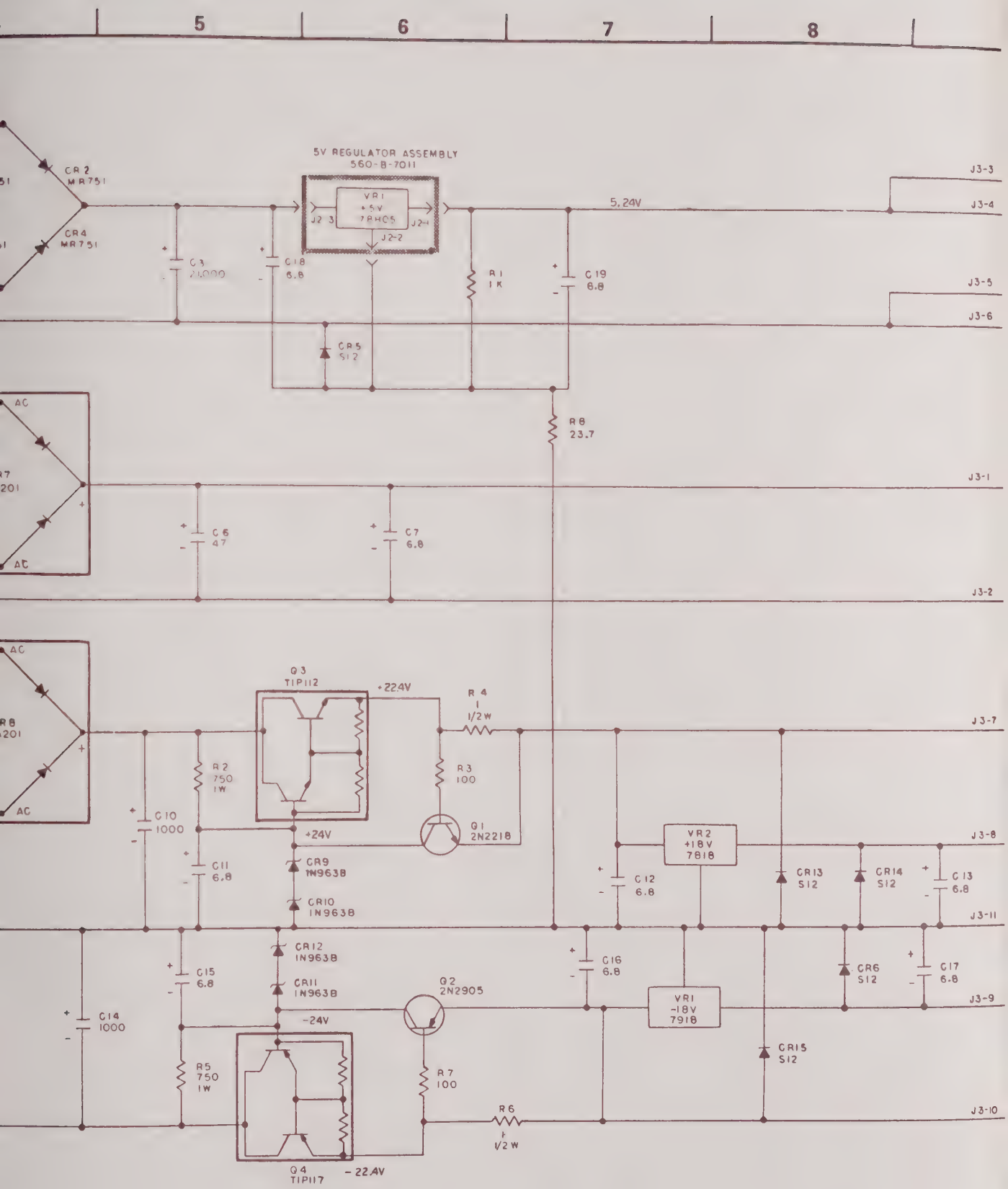


Figure 7-121. Power Supply (A4) PCB Schematic Diagram

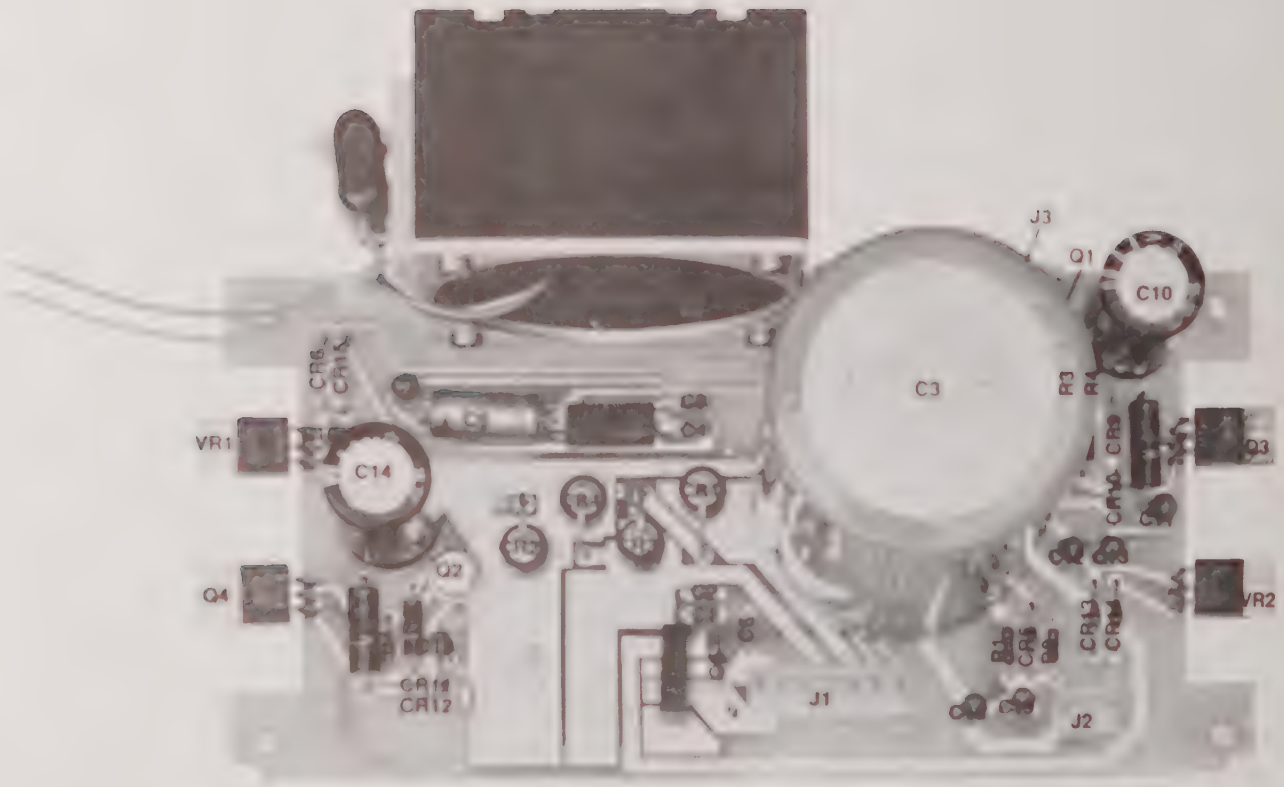


Figure 7-122. Power Supply (A4) PCB Parts Locator Diagram

7-10 POWER SUPPLY (A4) PRINTED CIRCUIT BOARD

This printed circuit board (PCB) provides five regulated dc voltages to the 560A network analyzer section, and one unregulated voltage to the 560A CRT mainframe section. The five regulated voltages include +5, +22, -22, +18, and -18 volts; the unregulated voltage is the 20-volt supply. The schematic for this circuit is shown in Figure 7-121, and the parts locator diagram is shown in Figure 7-122.

The input to the A4 PCB (Figure 7-121) is provided by the rear panel voltage selector module. This module allows the use of either of four international line voltages: 100, 115/120, 220, 230/240 Vac. The selected line voltage is applied, via the S1A and S1B sections of the front panel POWER switch, to the primary of transformer T1. The T1 secondary provides the input voltage for the 5, 20, and 22 volt bridge rectifier circuits.

The 5 volt bridge rectifier circuit consists of diodes CR1 thru CR4; its output voltage is applied to VR1, which is mounted on 5V Regulator Assembly 560-B-7011. To dissipate heat more efficiently, this assembly is mounted on the inside rear panel of the CRT mainframe. The output of the +5V regulator goes to the Digital (A2) PCB via connector A4J3, pin 4. The voltage output of the 5 volt supply is +5.24 ±0.2Vdc.

The 20 volt bridge rectifier circuit consists of diode bridge CR7. The output of CR7 is applied, via high frequency filter capacitors C6 and C7, to the CRT mainframe via connector J3, pins 1 and 2, and the Digital (A2) PCB. The voltage output of this circuit is unregulated and may vary between +17 and +22 Vdc.

The 22-volt bridge rectifier circuit consists of diode bridge CR8. The positive output of CR8 goes to the collector of Darlington transistor Q3; the negative output of CR8 goes to the collector of Darlington transistor Q4. The output voltages of Q3 and Q4 go to resistors R4 and R6, respectively.

Both R4 and R6 function as over-current sensing resistors. When the plus or minus 22V supply output current reaches 700mA, the voltage drop across R4 and R6 (0.7V) forward biases the respective Q1 or Q2 transistors. When forward biased Q1 and Q2 shunt the respective Q3 and Q4 transistors.

The output voltages of resistors R4 and R6 go to two places. The +22V output of R4 goes to +18V regulator VR2 and to connector J3, pin 7. The -22V output of R6 goes to -18V regulator VR1 and to connector J3, pin 10. The +18V output of VR2 goes to J3, pin 11, and the -18V output of VR1 goes to J3, pin 9. Connector J3 supplies these voltages to the network analyzer section via the Digital (A2) PCB. The output voltages of the 22 volt supply are +22 ± 1.0 Vdc and -22 ± 1.0 Vdc. The output voltages of the 18 volt supply are +18 ± 0.7 Vdc and -18 ± 0.7 Vdc.

7-11 INTERFACE CONTROL (A8) PRINTED CIRCUIT BOARD

This board generates signals for the Z-Axis Blanking and Retrace Blanking circuits. It also contains circuits for alternate-sweep mode, and for selecting either blanking output or pen lift mode. A block diagram that shows the interconnections between the A8 board, the Digital (A2) board, and the rear panel switches and connectors is shown in Figure 7-123. The A8 schematic is in Figure 7-125 and the parts locator diagram is in Figure 7-124.

A system of mnemonic symbols identifies the control and signal lines used between the A8 board and the rest of the 560A. Table 7-5 provides an alphabetical listing of these mnemonic symbols, including a "Definition," "To," and "From" column for each one.

Table 7-5. Listing of Mnemonic Symbols used with A8 PCB Circuits and Rear Panel Switches and Connectors

MNEMONIC	DEFINITION	FROM*	TO*
ALT1	Alternate 1. High-active state for alternate-sweep, Channel A display. Low-active state for alternate-sweep, Channel B display.	AUX I/O switch, Fig. 7-126/9G.	Fig. 7-125/1G via A8P2-4.
BIAS	Offset for ±8V Ramp Input.	Fig. 7-125/8F.	HORIZONTAL SELECT switch, Fig. 7-126/0D via A8P2-7.
BLANK INPUT	Blanking Input Signal.	Fig. 7-125/8D.	Fig. 7-81/0A via A2P8-5
BLANK OUT	Blanking Output Signal.	Fig. 7-88/9E.	Fig. 7-125/1F via A8P1-6.
BUF HOR OUT	Buffered Horizontal Output Signal.	Fig. 7-125/8D.	HORIZONTAL SELECT switch, Fig. 7-126/1C via A8P2-8.
COMP BLANK IN	Composite Blanking Input Signal.	Z AXIS SELECT connector, Fig. 7-126/3E.	Fig. 7-81/0F via A2P5-1.
CRT BLANKING	Blanking Output Signal.	Fig. 7-125/8F.	BLANK/PEN LIFT OUT connector, Fig. 7-126/1E via A8P2-8.
HCG	High Current Ground.	Fig. 7-62/9D.	Fig. 7-126/1B via A2J3-9, A2J3-13.
HO	Horizontal Output Ramp Signal.	Fig. 7-59 Sh. 2/9A	Fig. 7-125/1D via A8P1-8.
HOR BUFF IN	Buffered Horizontal Input Signal.	HORIZONTAL INPUT connector, Fig. 7-126/9C.	Fig. 7-125/1B via A8P2-11.
HORIZONTAL IN	Horizontal Input Signal.	HORIZONTAL SELECT connector, Fig. 7-126/9D.	Fig. 7-80/0F via A2P5-2.

* The numeric/alpha characters (e.g. 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

Table 7-5. Listing of Mnemonic Symbols used with A8 PCB Circuits and Rear Panel Switches and Connectors (Continued)

MNEMONIC	DEFINITION	FROM*	TO*
HOR OUT	Horizontal Output Signal.	Fig. 7-80/9F.	HORIZONTAL OUTPUT connector, via A2J3-12, Fig. 7-126/1C.
HRCDR/ LCRT	High-active state when OUTPUT MODE switch is in RCDR mode, low-active state when switch is in CRT mode.	Fig. 7-125/8G.	Fig. 7-89/0E via A2P8-7.
INT Z AXIS	Internal Z-Axis Signal.	Fig. 7-125/8D.	Z AXIS SELECT connector, Fig. 7-126/1E via A8P2-6.
LA	Low-active state, Input-Channel A Only Signal.	Fig. 7-125/8F.	Fig. 7-88/0G via A2P8-11.
LALTE	Low-active state, Alternate-Sweep Signal.	AUX I/O connector, Fig. 7-126/9F.	Fig. 7-125/1F via A8P2-3.
LAON	Low-active state, Channel A Only.	A ONLY switch, Fig. 7-126/9B.	Fig. 7-125/1F via A8P2-1.
LCG	Low Current Ground.	HORIZONTAL SELECT switch, Fig. 7-126/9D; Fig. 7-62/9D; Fig. 7-62/9C.	Fig. 7-62/9F via A2P8-1; Fig. 7-126/8G via A2P5-3; Fig. 7-125/1H via A8P1-4.
LDC	Low-active state, Data Valid Signal	Figure 7-81/9E	Fig. 7-62/0C Fig. 7-125/ via A2P8-10
LDV	Low-active state, Data Valid Signal	Fig. 7-81/9E	Fig. 7-62/0C Fig. 7-125/ via A2P8-10
L NORM/ H EXT	Low-active state when LOW LEVEL CAL switch is in NORM position; high-active state when switch is in EXT position.	LOW LEVEL CAL switch, Fig. 7-126/9B	Fig. 7-81/0C via A2J3-6.

*The numeric/alpha characters (e.g. 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

Table 7-5. Listing of Mnemonic Symbols used with A8 PCB Circuits and Rear Panel Switches and Connectors (Continued)

MNEMONIC	DEFINITION	FROM*	TO*
LRCDR/ HCRT	Low-active state when OUTPUT MODE switch is in RCDR position; high-active state when switch is in CRT position.	OUTPUT MODE switch, Fig. 7-126/9F.	Fig. 7-125/1G via A8P2-2.
MARKER IN	Marker Input Signal.	MARKER INPUT connector, Fig. 7-80/0A.	Fig. 7-126/8G via A2P5-4.
N. C.	Normally-Closed.	Fig. 7-88/9F.	Fig. 7-126/1F via A2P7-2.
N. O.	Normally-Open	Fig. 7-88/9F.	Fig. 7-126/1F via A2P7-3.
REAR PANEL GND	Rear Panel Ground for HORIZONTAL INPUT connector.	HORIZONTAL INPUT connector, Fig. 7-126/9C.	Fig. 7-125/1B via A8P2-10.
SYNC	Synchronize Alternate-Sweep Signal.	Fig. 7-125/8F.	Fig. 7-81/0F via A2P8-9
VERT OUT	Vertical Output Signal.	Fig. 7-80/9F.	VERTICAL OUTPUT connector, Fig. 7-126/1A via A2J3-3.

*The numeric/alpha characters (e.g. 9F, 0E, etc.) that follow the figure number(s) indicate the schematic grid coordinates.

7-11.1 Z-Axis Blanking

This circuit generates internal z-axis blanking for the 560A CRT during retrace and at bandswitch points. As shown in Figure 7-123, the Z-Axis Blanking circuitry consists of Buffer U1A; C1; Log Differentiator U1D; Inverting Amp U1C; Electronic Switch Q3; Sample & Hold U1B; Comparator U2C; Comparator U2D; C3; and Electronic Switch Q5.

The sweep ramp from the sweep generator is applied to Buffer U1A via the HORIZONTAL INPUT connector, HORIZONTAL SELECT switch, HORIZONTAL IN line, Digital (A2) board, and the HORIZONTAL OUT line. The U1A output is then sent to (1) Log Differentiator U1D and (2) the HORIZONTAL SELECT switch (paragraph 7-12.1).

Log Differentiator U1D has a logarithmic response to the sweep ramp and clamps its output between +0.7V and -0.7V. U1D responds to the sweep ramp as follows: (1) when the ramp is rising from 0 to +10V, the output is negative; (2) when the ramp is not rising, such as during a dwell or bandswitch point, the output is zero; and (3) when the ramp is falling from +10V to 0V during retrace, the output is positive. The output level of U1D depends on the duration of the sweep ramp; the faster the ramp, the closer the U1D output will be to the +0.7V and -0.7V limits. U1D then sends its output to Inverting Amp U1C. U1C clips off the negative pulse, but amplifies the positive pulse and sends it to (1) Electronic Switch Q3, and (2) Comparator U2C. Electronic Switch Q3, when turned on by Comparator U2D, allows the output from U1C to charge C3 to the level corresponding to a rising ramp. Comparator U2D has the ramp voltage at its inverting (-) input via the HORIZONTAL OUTPUT line from the A2 board. The U2D output goes positive for only a short time period, which corresponds with the beginning of the sweep ramp. When the U2D output is positive, it turns on Electronic Switch Q3, to allow the output from U1C to charge C3 to the level corresponding to a rising ramp. Sample & Hold U1B holds the voltage of C3 and outputs that voltage level to the noninverting (+) input of Comparator U2C.

Comparator U2C then compares the reference voltage at its noninverting input to the varying voltage level at its inverting input that was established by the pulse from U1C. During a dwell or bandswitch point on the sweep ramp, the output of U2C jumps from 0 to +5V, because the voltage level of the U1C pulse, which is falling from a positive level toward 0V, is now less than the reference voltage. At the end of a dwell on the sweep ramp, the output of U2C is turned off (0V), because the voltage level of the U1C pulse, which is rising from 0V to a positive level, is now greater than the reference voltage.

The U2C output is sent (1) to the Digital (A2) board via the INT Z-AXIS line, Z-AXIS SELECT switch, and the COMP BLANK IN line and (2) to OR Circuit CR5, CR6.

The above blanking cycle repeats for each dwell on the sweep ramp, until the sweep ramp returns to 0V during retrace. During retrace, Comparator U2A turns on Electronic Switch Q5 to discharge C3, so that the next sweep ramp is able to start the blanking cycle over again. Refer to paragraph 7-11.2 for an explanation of how U2A turns on Electronic Switch Q5.

7-11.2 Internal Retrace Blanking

This circuit generates blanking signals for the 560A Digital board circuitry. As shown in Figure 7-123, the blanking circuitry consists of Peak Detector U3A,U3B; Comparator U2A; Comparator U2B; Electronic Switch Q6; OR Circuit CR5, CR6; and C5.
and C5.

As shown in Figure 7-123, the input to the blanking circuitry is the sweep ramp from the Digital board, which is sent over the HO and HORIZONTAL OUTPUT lines. This ramp is applied to four places: (1) Peak Detector U3A, U3B; (2) Comparator U2A; (3) Comparator U2B; and (4) Comparator U2D. Refer to paragraph 7-11.1.

Peak Detector U3A continually samples the

sweep ramp as it rises from 0V to +10V. When the ramp reaches its peak value of +10V, C5 charges to this peak value. This voltage is applied to the noninverting (+) input of Comparator U2A via U3B and acts as a reference voltage for U2A. Although the sweep ramps applied to Comparator U2A and to Peak Detector U3A, U3B are identical, the ramp applied to the inverting (-) input of U2A is offset by a voltage that causes U2A to remain turned off (0V). Then, as the sweep ramp falls to 0V during retrace, the inverting input voltage also falls toward 0V, while the voltage at the noninverting input of U2A remains at a positive level. These input conditions cause U2A to produce a positive blanking pulse, which is sent to the A2 board over the BLANK INPUT line.

At the end of retrace the LDV line from the A2 Digital PCB resets the blanking circuitry. If the LDV line fails to supply a pulse at the end of retrace, Comparator U2B turns on the electronic switch.

Comparator U2B compares the sweep ramp at its inverting input to a fixed voltage at its noninverting input. At the end of retrace, as the ramp falls toward 0V, the voltage at the noninverting input will be greater than the voltage at the inverting input. These input conditions cause U2B to output a positive pulse, which turns on Electronic Switch Q6.

7-11.3 Alternate-Sweep Capability

Alternate-Sweep capability allows the 560A to process and then display two swept-frequency ranges with only one RF detector connected to the Channel A input. The 560A simultaneously displays the two swept-frequency ranges by multiplexing the output of the Log (A3) board (paragraph 7-7.21).

As shown in Figure 7-123, when a sweep generator with alternate-sweep capability (such as the WILTRON 6600A Series Programmable Sweep Generator) is connected to the rear panel AUX I/O connector, it sends out--among other signals described in paragraph 7-12.2--two alternate-sweep control signals: Alternate Sweep and Alternate 1.

Alternate Sweep (LALTE) goes LOW to indicate to the 560A that the sweep generator is in the alternate-sweep mode. This signal from the sweep generator is sent over the LA line to the Digital (A2) board via CR9.

Alternate 1 (ALT1) goes HIGH for Channel A display or LOW for Channel B display. This signal from the sweep generator synchronizes the switching of the Channel A and Channel B inputs with the multiplexing of the Channel A and Channel B alternate-sweep input to the A3 board (see paragraph 7-7.12).

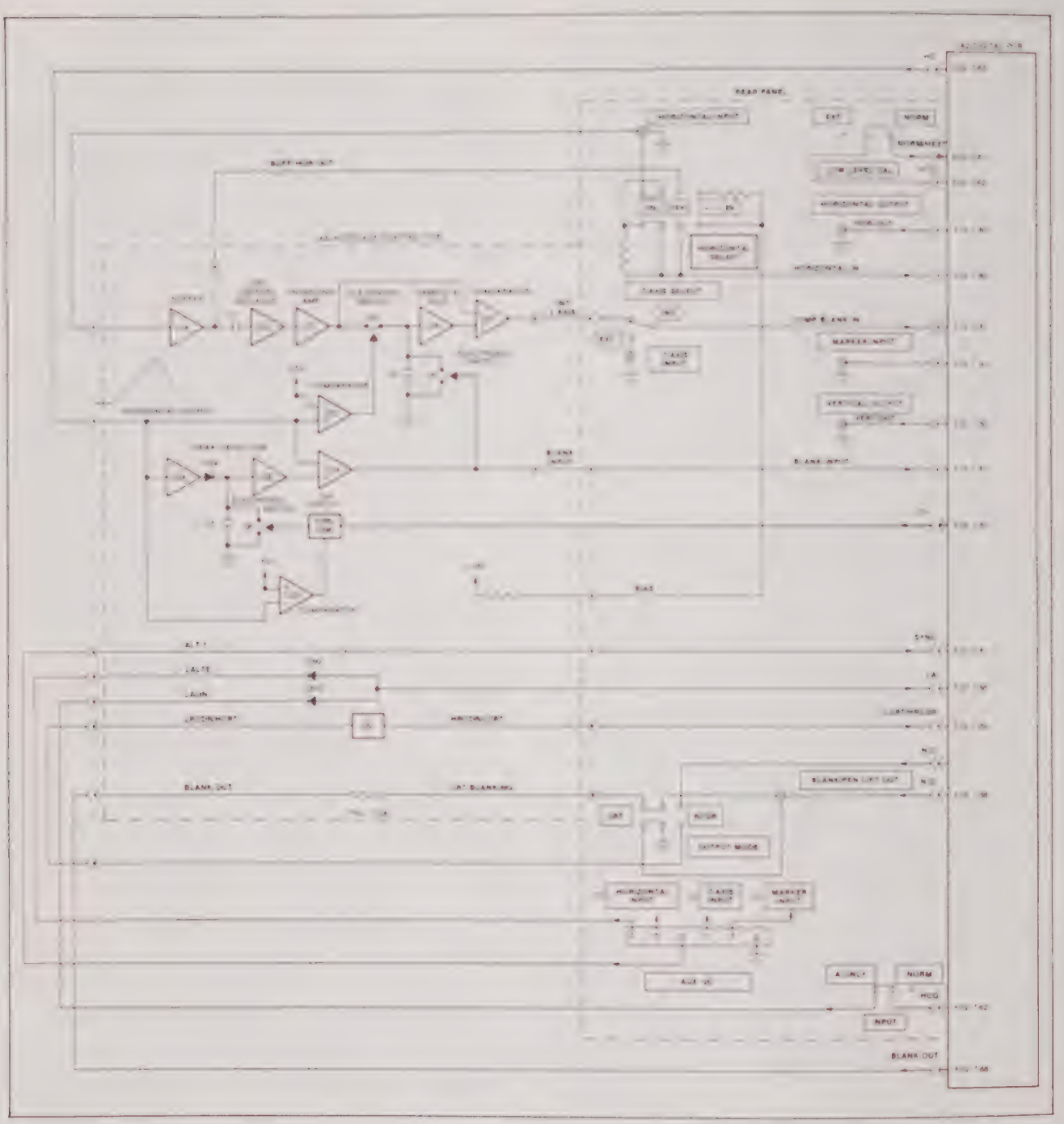


Figure 7-123. Interface Control (A8) PCB and Rear Panel Block Diagram

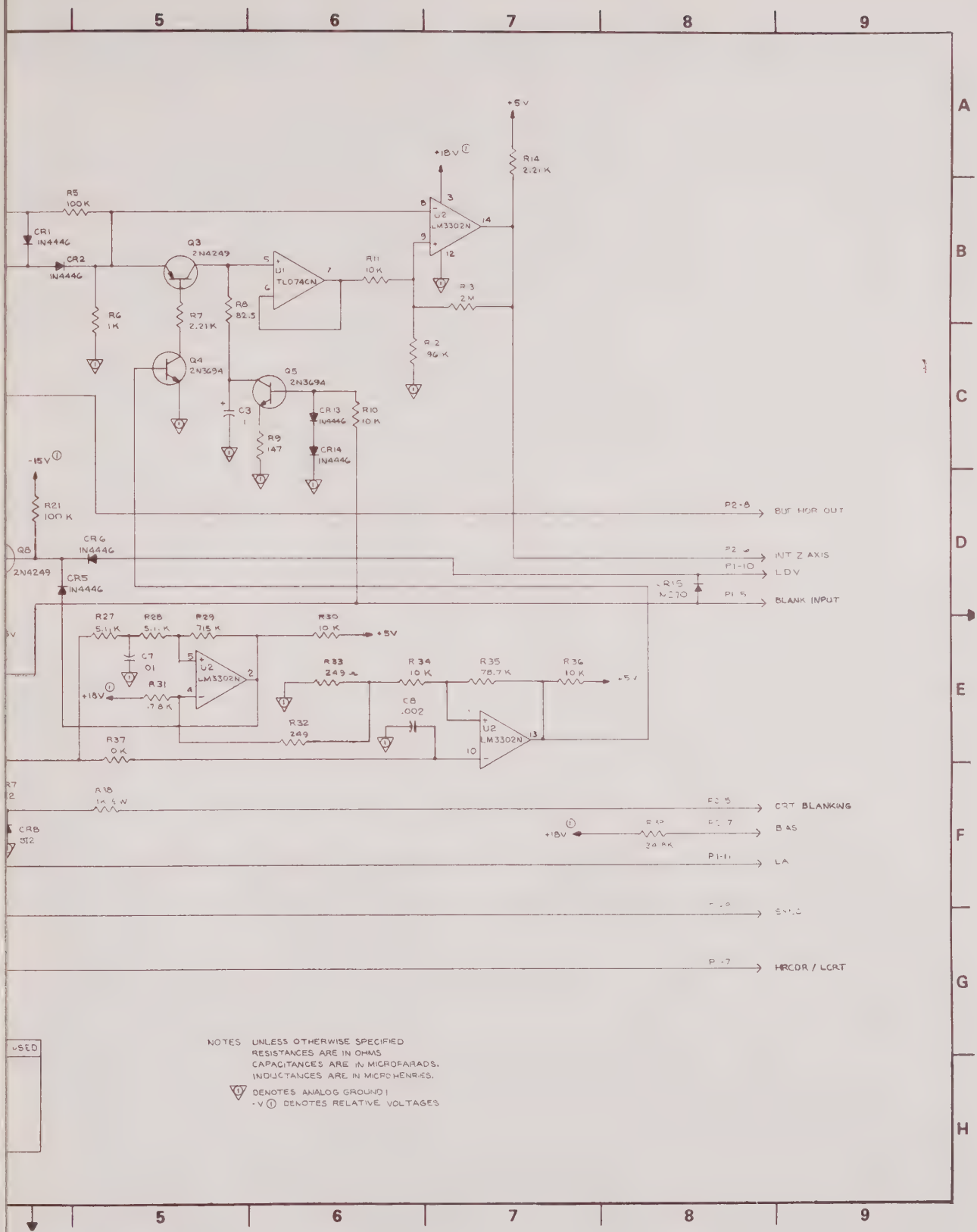


Figure 7-125. Interface Control (A8) PCB Z-Axis Blanking, CRT Blanking, and Alternate-Sweep Schematic Diagram

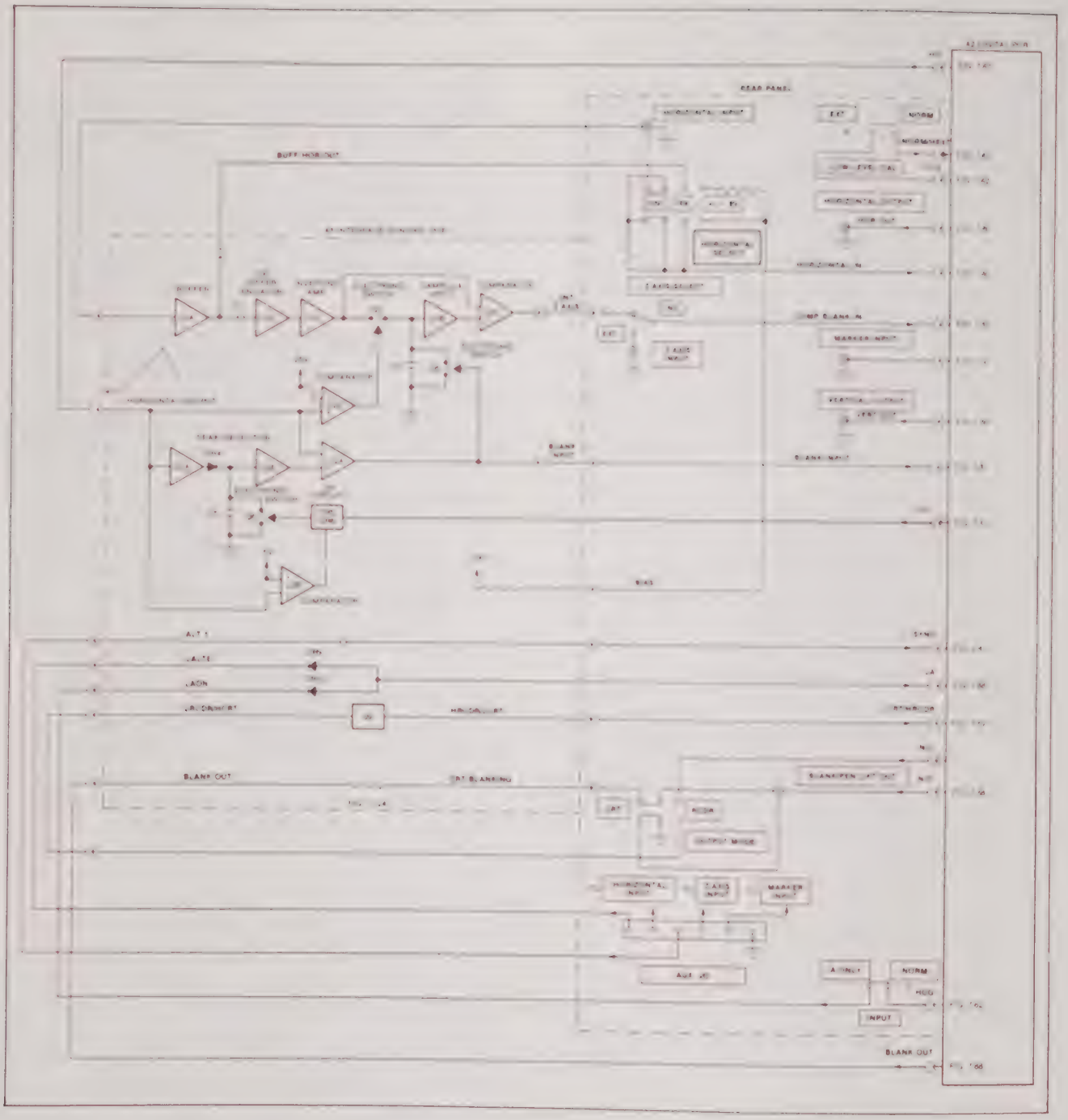


Figure 7-123. Interface Control (A8) PCB and Rear Panel Block Diagram

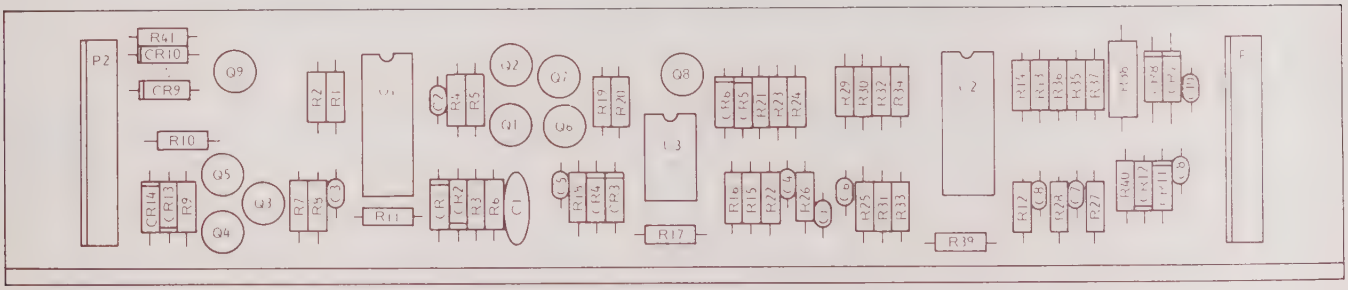
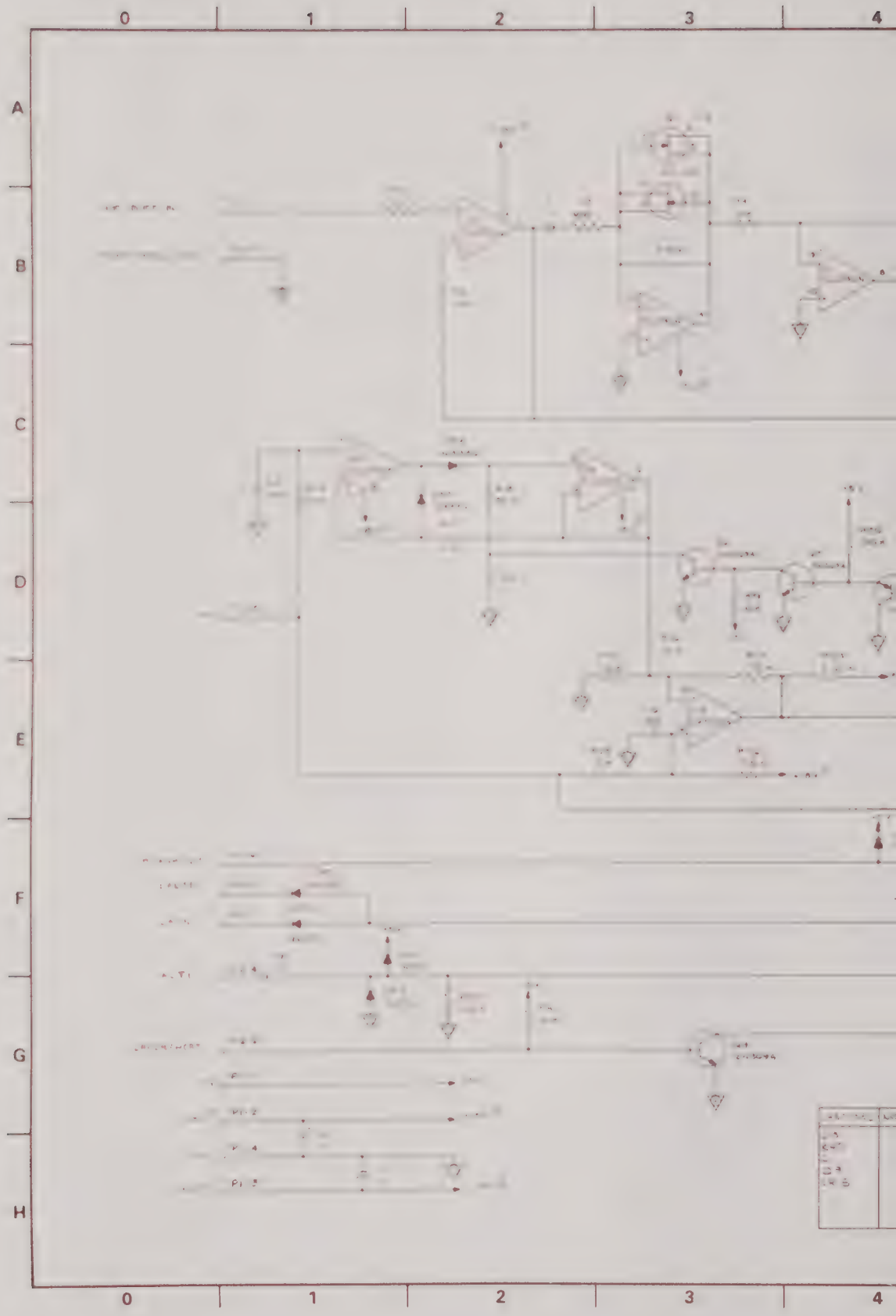


Figure 7-124. Interface Control (A8) PCB Parts Locator Diagram


0
1
2
3
4
A
B
C
D
E
F
G
H

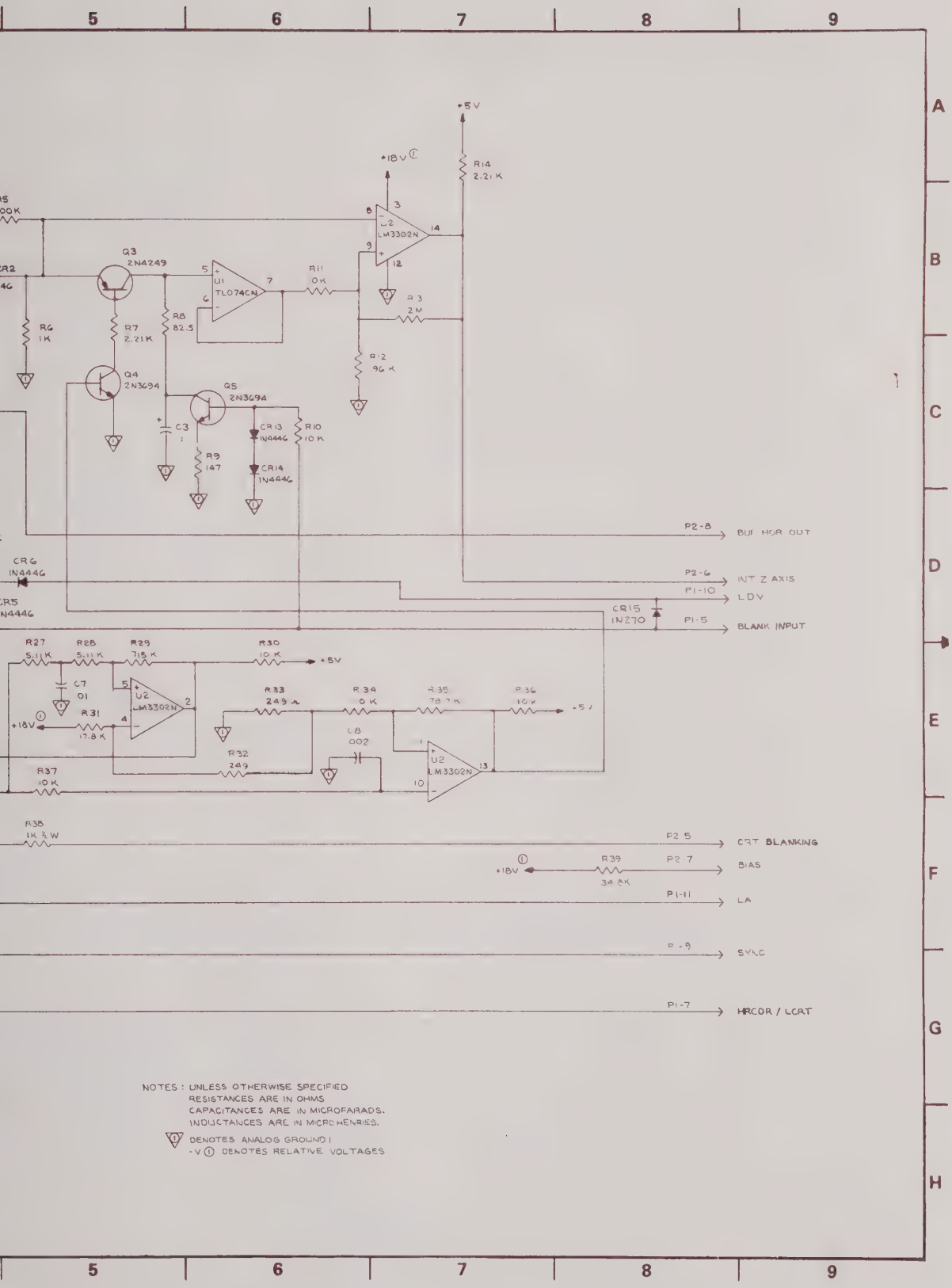


Figure 7-125. Interface Control (A8) PCB Z-Axis Blanking, CRT Blanking, and Alternate-Sweep Schematic Diagram

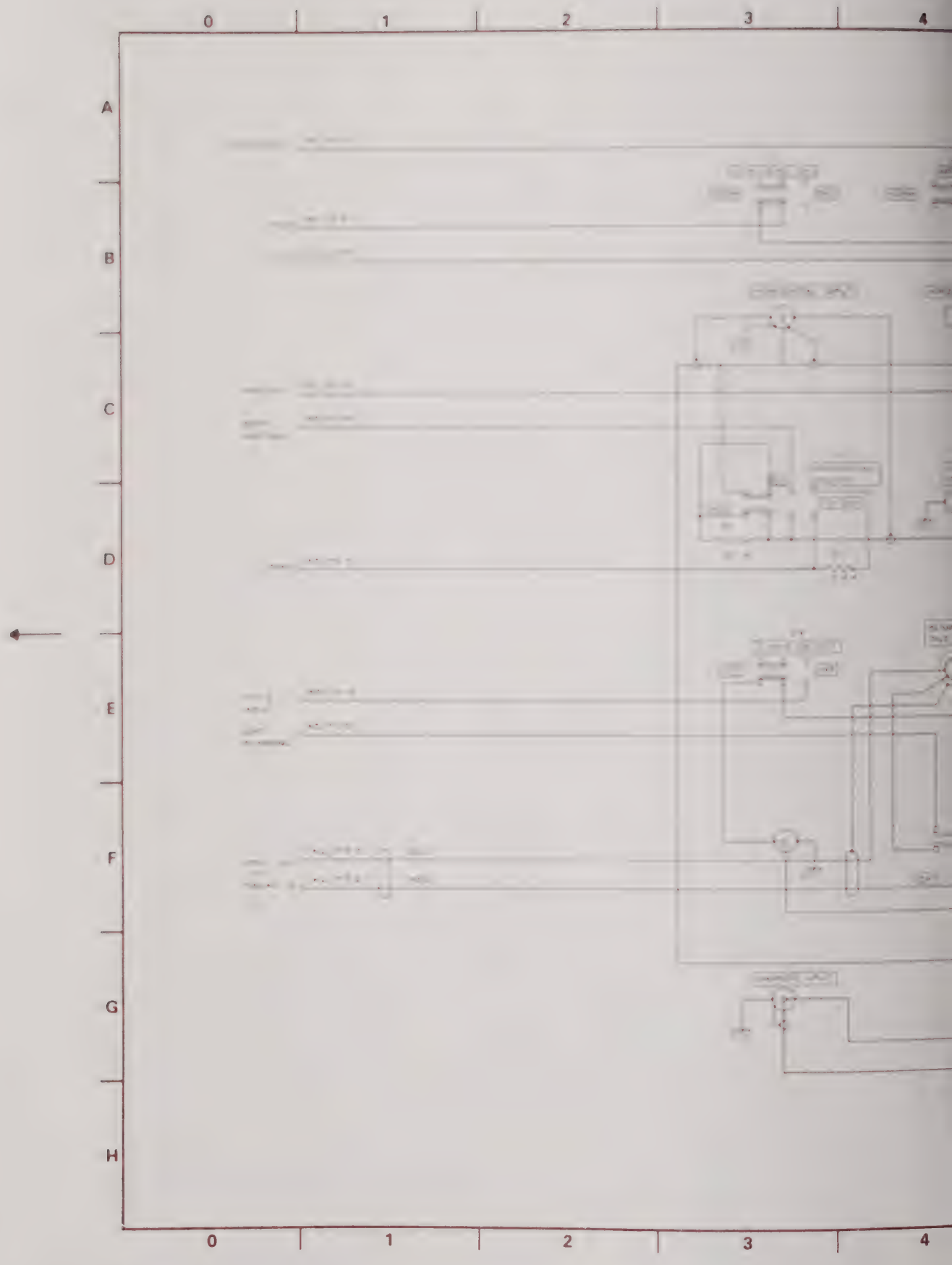


Figure 7-126. Rear Panel Interconnection Schematic

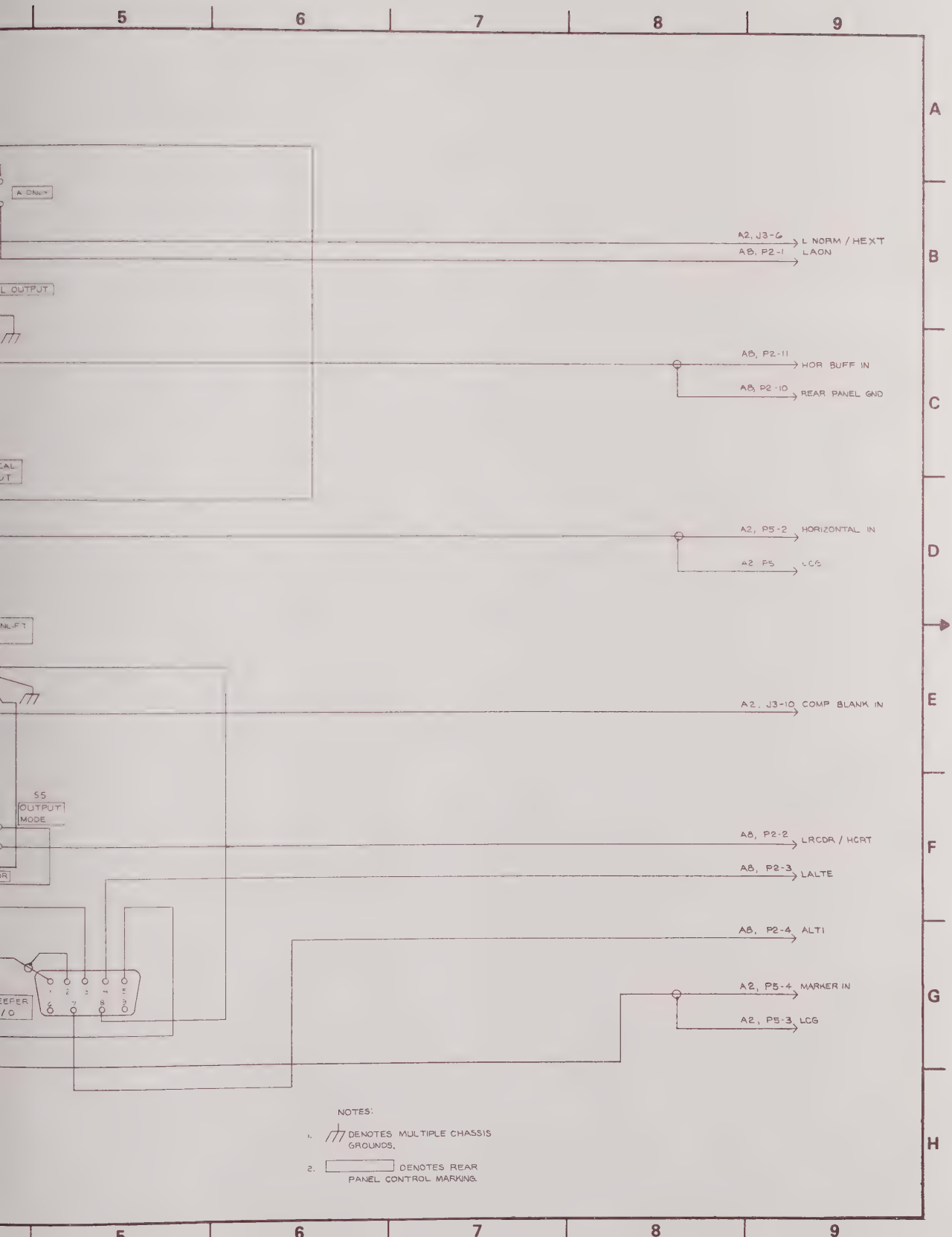

5
6
7
8
9
A
B
C
D
E
F
G
H
A ONLY
L OUTPUT
A2, J3-6
L NORM / HEXT
A8, P2-1
LAON
A8, P2-11
HOR BUFF IN
A8, P2-10
REAR PANEL GND
A2, P5-2
HORIZONTAL IN
A2 P5
LCG
A2, J3-10
COMP BLANK IN
S5
OUTPUT
MODE
A8, P2-2
LRCDR / HCRT
A8, P2-3
LALTE
A8, P2-4
ALTI
A2, P5-4
MARKER IN
A2, P5-3
LCG
NOTES:
1. DENOTES MULTIPLE CHASSIS GROUNDS.
2. DENOTES REAR PANEL CONTROL MARKING.

Figure 7-126.

7-12 A9 REAR PANEL ASSEMBLY

The A9 Rear Panel Assembly contains the rear panel switches, connectors, and associated components. The schematic is shown in Figure 7-126.

7-12.1 Rear Panel Switches

The rear panel switches are described below. See Figure 7-123.

a. LOW LEVEL CAL switch. See paragraph 7-7.16.

b. INPUT switch. This switch has two modes--NORM and A ONLY. In the NORM position, the 560A CRT displays either Channel A, Channel B, or both--depending upon the front panel control settings. In the A ONLY position, a ground condition (HCG) is sent to the Digital (A2) board via the INPUT switch, the LAON line, CR10 on the Interface Control (A8) board, and the LA line. In the A ONLY position, the 560A displays only the Channel A input on Channel A, Channel B, or both--depending upon the front panel control settings.

c. Z AXIS SELECT switch. This switch has two modes: INT and EXT. In the INT position, the Z-Axis Blanking circuitry supplies the Digital (A2) board with blanking pulses, as described in paragraph 7-11.1. In the EXT position, an external blanking source connected to the Z AXIS input connector supplies the necessary blanking pulses to the A2 board.

d. HORIZONTAL SELECT switch. This switch has three modes: 10V, 15V, and +/- 8V. In the 10V position, the 0 to +10V sweep ramp that is applied to the HORIZONTAL INPUT connector is sent over the HORIZONTAL INPUT line to the Digital(A2) board via the HORIZONTAL SELECT switch. In the 15V position, the 0 to 15V sweep ramp applied to the HORIZONTAL INPUT connector is sent to the A2 board via the HOR BUFF IN line, Buffer U1A, and the BUFF HOR OUT line on the Interface Control (A8) board; the HORIZONTAL SELECT switch; and the HORIZONTAL IN line. The resistor in series with the HORIZONTAL IN line places an additional resistance at the input of a buffer amplifier on the A2 board. This additional resistance decreases the gain of the buffer amplifier, so that its output is a 0 to +10V ramp. In the ±8V position, the -8 to +8V sweep ramp follows the same path as the 0 to +15V sweep ramp. In addition, an offset voltage is applied to the sweep ramp via the BIAS line. This voltage cancels the 8V offset in the sweep ramp to produce a 0 to +16V ramp. The resistor in series with the HORIZONTAL IN line decreases the gain of the buffer amplifier on the A2 board, so that its output is a 0 to +10V ramp.

e. OUTPUT MODE switch. This switch has two positions: CRT and RCDR. In the CRT mode, the switch places a HIGH on the LRCDR/HCRT line, which goes to the Interface Control (A8) board. Q9 on the A8 board inverts the signal and then places a LOW on the HRCDR/LCRT line, which is sent to the Digital (A2) board. When this line is LOW, the A2 board sends blanking pulses to the BLANK/PEN LIFT OUT connector via the BLANK OUT line. In the RCDR position, the switch places a LOW on the LRCDR/HCRT line. Q9 on the A8 board inverts the signal and then places a HIGH on the HRCDR/LCRT line, which

is sent to the A2 board. When this line is HIGH, the A2 board connects the normally-open relay contacts to the BLANK/PEN LIFT OUT connector via the N.O. line.

7-12.2 Rear Panel Connectors

The rear panel connectors are listed below. See Figure 7-123.

a. HORIZONTAL OUTPUT. Refer to paragraph 7-7.11.

b. VERTICAL OUTPUT. Refer to paragraph 7-7.10.

c. Z AXIS SELECT - EXT. Refer to paragraph 7-12.1 (under Z AXIS SELECT).

d. MARKER INPUT. Refer to paragraph 7-7.11.

e. BLANK/PEN LIFT OUT. Refer to paragraph 7-12.1 (under OUTPUT MODE).

f. AUX I/O. This connector is wired in parallel with the rear panel MARKER INPUT, Z AXIS SELECT-EXT, HORIZONTAL INPUT, and BLANK/PEN LIFT OUT connectors. It also has two alternate-sweep control signals (paragraph 7-11.3).

7-13 CRT MAINFRAME

The 560A CRT mainframe is the Tektronix Model 620 Monitor, containing Options 1 and 31. The theory of operation, schematics, and parts locator diagrams that follow are from the 620 Monitor Instruction Manual; they are reprinted by permission of Tektronix, Inc. The information included under this paragraph heading (e.g. text, illustrations, and schematics) should be sufficient to support maintenance and troubleshooting of the CRT mainframe.

7-13.1 Block Diagram

The following discussion is provided to aid in understanding the overall concept of the 620 Monitor before the individual circuits are discussed in detail. A basic block diagram is shown in Figure 7-127.

Vertical and horizontal signals to be displayed on the CRT are supplied to the deflection amplifiers through the appropriate Y and X Input connections. The deflection amplifiers process the input signals and provide push-pull outputs to drive the deflection plates of the CRT. Both deflection amplifiers contain position and gain controls.

The Z-Axis Amplifier controls the display intensity by providing a voltage to drive the CRT control grid. Input signals are applied to the A1 PCB Z Input connection.

The High-Voltage and Low-Voltage Power Supplies provide all the voltages necessary for operation of this instrument.

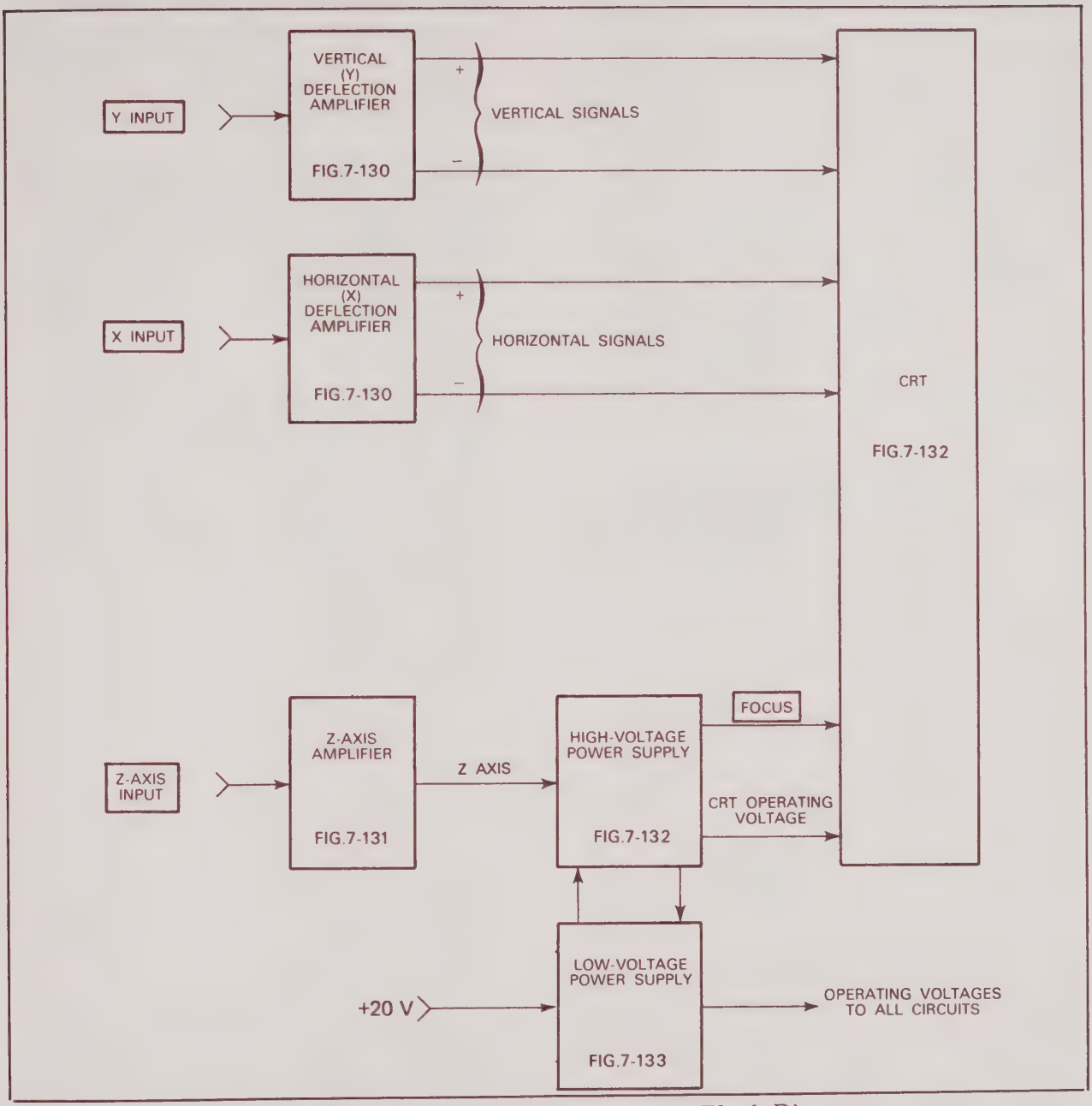


Figure 7-127. CRT Mainframe Block Diagram

7-13.2 Deflection Amplifiers

The Vertical (Y) and Horizontal (X) Deflection Amplifiers convert single-ended input signals to push-pull outputs suitable to drive the deflection plates of the CRT. A schematic diagram of the deflection amplifiers is shown in Figure 7-130.

a. Vertical Deflection Amplifier. The Vertical (Y) Deflection Amplifier consists mainly of two noninverting operational amplifiers. A1Q123A-A1Q136-A1Q141 and A1Q123B-A1Q186-A1Q191, which provide amplified push-pull signals to drive the vertical deflection plates of the CRT.

Signals to be displayed on the CRT are applied to J13 in the 620/Option 31 Monitor. A matched dual field-effect transistor (A1Q123A and A1Q123B) provides high input impedance and temperature stability. Excessively large negative-going signals are diode-clamped by A1CR122 at the gate of A1Q123A to protect the FET. The Y Gain control, A1R125, allows setting the CRT full-screen deflection sensitivity. This control is set at the factory for 8 divisions of deflection with a 1-volt input signal applied. Provisions have been made for the addition of an attenuating resistor (in place of A1W113) if signals much larger than the nominal 1 volt are to be applied to the input.

A2 PCB control A2R305 provides vertical positioning by setting the bias at the gate of A1Q123B.

The push-pull signals from A1Q123A and A1Q123B are held to within about 1.4 volts of each other by diodes A1CR175, A1CR176, A1CR177, and A1CR178 to improve overdrive recovery of the amplifier. The signals are then applied to emitter-followers A1Q136 and A1Q186, which provide drive for the output transistors. Transistors A1Q141 and A1Q191 provide final amplification of the vertical signals before they are applied to the CRT deflection plates. Quiescently, the output voltage (with the CRT beam positioned to center-screen) is about -26 volts. Feedback is provided by A1R133-A1C133 and A1R183-A1C183. High-frequency compensation is provided by A1R129-A1C128.

b. Horizontal Deflection Amplifier. The Horizontal (X) Deflection Amplifier consists mainly of two noninverting operational amplifiers, A1Q223A-A1Q236-A1Q241 and A1Q223B-A1Q286-A1Q291, which provide amplified push-pull signals to drive the horizontal deflection plates of the CRT.

Signals to be displayed on the CRT are applied to J18 in the Option 31 620 Monitor. A matched dual field-effect transistor (A1Q223A and A1Q223B) provides high input impedance and temperature stability. Excessively large negative-going signals are diode-clamped by A1CR222 at the gate of A1Q223A to protect the FET. The X Gain control, A1R225, allows setting the CRT full-screen deflection sensitivity. This control is set at the factory for 8 divisions of deflection with a 1-volt input signal applied. Provisions have been made for the addition of an attenuating resistor (in place of A1W213) if signals much larger than the nominal 1 volt are to be applied to the input.

The front panel HORIZ POSITION control, A2R315, provides horizontal positioning by setting the bias at the gate of A1Q223B.

The push-pull signals from A1Q223A and A1Q223B are held to within 1.4 volts of each other by diodes A1CR275, A1CR276, A1CR277, and A1CR278 to improve overdrive recovery of the amplifier. The signals are then applied to emitter-followers A1Q236 and A1Q286, which provide drive for the output transistors. Transistors A1Q241 and A1Q291 provide final amplification of the horizontal signals before they are applied to the CRT deflection plates. Quiescently, the output voltage (with the CRT beam centered) is about -26 volts. Feedback is provided by A1R223-A1C223 and A1R283-A1C283. High-frequency compensation is provided

by A1R229-A1C228.

7-13.3 Z-Axis Amplifier

The Z-Axis Amplifier provides the drive signal to control the CRT intensity. A schematic diagram of the Z-Axis Amplifier is shown in Figure 7-131. A detailed block diagram showing each major stage is superimposed on the schematic diagram with wide shaded lines. The stage names (given as subheadings in the following discussion) can be found in the shaded boxes in Figure 7-132.

a. Z Preamplifier. Single-ended input signals are applied to J26 in the 620/Option 31 Monitor. A matched dual FET (A1Q353A and A1Q353B) provides high input impedance and temperature stability. Excessively large negative-going signals are diode-clamped by A1CR351 at the gate of A1Q353A to protect the FET. Provisions have been made for the addition of an attenuating resistor (in place of A1W343) if signals much larger than the nominal 1 volt are to be applied to the input.

FET A1Q353A functions as a source follower, with source current provided by A1Q353B. The output of A1Q353 is applied to the base of A1Q354. Front-panel INTENSITY control A1R325 sets the voltage at the base of A1Q334. Transistors A1Q334-A1Q354 are connected in a differential configuration; however, only one output is applied to A1Q327. A positive input signal will increase the display intensity. When these straps are connected to the N terminals, a negative input signal will increase the display intensity. In either case, however, rotating the INTENSITY control clockwise will increase display brightness.

The Z-Axis signal at the base of A1Q354 is amplified by A1Q354 and applied across common-base transistor A1Q327.

b. Limiter. Diodes A1CR361-A1CR362-A1CR363-A1CR364 act to limit the output signal from the Z Preamplifier to within about 1 volt of ground. This maintains the Z Output Amplifier in the active state and prevents saturation of the amplifier transistors.

c. Z Output Amplifier. The Z Output Amplifier is a current-driven operational amplifier consisting of active components A1Q367-A1Q369-A1Q379. Feedback for the amplifier is provided by A1R372-A1R371-A1C371. Components A1CR381-A1CR382-A1R382 provide voltage-surge protection in the event of a high-voltage malfunction. The Z-Axis output signal is applied to the CRT control grid through the Control Grid DC Restorer network (Figure 7-128) to control the CRT beam intensity.

7-13.4 High Voltage Power Supply

The High-Voltage Power Supply provides the voltage levels and control circuits necessary for operation of the cathode ray tube (CRT). A schematic diagram of the High-Voltage Power Supply is shown in Figure 7-132. A detailed block diagram, showing each major stage of the circuit, is superimposed on the schematic diagram with wide shaded lines. The stage names (given as sub-headings in the following discussion) can be found in the shaded boxes in Figure 7-132.

a. High Voltage Oscillator. A repetitive, sinusoidal signal is produced by a regenerative feedback oscillator in the primary of A2T110 and induced into the secondary. Current drive for the primary winding is supplied by Q35. The conduction of Q35 is controlled by the output voltage of the Error Amplifier.

b. Cathode Supply. The Cathode Supply, -2250 volts, is produced by voltage doubler A2C116-A2CR116-A2CR117. This voltage is then filtered by A2C121-A2R-122-A2C123 before being applied to the CRT cathode (pin 2 of V39). The Cathode Supply is regulated by the Error Amplifier.

c. Error Amplifier. Regulation of the Cathode Supply voltage is accomplished by applying a sample of the -2250 volts from voltage divider A2R163C-A2R163D-A2R183 to the positive input (pin 3) of A2U175A. If the output level of the Cathode Supply exceeds the normal -2250 volts (becomes more negative), the voltage at pin 3 of A2U175A goes negative from its quiescent zero-volt level. This results in the output voltage from A2U175A becoming more negative, which in turn controls A2Q173. A more negative potential from the Error Amplifier reduces conduction of the High-Voltage Oscillator, resulting in a smaller peak-to-peak amplitude of the signal in the secondary of A2T110 and returning the Cathode Supply to -2250 volts.

d. Control Grid Restorer. The Control-Grid DC Restorer couples the dc and low-frequency components of the Z-Axis Amplifier output signal to the CRT control grid (pin 3 of V39). This allows the Z-Axis Amplifier to control the CRT beam intensity. The potential difference between the Z-Axis Amplifier output level and the CRT control grid (about -2250 volts) prohibits direct coupling.

The Control-Grid DC restorer is actually a cathode-referenced bias supply for the CRT control grid. Quiescently, its output voltage is more negative than the CRT cathode by an amount determined by the Z-Axis Amplifier output level and the setting of the CRT Bias adjustment (A2R130), in conjunction with A2VR130 and A2C131. (The cutoff voltage at the CRT control grid is typically about 65 volts more negative than the CRT cathode level.)

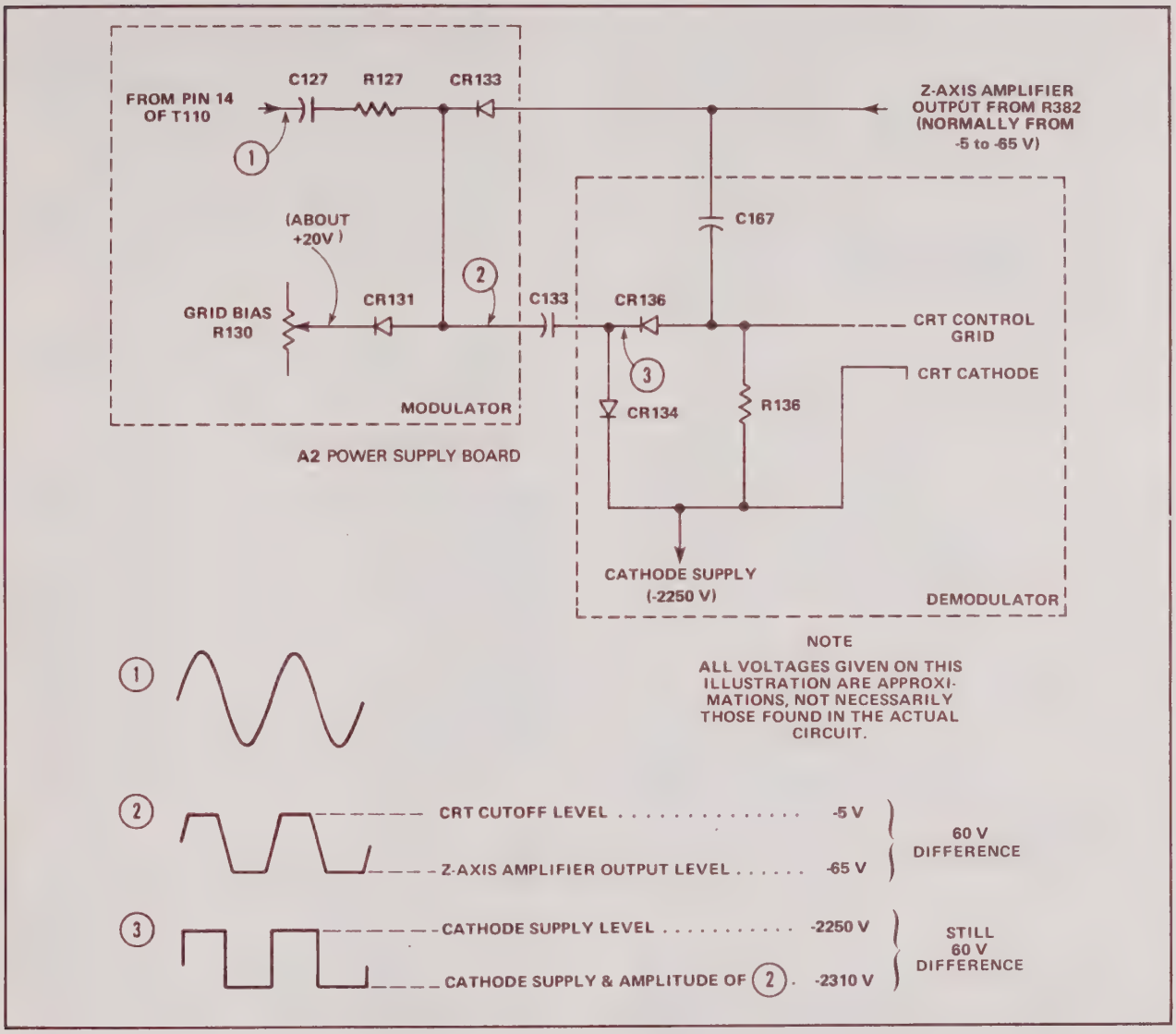

FROM PIN 14 OF T110
C127
R127
CR133
Z-AXIS AMPLIFIER OUTPUT FROM R382 (NORMALLY FROM -5 to -65 V)
(ABOUT +20V)
GRID BIAS R130
CR131
C133
CR136
C167
CRT CONTROL GRID
CRT CATHODE
CR134
R136
MODULATOR
A2 POWER SUPPLY BOARD
CATHODE SUPPLY (-2250 V)
DEMODULATOR
NOTE
ALL VOLTAGES GIVEN ON THIS ILLUSTRATION ARE APPROXIMATIONS, NOT NECESSARILY THOSE FOUND IN THE ACTUAL CIRCUIT.
CRT CUTOFF LEVEL . . . . . -5 V
Z-AXIS AMPLIFIER OUTPUT LEVEL . . . . . -65 V
60 V DIFFERENCE
CATHODE SUPPLY LEVEL . . . . . -2250 V
CATHODE SUPPLY & AMPLITUDE OF (2) . -2310 V
STILL 60 V DIFFERENCE

Figure 7-128. Control Grid DC Restorer Circuit

NOTE

A simplified diagram of the Control-Grid DC Restorer is shown in Figure 7-128. The voltages given on this diagram are idealized levels and will not necessarily be the same as those found in the actual instrument.

The Control-Grid DC Restorer is divided into two sections for ease of explanation. The first section can be considered a modulator at low-voltage potentials, and the remaining section as a demodulator at high-voltage potentials (see Figure 7-128).

1. Modulator. When the secondary winding output of A2T110 (pin 10) swings positive, A2C133 charges through A2C127 and A2R127 to a voltage level determined by the setting of the CRT Bias adjustment, in conjunction with A2VR130 and A2C131. At this voltage

level (approximately 65 volts), diode A2CR131 conducts, preventing any additional increase in the positive voltage across A2C133. When the secondary winding swings negative, diode A2CR131 turns off. Then A2CR133 conducts and clamps the negative excursion at A2C133 to the voltage level of the Z-Axis output level and the CRT Bias adjustment setting. (See waveform 2 in Figure 7-128. This square wave is coupled through A2C133 to the Demodulator.

2. Demodulator. The Demodulator rectifies the signal from the Modulator and references it to the CRT Cathode Supply level. The positive swing of waveform 3, Figure 7-128, is limited by A2CR134 to the level of the Cathode Supply; the negative excursion is coupled through A2CR136 to A2C167. Quiescently, A2C167 will charge to about -2250 volts through A2R136. After repetitive cycles from A2C133, A2C167 will charge to the negative level of waveform 3. Capacitor A2C167 holds the voltage constant at the CRT control grid, and also provides a path for the ac portions of the Z-Axis Amplifier output signal to be coupled to the CRT control grid.

   The remainder of the components not shown on the simplified diagram in Figure 7-128 provide circuit protection in the event of a high-voltage arc or other malfunction.

e. Unregulated Power Supply. The -75 volts unregulated is produced by voltage doubler A2C139-A2CR139-A2CR140. It is then filtered by A2C140, before being applied to the -70 Volt Regulated Supply, Figure 7-133.

   The -20 volts unregulated is produced by voltage doubler A2C142-A2CR142-A2CR143. It is then filtered by A2C143 before being applied to the 15 Volt Regulated Supply, Figure 7-133.

f. CRT Interconnects. The Astig screwdriver adjustment, A2R160, which is used in conjunction with the front-panel FOCUS control (A2R165) to provide a well-defined display, varies the negative level on the astigmatism element of the CRT.

   The Geom screwdriver adjustment, A2R155, varies the negative level on the geometry element to control the overall geometry of the display.

   The voltage divider A2VR150-A2R150 provides approximately -33 volts dc for additional CRT elements.

7-13.5 Low-Voltage Power Supply

The Low-Voltage Power Supply provides the operating power for the monitor. Electronic regulation is used to provide stable, low-ripple output voltages. A schematic diagram of the Low-Voltage Power Supply is shown in Figure 7-133. A detailed block diagram, showing each major stage of this circuit, is superimposed on the schematic with wide shaded lines. The stage names (given as sub-headings in the following discussion) can be found in the shaded blocks in Figure 7-133.

a. +20 Volt Unregulated Supply. The +20 Volt Unregulated Supply provides unregulated power for the other circuits in Figures 7-132 and 7-133. Fuse A2F226 provides circuit protection in the event of an overload.

b. +15 Volt Regulated Supply. The +15 Volt Regulated Supply, in addition to providing power to circuitry throughout the instrument, provides a reference-voltage source to establish the operating level for the feedback regulator of the -15 Volt Regulated Supply and -70 Volt Regulated Supply. The regulator for the +15 Volt Regulated Supply is a feedback amplifier system that operates between ground and the +20 Volt Unregulated Supply. Current to the load is delivered by the series-pass transistor A2Q241, which is located in the output side of the supply. The supply voltage is established by the drop across resistive-divider network A2R244-A2R245-

A2R246. The feedback through this network is compared to the reference level established at the input of A2U232A (pin 2) by the voltage drop across A2VR231. Any variation in output voltage of the supply (due to ripple change of current through the load, etc.) is immediately transmitted to the base of A2Q241 and nullified by a change in A2Q241 conduction, maintaining a steady output.

The series regulator, A2Q241, is protected against excessive current demand by a network consisting of A2CR236-A2CR237-A2CR238-A2R241. Essentially, all current from this supply flows through A2R241. When excess current is demanded from the +15 volt series regulator (due to a short circuit or similar malfunction at the output of this supply), the voltage drop across A2R241 increases enough to forward-bias A2CR236, A2CR237, and A2CR238, which in turn reduces the conduction of A2Q241 to limit the supply current to a safe level. Fuse A2F227 provides additional circuit protection in the event of a regulator malfunction.

The output of the supply is set to exactly +15 volts by adjustment of A2R245, the +15 V Adj.

c. -15 Volt Regulated Supply. The regulator for -15 Volt Regulated Supply consists of series-pass transistor A2Q265, with A2U232B being the control amplifier. Unregulated -20 volts, from which the regulator operates, comes from High-Voltage transformer A2T110, shown in Figure 7-133. This is a feedback amplifier system similar to that just described for the +15 Volt Regulated Supply.

d. -70 Volt Regulated Supply. The regulator for -70 Volt Regulated Supply consists of series-pass transistor A2Q285, with A2U175B being the control amplifier. Unregulated -75 volts, from which the regulator operates, comes from the High-Voltage transformer A2T110, shown in Figure 7-133.

This is a feedback amplifier system similar to those of +15 and -15 Volt Regulated Supply. The only difference is the use of a level-shifting transistor (A2Q280) rather than a level-shifting Zener diode.

7-13.6 CRT Mainframe X,Y,Z, and +20 Volt Input Connections

Deflection potentials (X, Y, and Z input signals) and operating power (+20V) are provided to the CRT mainframe A1 and A2 PCBs. Figure 7-129 shows the physical location of these input connections.

7-13.7 Parts Locator Diagrams

Parts locator diagrams for the CRT mainframe A1 and A2 PCBs are provided in Figures 7-134 and 7-135, respectively.

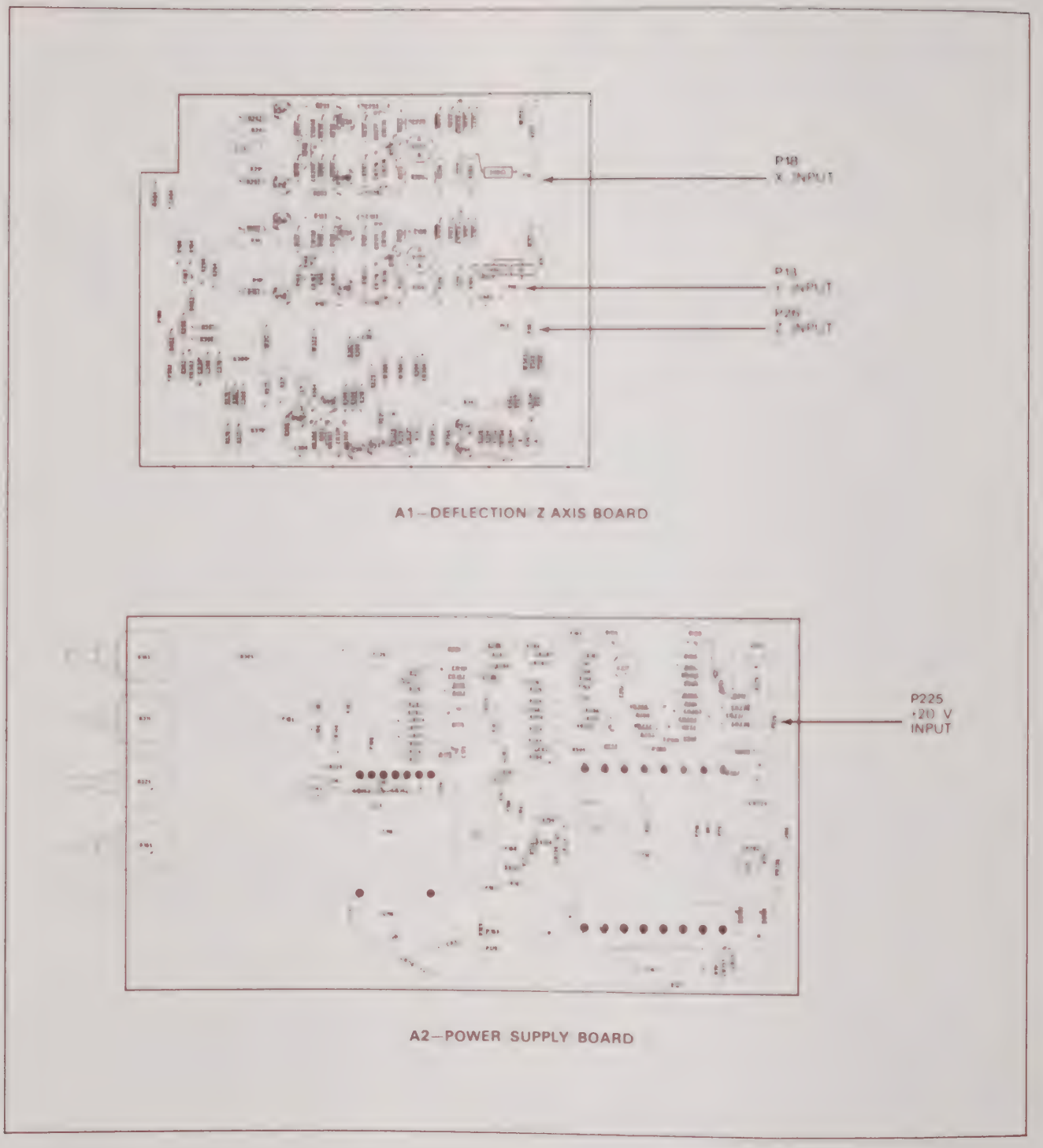


Figure 7-129. CRT Mainframe X, Y, Z, and +20V Input Connector Locations

VOLTAGE AND WAVEFORM CONDITIONS

NOTE

Voltage Conditions. The dc voltages indicated on the schematic diagrams were obtained with a digital multimeter and with no test signal input. The 620 INTENSITY and position controls were set for a barely visible spot positioned at near center screen.

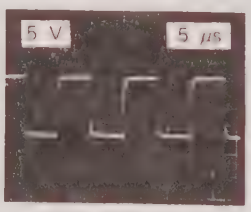
Waveform Conditions (Vertical Deflection Amplifier). The following waveforms were monitored with a test oscilloscope equipped with a X10 probe. A 0.5 peak to peak square wave was applied to the Y INPUT (J12) with the vertical position control (↕) centered. Test oscilloscope deflection factor and sweep rate settings appear on the waveform illustrations.

Waveform Conditions (Horizontal Deflection Amplifier). The following waveforms were monitored with a test oscilloscope equipped with a X10 probe. A 0.5 peak-to-peak square wave was applied to the X INPUT (J17) with the horizontal position control (↔)centered. Test oscilloscope deflection factor and sweep rate settings appear on the waveform illustrations.

1

+250 mV

2



-25 V

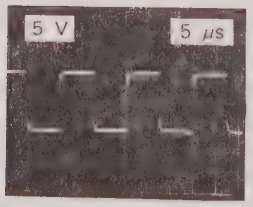
3

-34 V

4

+250 mV

5



-25 V

6

-34 V

A2 PARTIAL
POWER SUPPLY BOARD
A1 PARTIAL
DEFLECTION / Z AXIS

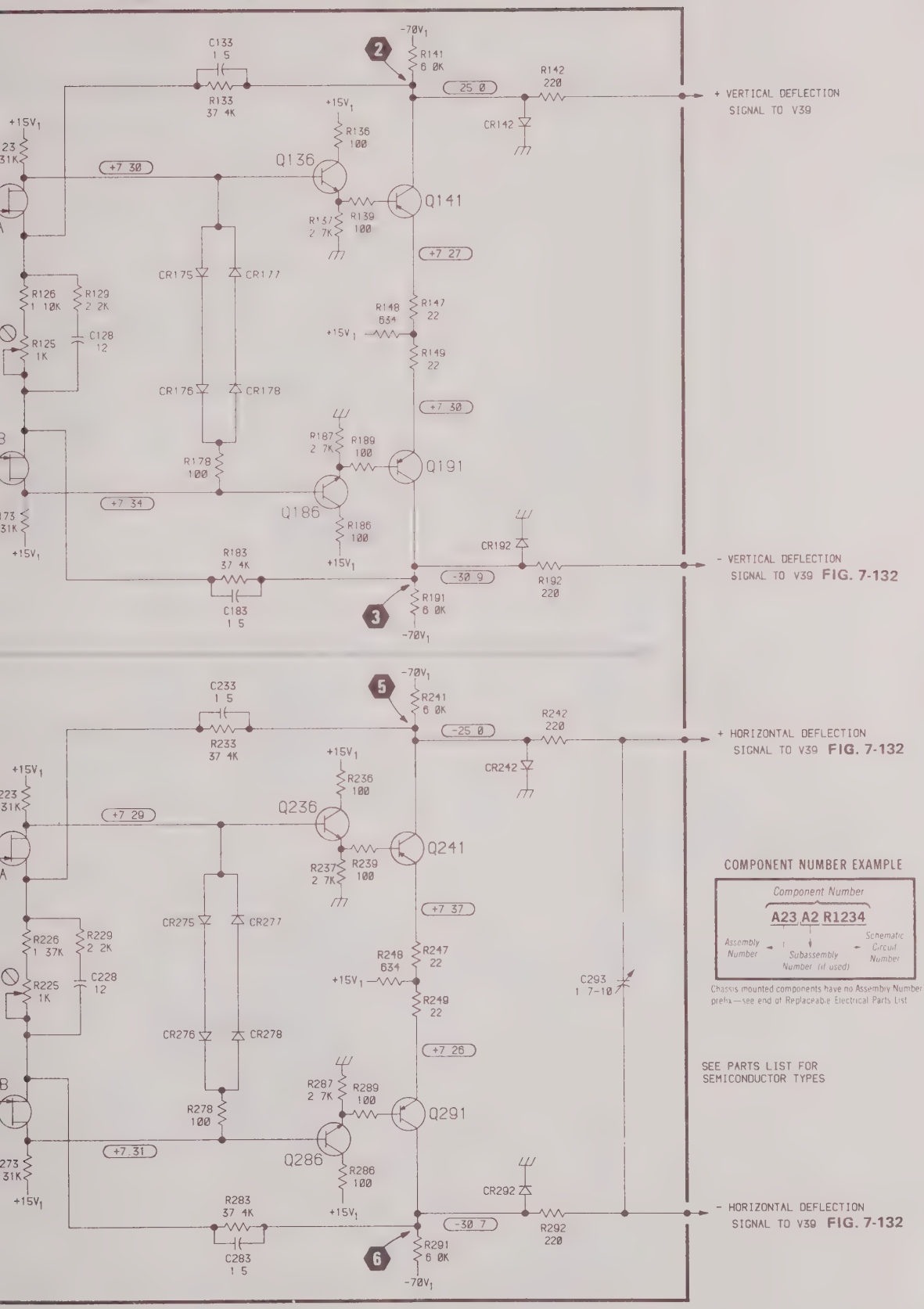
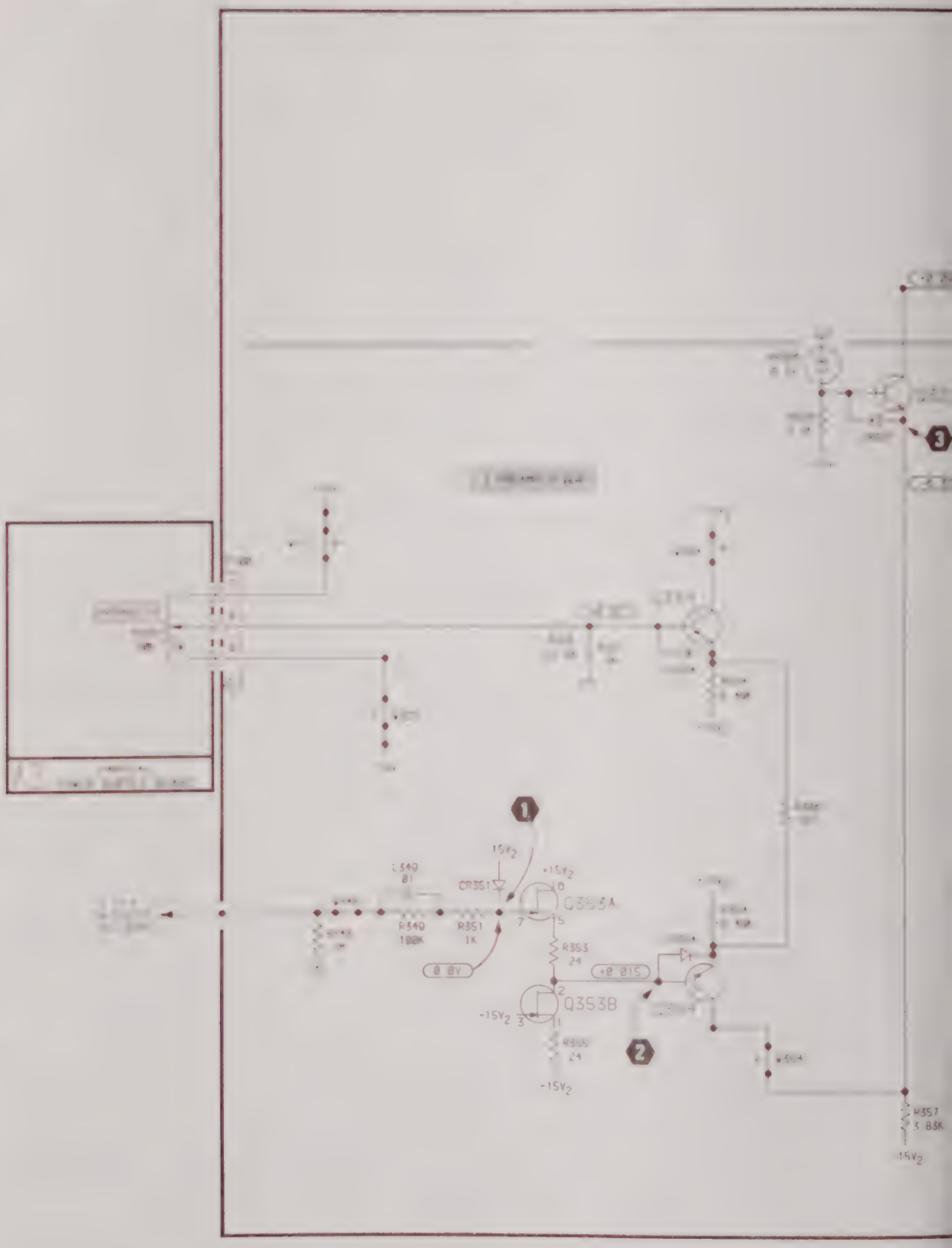
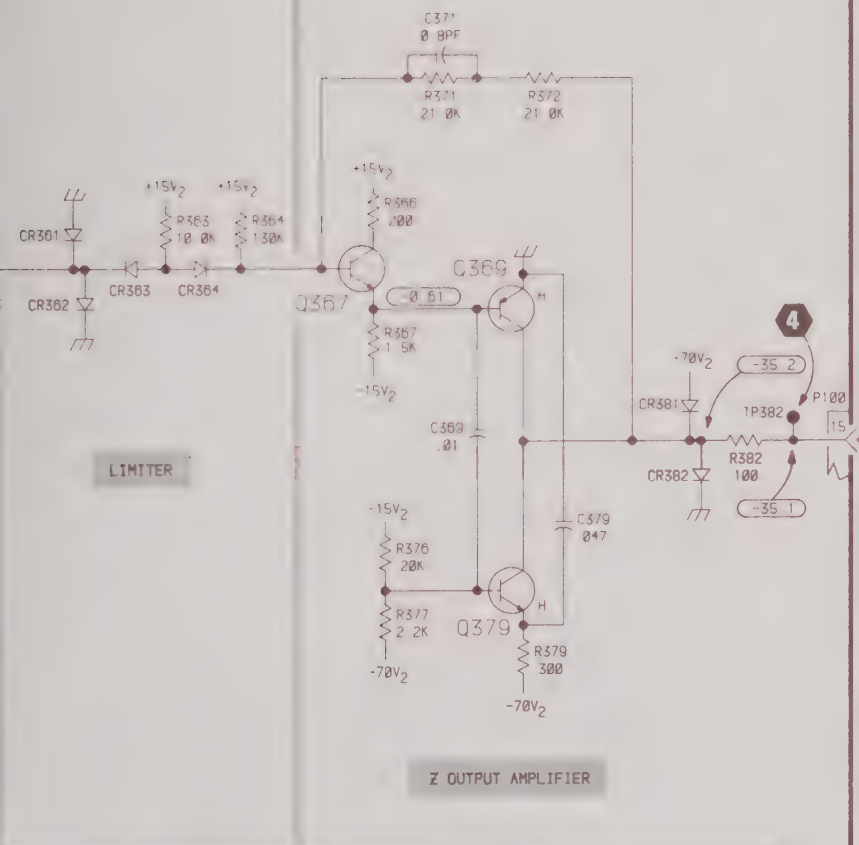
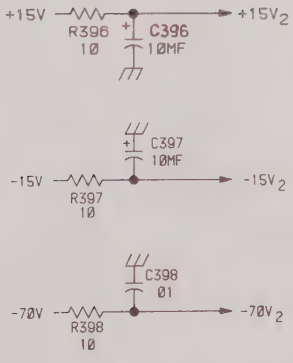


Figure 7-130. CRT Mainframe Deflection Amplifiers, Schematic Diagram


A
B
C
1
2
3
1
2
3
+15V2
CR351
Q353A
R351
1K
R353
24
+0.015
0.0V
Q353B
-15V2
R355
24
-15V2
R357
3.83K
15V2

2650-61





COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

A1 PARTIAL DEFLECTION / Z AXIS BOARD

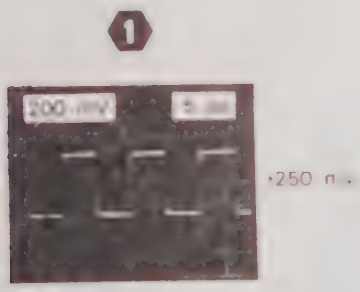
A2 PARTIAL POWER SUPPLY BOARD

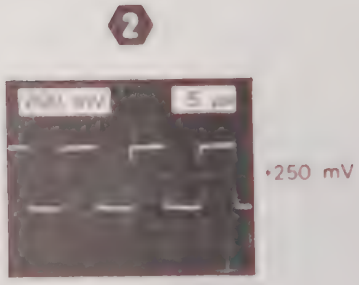
VOLTAGE AND WAVEFORM CONDITIONS

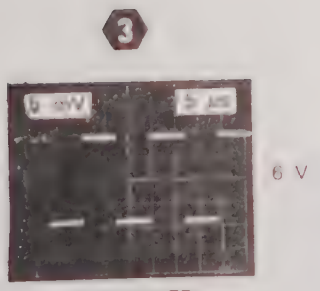
NOTE

Voltage Conditions. The dc voltages indicated [illegible] digital multimeter and with no test signal input. The 620 INTENSITY and positioning controls are set for a [illegible] at near center screen.

Waveform Conditions. The following waveforms were [illegible] with a X10 probe. A 0.5 volt peak-to-peak square wave was applied to the Z INPUT [illegible] off screen to prevent burning the crt phosphor. The INTENSITY control was set to [illegible] output). Test oscilloscope deflection factor and sweep rate settings appear [illegible].







AC COUPLED

Figure 7-131. CRT Mainframe Z-Axis Amplifier, Schematic Diagram

△See Title Page

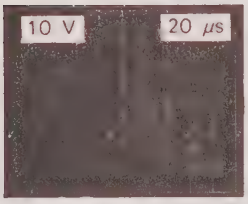
VOLTAGE AND WAVEFORM CONDITIONS

NOTE

Voltage Conditions. The dc voltages indicated on the schematic diagrams were obtained with a digital multimeter and with no test signal input. The 620 INTENSITY and position controls were set for a barely visible spot positioned at near center screen.

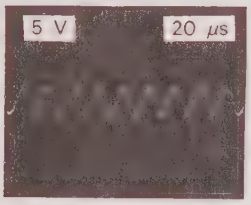
Waveform Conditions. The following waveforms were monitored with a test oscilloscope equipped with a X10 probe. The 620 INTENSITY and position controls were set for a barely visible spot positioned at near center screen. No input signals were applied to the monitor.

1



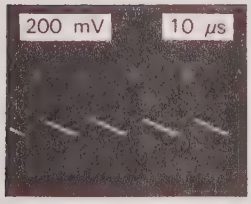
+24 V

2



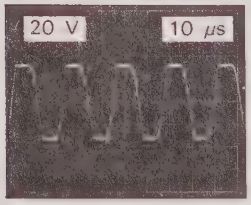
0 V

3

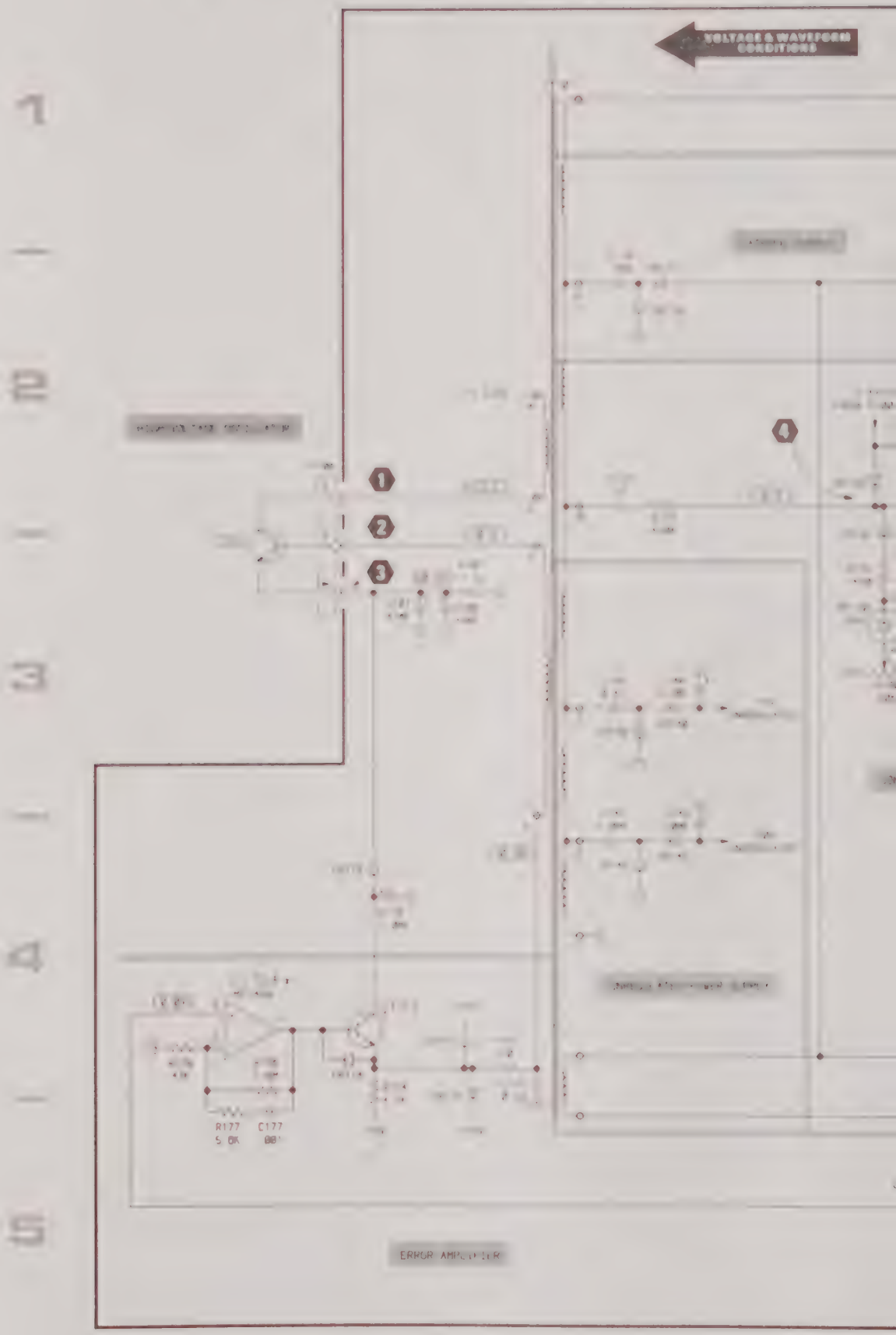


+1 V

4



-34 V


A
B
C
1
2
3
4
5
VOLTAGE & WAVEFORM CONDITIONS
1
2
3
4
R177
5.6K
C177
ERROR AMPLIFIER

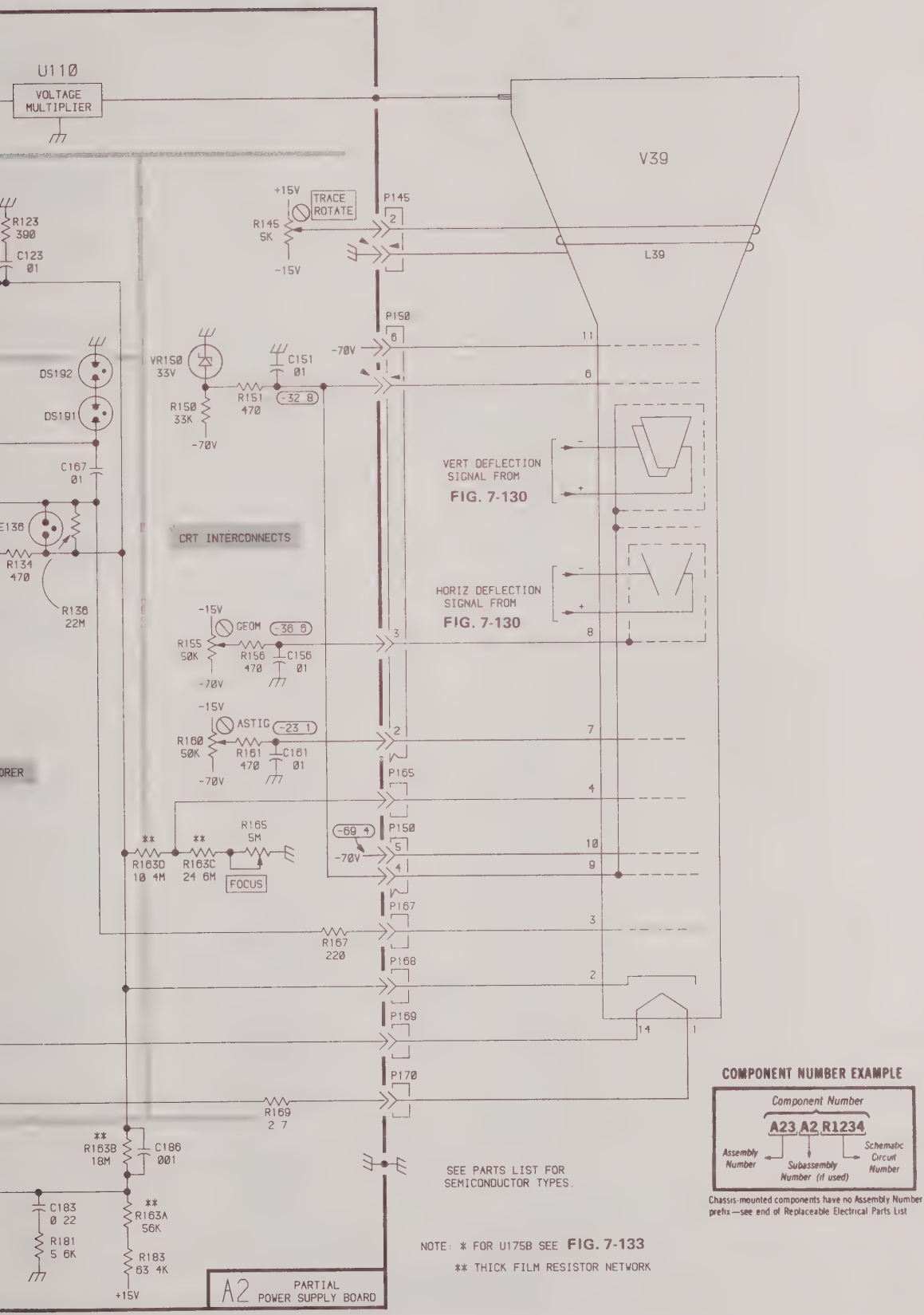
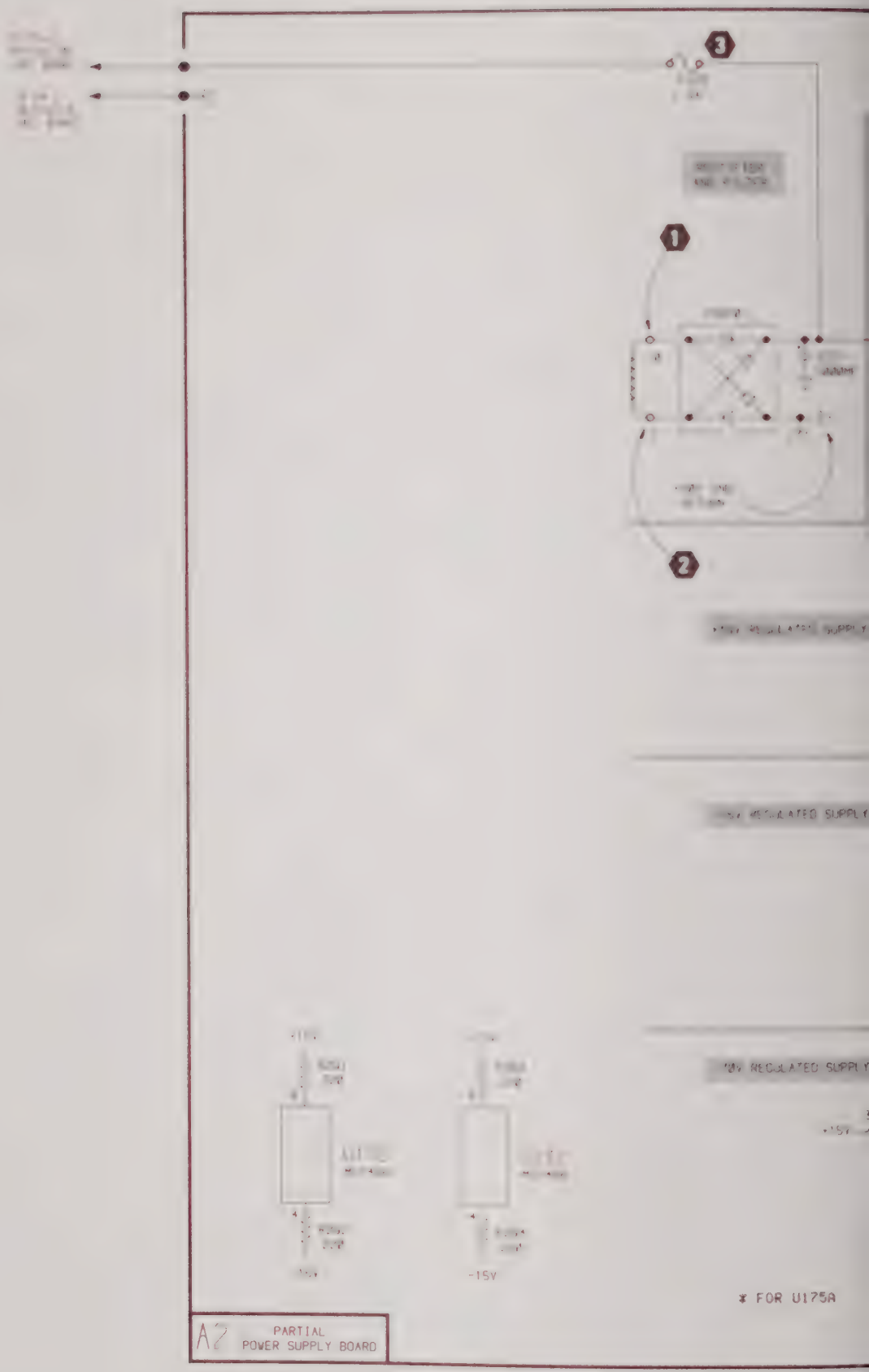
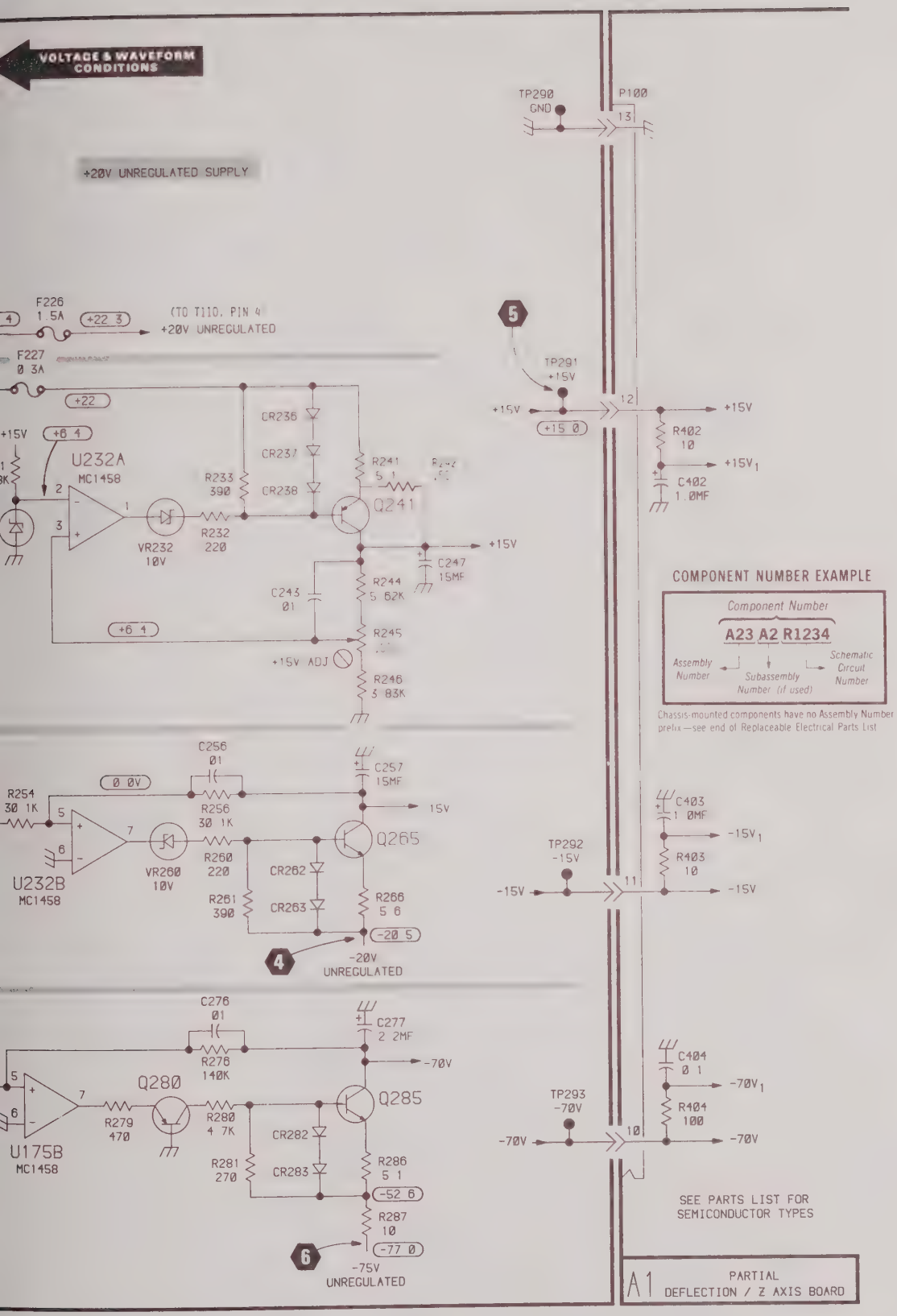


Figure 7-132. CRT Mainframe High-Voltage Power Supply, Schematic Diagram


3
1
2
-15V
* FOR U175A
A2 PARTIAL POWER SUPPLY BOARD

VOLTAGE & WAVEFORM CONDITIONS

+20V UNREGULATED SUPPLY

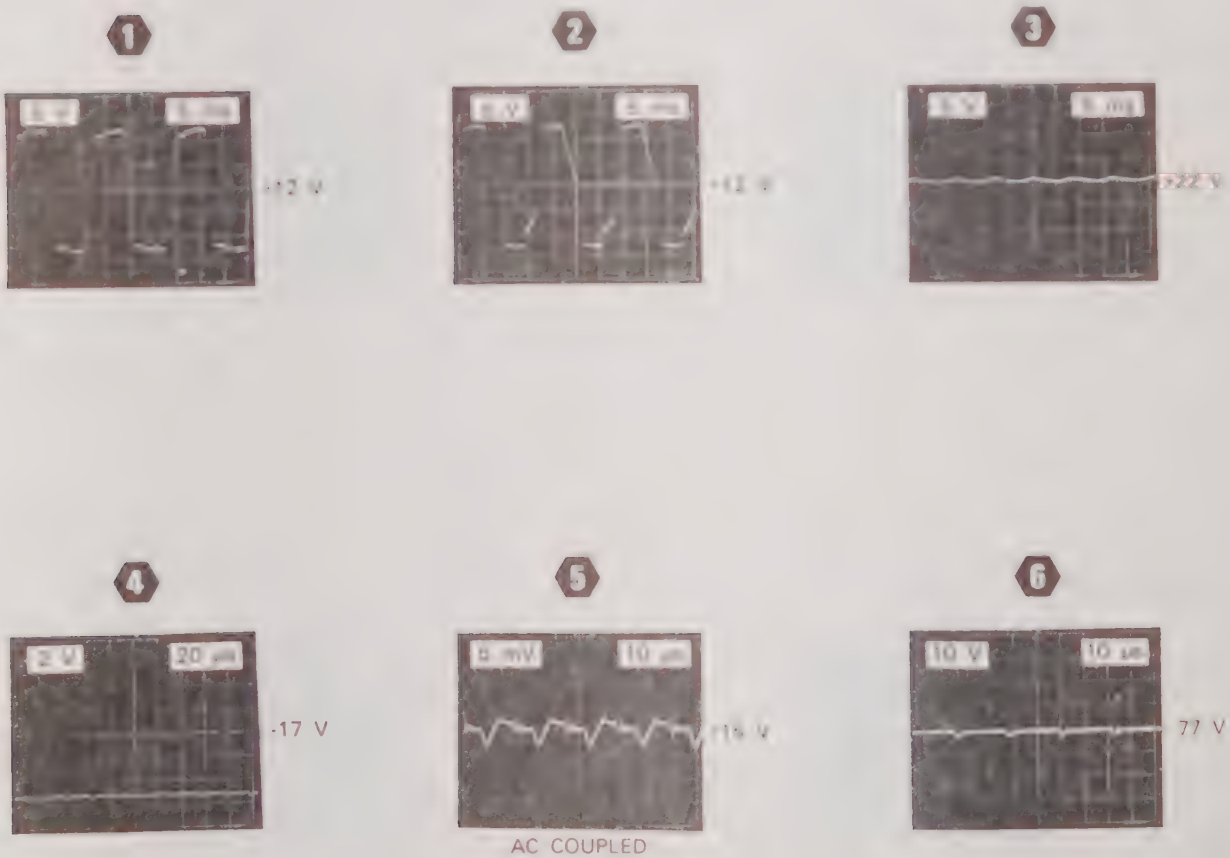


VOLTAGE AND WAVEFORM CONDITIONS

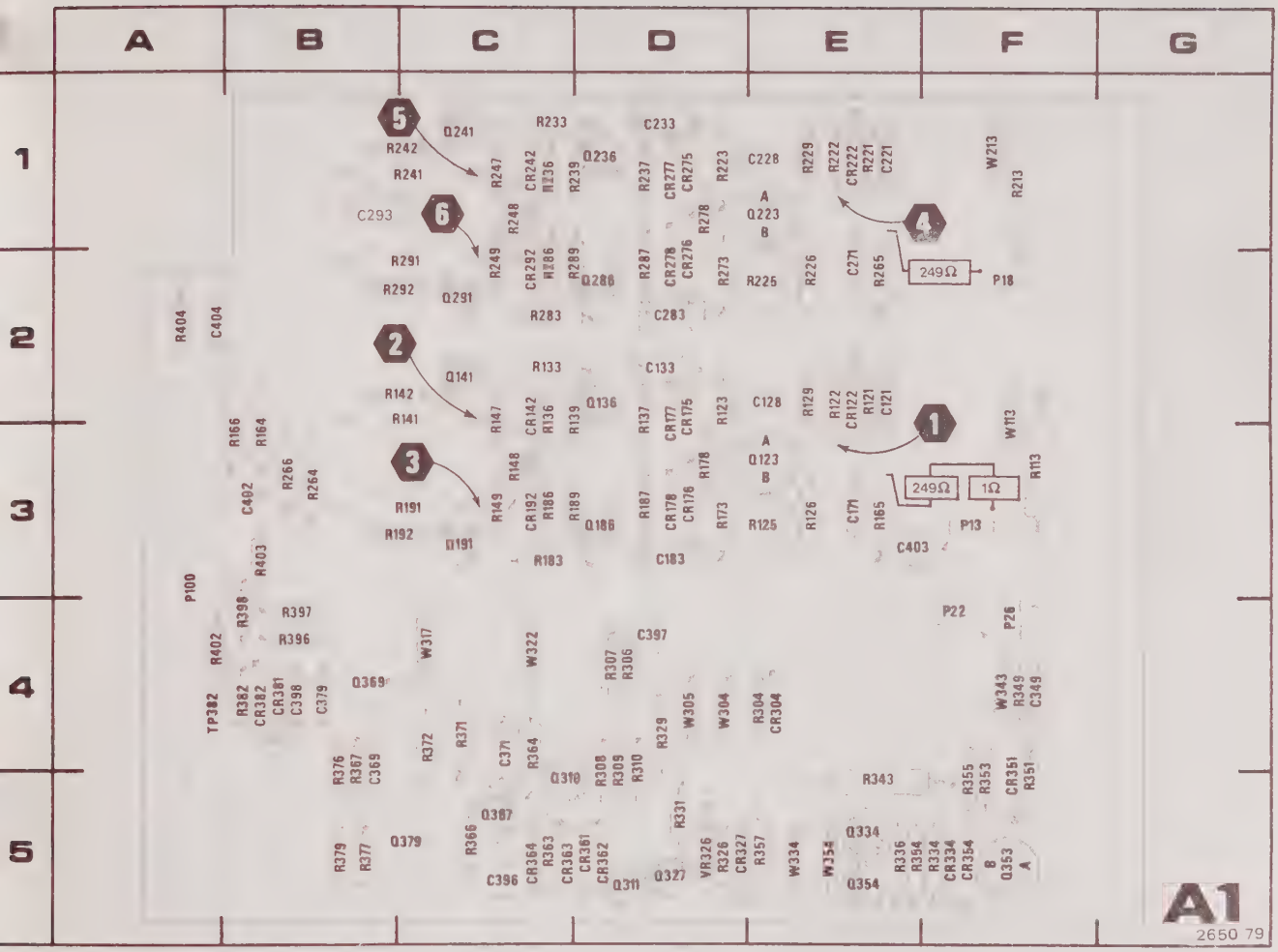
NOTE

Voltage Conditions. The dc voltages measured are the reference designation value with a digital multimeter and with the front panel scale. The 620 INTENSITY and position controls were set for a barely visible spot positioned at near center screen.

Waveform Conditions. The following waveforms were monitored with a test oscilloscope equipped with a 1:10 probe. The 620 INTENSITY and position controls were set for a barely visible spot positioned at near center screen. No input signals were applied to the mainframe.



← Figure 7-133. CRT Mainframe Low-Voltage Power Supply, Schematic Diagram



COMPONENT NUMBER EXAMPLE

Component Number

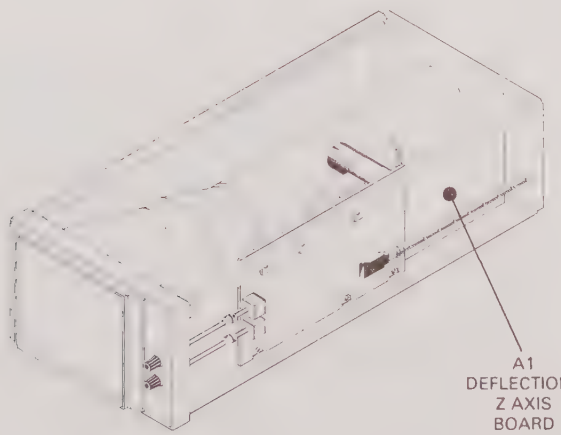
A23 A2 R1234

Assembly Number

Subassembly Number (if used)

Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List



P O A1 ASSY — Deflection Amplifiers FIG. 7-131

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION

P/O A1 ASSY also shown on Figures 7-131 & 7-133

P O A2 ASSY — Deflection Amplifiers FIG. 7-130

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R305	A2	B1*
R315	A5	B2*

*See Figure 7-135

P/O A2 ASSY also shown on Figures 7-131, 7-132 & 7-133

CHASSIS MOUNTED PARTS — Deflection Amplifiers FIG. 7-130

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J12	A1	CHASSIS	P1Q	A1	CHASSIS
J17	A4	CHASSIS	P10	A3	CHASSIS

P/O A1 ASSY			Z AXIS AMPLIFIER FIG. 7-131		
CIRCUIT NUMBER	SCHEM. LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM. LOCATION	BOARD LOCATION
C349	B3	F4	R307	C1	D4
C369	E2	B5	R308	C1	D4
C371	E1	C4	R309	C2	D4
C379	E2	B4	R310	C1	D4
C396	E3	C5	R326	C2	D5
C397	E4	D4	R329	B3	D4
C398	E4	B4	R331	C3	D5
			R334	C3	F5
CR304	B1	E4	R336	C3	E5
CR327	D2	D5	R343	B4	E5
CR334	C3	F5	R349	B4	F4
CR351	B4	F5	R351	B4	F5
CR354	C4	F5	R353	C4	F5
CR361	D1	D5	R354	C4	E5
CR362	D2	D5	R355	C4	F5
CR363	D2	C5	R357	D4	E5
CR364	D2	C5	R363	D1	C5
CR381	F2	B4	R364	E1	B3
CR382	F2	B4	R366	E1	C5
			R367	E2	B5
P22	A1	F4	R371	E1	C4
P26	A4	F4	R372	E1	C4
P100	A2	A3	R376	E2	B5
P100	F2	A3	R377	E2	B5
			R379	E3	B5
Q310	C1	C5	R382	F2	B4
Q311	C1	D5	R396	E3	B4
Q327	D2	D5	R397	E4	B4
Q334	C3	E5	R398	E4	B4
Q353A	C4	F5			
Q353B	C4	F5	TP382	F2	A4
Q354	C4	E5			
Q367	E2	C5	VR326	C2	D5
Q369	E2	B4			
Q379	E2	C5	W304	B1	D4
			W305	B1	D4
R304	B2	E4	W343	B4	F4
R306	C1	D4			

P/O A1 ASSY also shown on Figures 7-130 & 7-133

P/O A2 ASSY			Z AXIS AMPLIFIER FIG. 7-131
CIRCUIT NUMBER	SCHEM. LOCATION	BOARD LOCATION	
R325	A3	B3*	
*See Figure 7-135			

P/O A2 ASSY also shown on Figures 7-131, 7-132 & 7-133

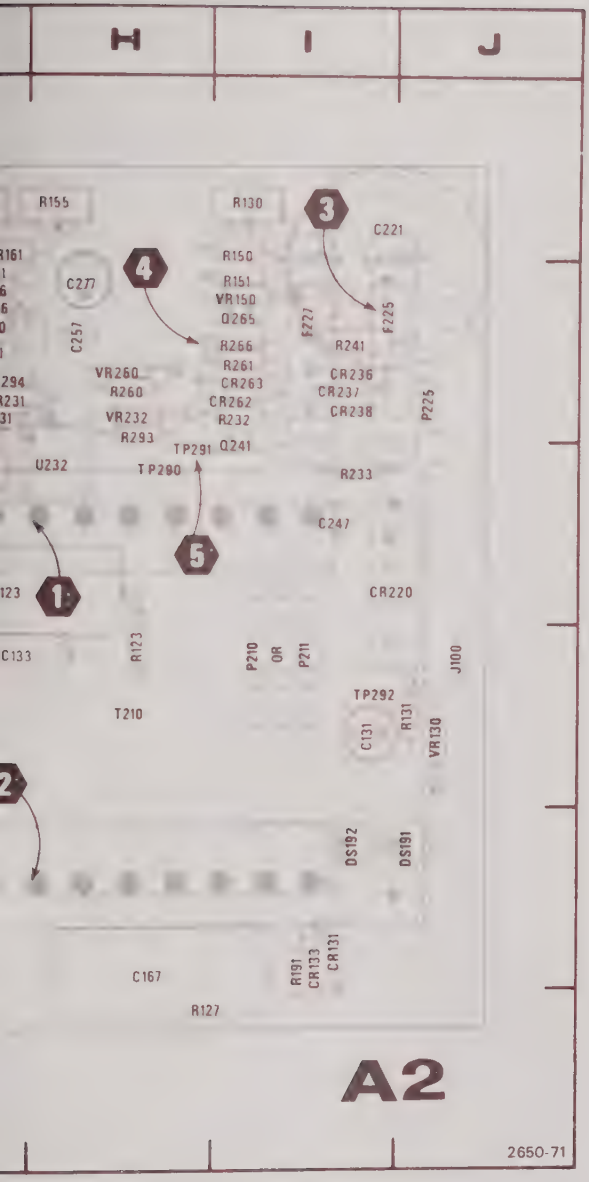
CHASSIS MOUNTED PARTS			Z AXIS AMPLIFIER FIG. 7-131		
CIRCUIT NUMBER	SCHEM. LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM. LOCATION	BOARD LOCATION
J21	A1	CHASSIS	P10	A1	CHASSIS
J25	A4	CHASSIS	P10	A4	CHASSIS

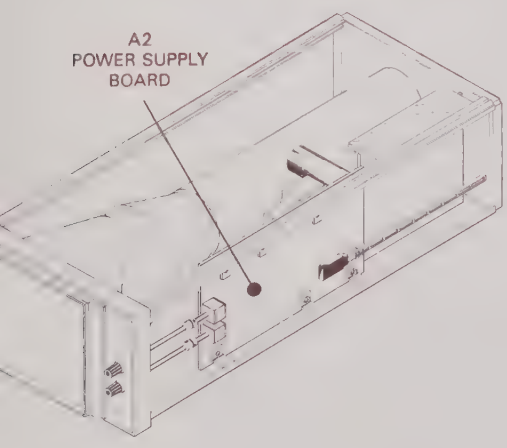
Figure 7-134. CRT Mainframe Deflection/Z-Axis PCB, Parts Locator Diagram

COMPONENT NUMBER EXAMPLE

A23 A2 R1234

Chassis mounted components have no Assembly Number prefix - see end of Replaceable Electrical Parts List





P/O A1 ASSY — **LOW-VOLTAGE POWER**

CIRCUIT NUMBER	SCHEM. LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SC LO
C402	F2	B3 *	R402	
C403	F3	E3 *	R403	
C404	F4	A2 *	R404	
P100	F1	A3 *		

*See Figure 7-13

P/O A1 ASSY also shown on Figures 7-130 & 7-131

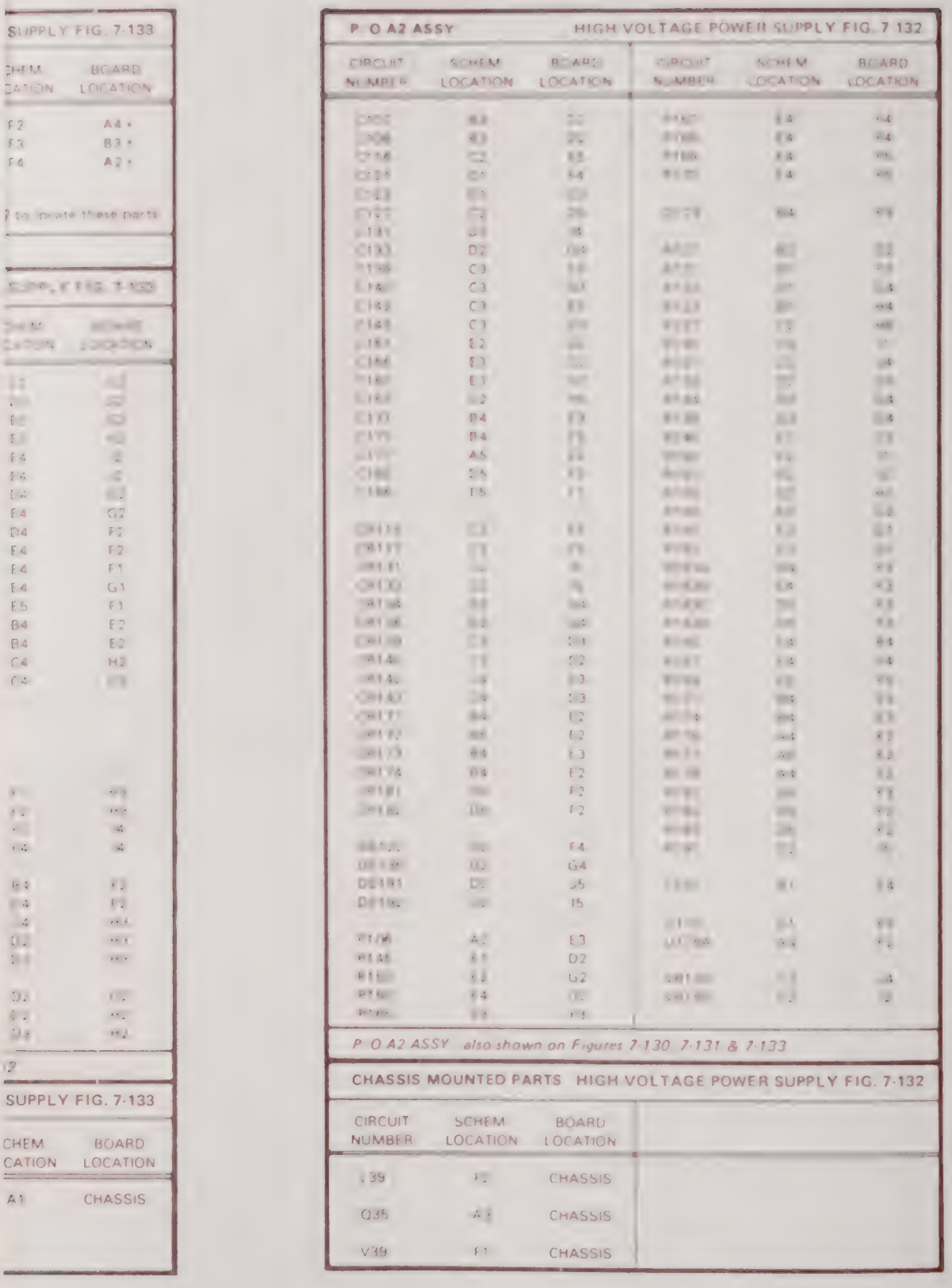
P/O A2 ASSY — **LOW-VOLTAGE POWER**

CIRCUIT NUMBER	SCHEM. LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SC LO
C221	D2	I1	R246	
C243	E3	G3	R254	
C247	E2	I3	R256	
C256	E3	G2	R260	
C257	E3	H2	R261	
C276	E4	G2	R266	
C277	E4	H2	R274	
			R276	
CR220	C2	I3	R279	
CR236	E2	I2	R280	
CR237	E2	I2	R281	
CR238	E2	I2	R286	
CR262	E3	I2	R287	
CR263	E4	I2	R291	
CR282	E4	G2	R292	
CR283	E4	G1	R293	
			R294	
F225	C1	I2		
F226	D2	E1		
F227	D2	I2		
P210	B2	I4		
P211	B2	I4	TP290	
P225	A1	J2	TP291	
			TP292	
Q241	E2	I3	TP293	
Q265	E3	I2		
Q280	D4	F2	U175	
Q285	E4	F1	U175B	
			U232	
R231	D2	G2	U232A	
R232	E2	I2	U232B	
R232	E2	I2		
R241	E2	I2	VR231	
R244	E2	G3	VR232	
R245	E3	G3	VR260	

P/O A2 ASSY also shown on Figures 7-130, 7-131 & 7-1

CHASSIS MOUNTED PARTS — **LOW-VOLTAGE POWER**

CIRCUIT NUMBER	SCHEM. LOCATION	BOARD LOCATION	CIRCUIT NUMBER	S LO
F42	A1	CHASSIS	P42	
P20	A1	CHASSIS		
P41	A2	CHASSIS		



SUPPLY FIG. 7-133

CHEM CATION	BOARD LOCATION
F2	A4 •
F3	B3 •
F4	A2 •

? to locate these parts

SUPPLY FIG. 7-133

CHEM CATION	BOARD LOCATION
A1	CHASSIS

P O A2 ASSY — HIGH VOLTAGE POWER SUPPLY FIG. 7-132

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C133	D2				
C143	C3				
C144	C3				
C145	C3				
C184	E3				
C185	E3				
C186	E5				
C190	B4				
C195	B4				
C196	A5				
C198	E5				
CR115	C3				
CR130					
CR140					
CR141					
CR142					
CR143					
CR171					
CR173					
CR174					
CR181					
CR185					
DS181					
DS182					
P144	A2	E3			
P145	A1	D2			

P O A2 ASSY also shown on Figures 7-130, 7-131 & 7-133

CHASSIS MOUNTED PARTS HIGH VOLTAGE POWER SUPPLY FIG. 7-132

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L39		CHASSIS
Q35		CHASSIS
V39		CHASSIS

Figure 7-135. CRT Mainframe Power Supply PCB, Parts Locator Diagram

7-14 DISASSEMBLY/REASSEMBLY INSTRUCTIONS

The 560A network analyzer is produced in two configurations--horizontal and vertical (Option 2)--and contains two major sections: CRT mainframe and network analyzer. To perform certain maintenance actions, it is necessary to separate the CRT mainframe section from the network analyzer section. These maintenance actions include (1) replacing the Digital (A2) PCB components or removing the front panel assembly on vertically-configured 560As and (2) replacing components on CRT mainframe section PCB's on horizontally-configured 560As. In the horizontal configuration, the CRT mainframe and network analyzer sections are mounted side-by-side; in the vertical configuration, the CRT mainframe section is mounted on top of the network analyzer section. Disassembly/reassembly instructions for separating these two sections are contained in paragraph 7-14.1.

To remove and replace a defective component on the Front Panel (A1) PCB, remove the front panel assembly from the network analyzer section and then disassemble the A1 PCB from the front panel itself. Instructions for front panel assembly removal/reinstallation, and for A1 PCB disassembly/reassembly are contained in paragraph 7-14.2.

7-14.1 Disassembly/Reassembly Instructions for Separating CRT Mainframe Section From Network Analyzer Section

Disassembly/reassembly instructions for separating the CRT mainframe section from the network analyzer section are contained below. Instructions for the horizontal configuration are given in subparagraph a and for the vertical configuration in subparagraph b.

a. Horizontal Configuration.

1. Disassembly Instructions.

(a) Remove the four corner brackets, two straight brackets, and cover plate from the 560A rear panel (Figure 7-136).

NOTE

When straight brackets are removed, cover plate will fall off.

(b) Remove the top cover from both the CRT mainframe and network analyzer sections.

(c) Remove side cover from network analyzer section.

(d) Remove top channel cover (Figure 7-137) from between CRT mainframe and network analyzer sections.

(e) Loosen the five channel-bracket screws approximately 2 to 3 turns; slide the bracket toward the rear and remove it from between CRT mainframe and network analyzer sections.

(f) Remove the 6-wire harness connector from plug A2P4 on Digital (A2) PCB.

(g) Remove the 3-wire harness connector from jack A4J2 on Power Supply (A4) PCB.

NOTE

If 560A contains Option 3 GPIB Interface, it may be necessary to remove the GPIB Interface Connector PCB to gain access to A4J2. This PCB can be removed by (1) disconnecting the interface-connector cable harness from plug A6P1 on the GPIB Interface (A6) PCB, (2) removing the two screws that secure the 560A Option 3 IEEE 488 (IEC 625-1) Interface panel to the rear of the 560A, and (3) pulling the interface panel straight away from the 560A.

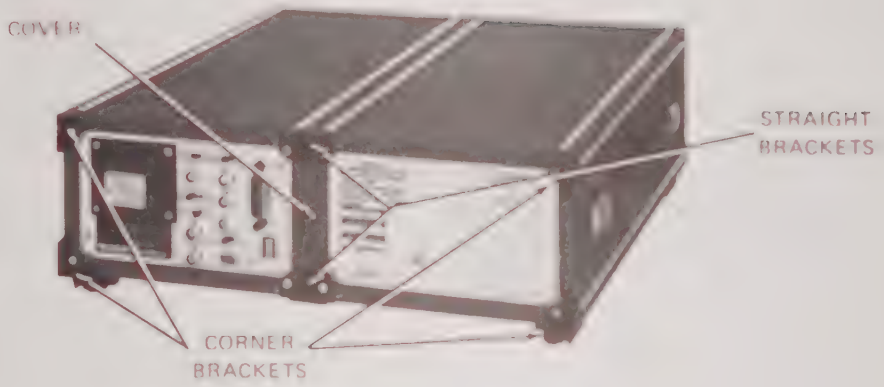


Figure 7-136. 560A Horizontal Configuration With Rear Panel Brackets Indexed

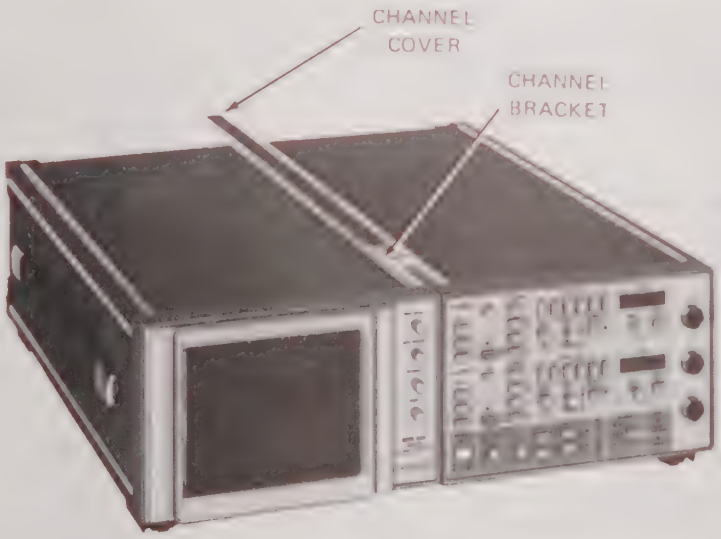


Figure 7-137. 560A Horizontal Configuration With Channel Cover and Channel Bracket Indexed

(h) Hold the two sections together and turn 560A upside down.

(i) Remove bottom channel cover and bottom channel bracket (refer to steps (d) and (e) above).

(j) Separate the two sections.

2. Reassembly Instructions. Reassembly is a reversal of the disassembly instructions.

b. Vertical Configuration.

1. Disassembly Instructions.

(a) Remove the four corner brackets, two straight brackets, and cover plate from the 560A rear panel (Figure 7-138).

NOTE

When straight brackets are removed, cover plate will fall off.

(b) Lay 560A on its right side (INTENSITY and FOCUS controls on CRT mainframe down).

(c) Remove side cover from CRT mainframe and network analyzer sections.

(d) Remove bottom cover from network analyzer section.

(e) Remove the 6-wire harness connector from plug A2P4 on Digital (A2) PCB.

(f) Remove the 3-wire harness connector from jack A4J2 on Power Supply (A4) PCB.

NOTE

If 560A contains Option 3 GPIB Interface, it may be necessary to remove the GPIB Interface Connector PCB to gain access to A4J2. This PCB can be removed by (1) disconnecting the interface-connector cable harness from plug A6P1 on the GPIB Interface (A6) PCB, (2) removing the two screws that secure the 560A Option 3 (IEEE 488/IEC 625-1) Interface panel to the rear of the 560A, and (3) pulling the interface panel straight away from the 560A.

(g) Remove channel cover (Figure 7-139) from between CRT mainframe and network analyzer sections.

(h) Loosen the five screws on the channel bracket approximately 2 to 3 turns; slide the bracket toward the rear and remove it from between the CRT mainframe and network analyzer sections.

(i) Hold the two sections together and turn 560A over on its left side.

(j) Remove channel cover and channel bracket (refer to steps (g) and (h) above).

(k) Separate the two sections.

2. Reassembly Instructions. Reassembly is a reversal of the disassembly instructions.

Figure 7-138. 560A Vertical Configuration With Rear Panel Brackets Indexed

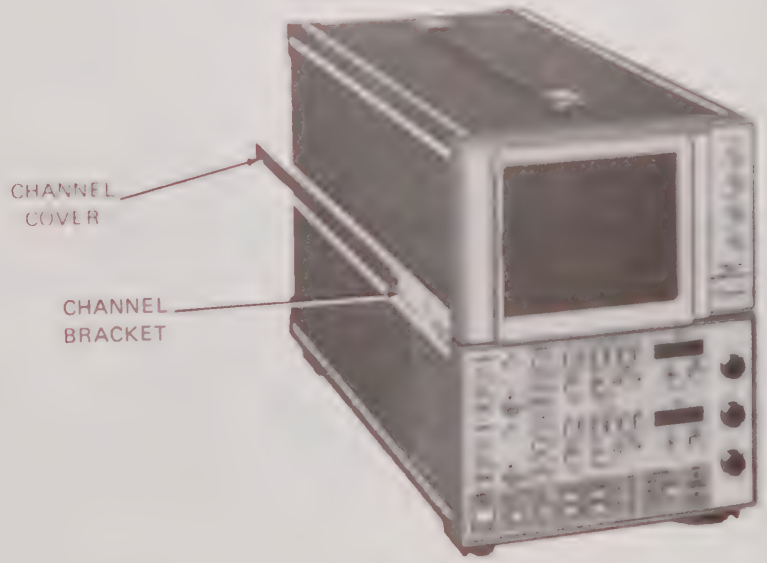


Figure 7-139. 560A Vertical Configuration With Channel Cover and Channel Bracket Indexed

7-14.2 Disassembly/Reassembly Instructions For Network Analyzer Section Front Panel Assembly

Disassembly/reassembly instructions for the network analyzer section front panel assembly are given below. Instructions are the same for either the 560A horizontal or vertical configuration. Disassembly instructions are given in subparagraph a, and reassembly instructions in paragraph b.

a. Disassembly Instructions.

1. Position network analyzer section upside down.

2. Remove connector from jack A2J1 on Digital (A2) PCB. Fold this flatwire harness back, over front panel assembly (Figure 7-140) and out of the way.

3. Remove Channel R connector from plug A3P1 (on Log Amplifier PCB), and Channel A and B connectors from their respective CHAN A and B Input Module plugs. Tag connectors for identification on reinstallation.

4. Remove cable clamps (Figure 7-140) and fold cable harness back, over front panel assembly and out of the way (Figure 7-141).

5. Remove connectors from A1P1, A1P2, and A1P3 on Front Panel (A1) PCB (Figure 7-141).

6. Loosen front panel retaining screws using 3/32-inch hex wrench (Allen wrench). These retaining screws are located in the four corners of the panel (Figure 7-141). To prevent binding, all four screws should be loosened 2 to 3 turns before any one screw is loosened all the way.

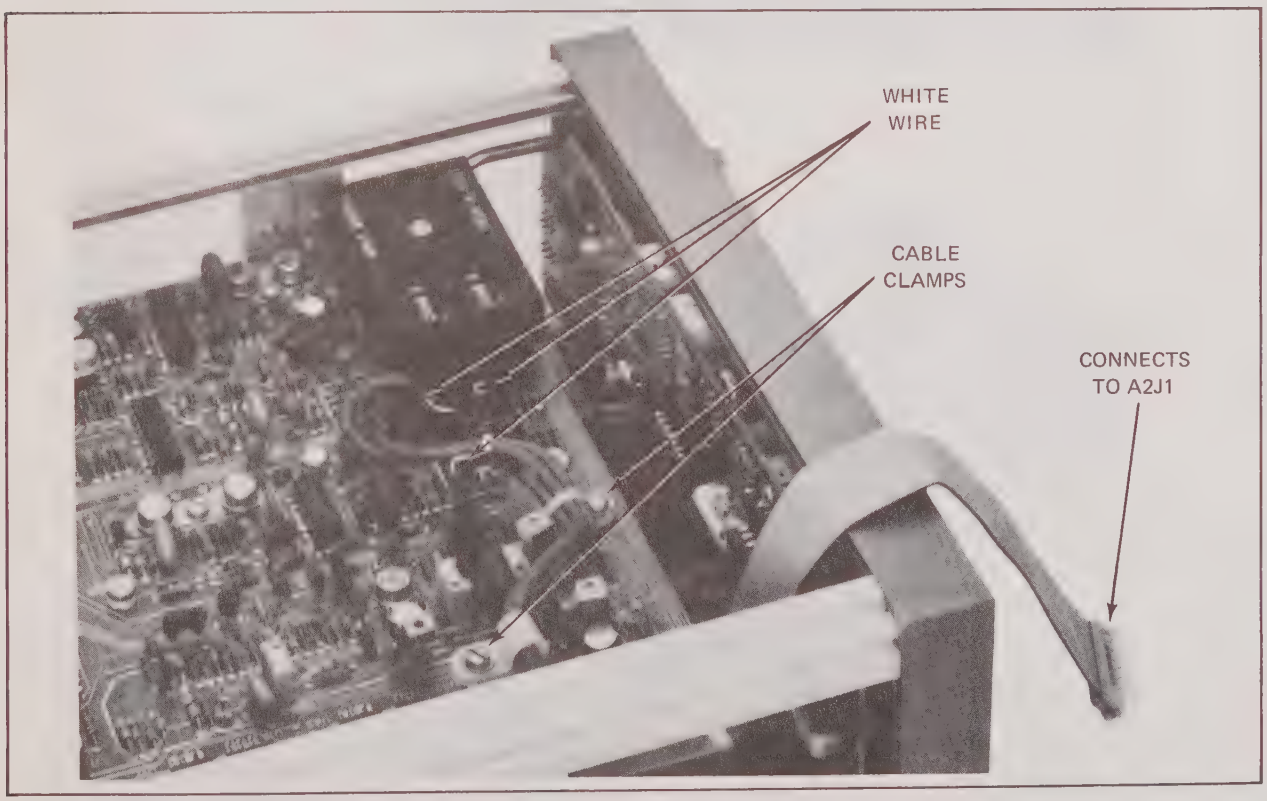


Figure 7-140. Network Analyzer Section With Input Cable Clamps Indexed

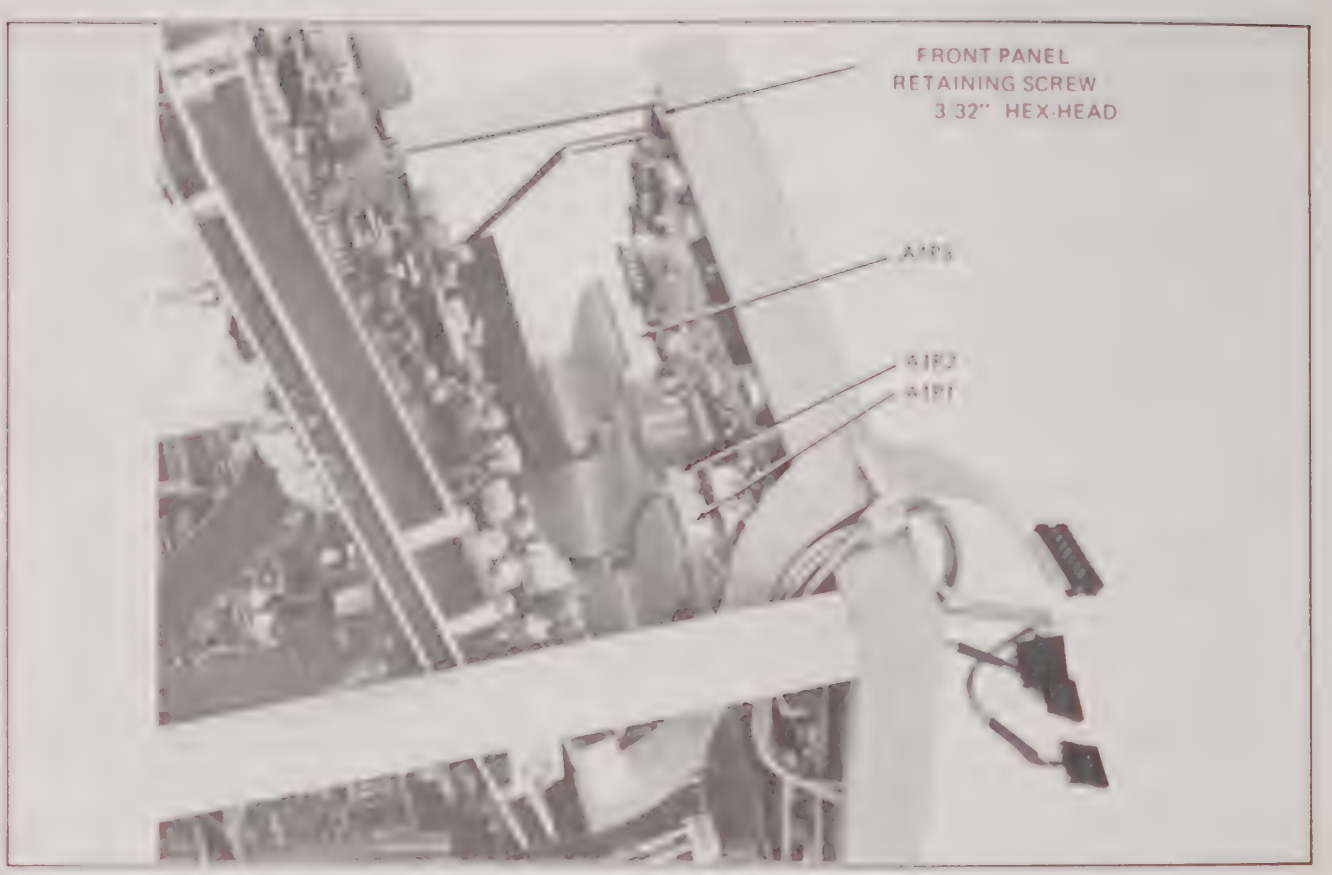


Figure 7-141. Network Analyzer Section With Connectors A1P1, A1P2, and A1P3 Indexed

NOTE

On vertically configured 560As, the RF shield will have to be removed to gain access to retaining screws located in the top right- and left-hand corners.

7. Remove front panel assembly from network analyzer section.

NOTE

The following steps provide instructions for disassembling the A1 PCB from the front panel plate.

8. Remove the knobs from the following controls: Channel A OFFSET, Channel B OFFSET, TILT, and THRESHOLD (Figure 7-142). To remove, pull knobs straight off.

NOTE

Do not remove knobs from ZERO dB SET controls.

9. Remove the 5 retaining screws and flatwashers from the A1 PCB (Figure 7-143). To prevent binding, all five screws should be loosened 2 to 3 turns before any one screw is removed.

10. Lift A1 PCB straight away from the front panel plate.

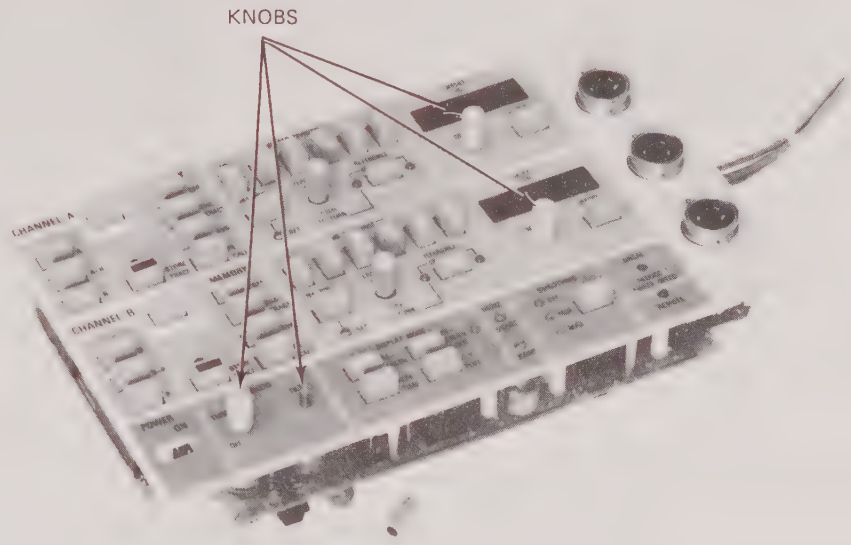


Figure 7-142. Front Panel Assembly With Knobs That Require Removal Indexed

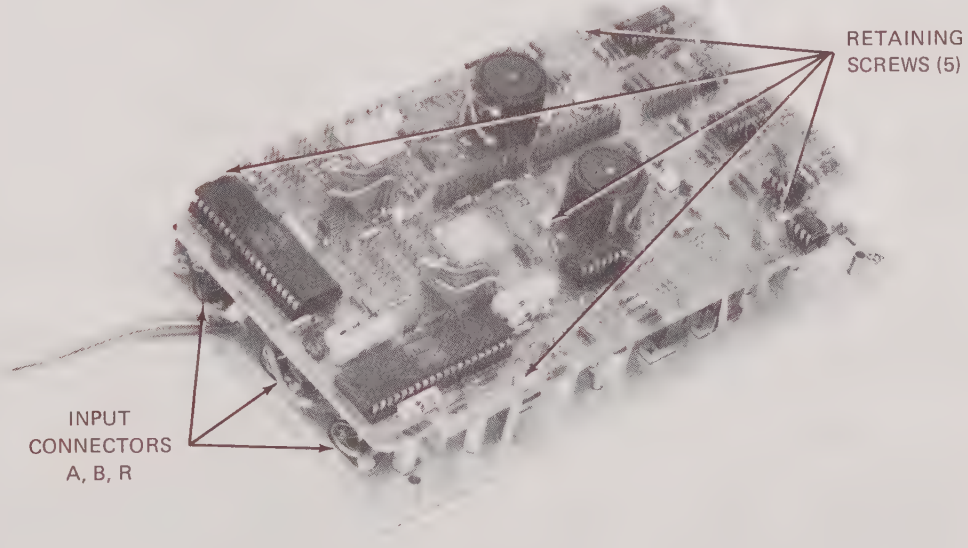


Figure 7-143. Front Panel Assembly With A1 PCB Retaining Screws and Input Connectors Indexed

Reassembly Instructions

1. Reinstall A1 PCB onto front panel plate; PCB should fit flush with, and be resting on, each of the five retaining screw standoffs.

2. Reinstall center retaining screw and flatwasher.

3. Check each of the front panel pushbutton switches and insure that none are binding.

4. Reinstall the remaining four retaining screws and flatwashers.

5. Reinstall knobs on front panel controls. Knob with index mark goes on THRESHOLD control.

6. Inspect input connectors (Figure 7-143) for broken or chafed wires.

7. Reinstall front panel assembly on network analyzer section chassis; tighten the four retaining screws.

8. Reinstall connectors on plugs A1P1, A1P2, and A1P3. Refasten Log Amplifier to network analyzer section chassis.

9. Reconnect A, B, and R connectors; orient connectors so that white wire is positioned as shown in Figure 7-140.

NOTE

If connectors are not tagged, they may be identified as follows: Channel A connector is attached to longest cable, Channel B connector is attached to second-longest cable, and Channel R connector is attached to shortest cable.

10. Reconnect flatwire harness connector to jack A2J1.

11. Reinstall RF shield (vertical configuration).

7-14.3 Disassembly Reassembly Instructions for Fan Assembly in Network Analyzer Section

a. Disassembly Instructions

1. Position network analyzer upside down

2. Remove the two corner and two straight brackets, and slide off the bottom cover.

3. Remove the retaining screws from the A3 PCB, and tilt the PCB up and away from the A4 PCB.

4. Remove the four screws from the corners of the rear panel.

5. Carefully pull the panel away from the unit just enough to disconnect the fan leads from pins J and K.

6. Remove the two mounting bracket screws from the foil side of the A4 PCB, and remove the fan assembly.

b. Reassembly Instructions

Reassembly is a reverse of the disassembly procedure in subparagraph a. above.

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